

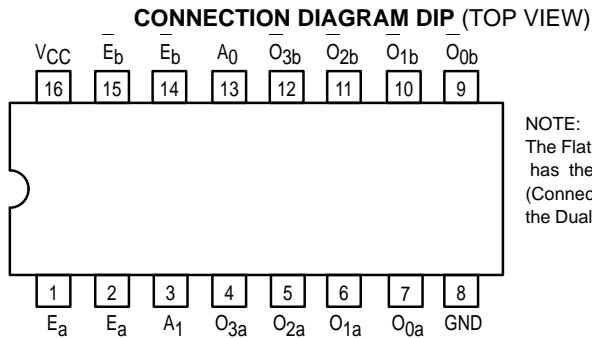


# DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

The SN54/74LS155 and SN54/74LS156 are high speed Dual 1-of-4 Decoder/Demultiplexers. These devices have two decoders with common 2-bit Address inputs and separate gated Enable inputs. Decoder "a" has an Enable gate with one active HIGH and one active LOW input. Decoder "b" has two active LOW Enable inputs. If the Enable functions are satisfied, one output of each decoder will be LOW as selected by the address inputs. The LS156 has open collector outputs for wired-OR (DOT-AND) decoding and function generator applications.

The LS155 and LS156 are fabricated with the Schottky barrier diode process for high speed and are completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Common Address Inputs
- True or Complement Data Demultiplexing
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts



NOTE:  
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

### PIN NAMES

A<sub>0</sub>, A<sub>1</sub> Address Inputs  
 E<sub>a</sub>, E<sub>b</sub> Enable (Active LOW) Inputs  
 E<sub>a</sub> — Enable (Active HIGH) Input  
 O<sub>0</sub>–O<sub>3</sub> Active LOW Outputs (Note b)

### LOADING (Note a)

HIGH	LOW
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
0.5 U.L.	0.25 U.L.
10 U.L.	5 (2.5) U.L.

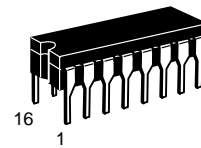
### NOTES:

- a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.  
 b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges. The HIGH level drive for the LS156 must be established by an external resistor.

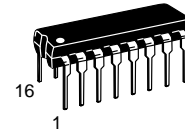
## SN54/74LS155 SN54/74LS156

### DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

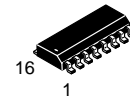
LS156-OPEN-COLLECTOR  
LOW POWER SCHOTTKY



**J SUFFIX**  
CERAMIC  
CASE 620-09



**N SUFFIX**  
PLASTIC  
CASE 648-08

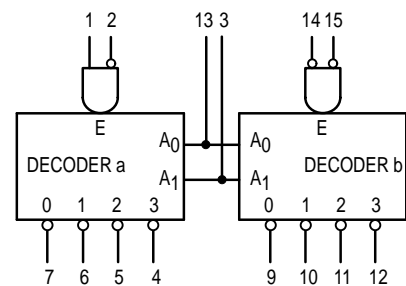


**D SUFFIX**  
SOIC  
CASE 751B-03

### ORDERING INFORMATION

SN54LSXXXJ Ceramic  
 SN74LSXXXN Plastic  
 SN74LSXXXD SOIC

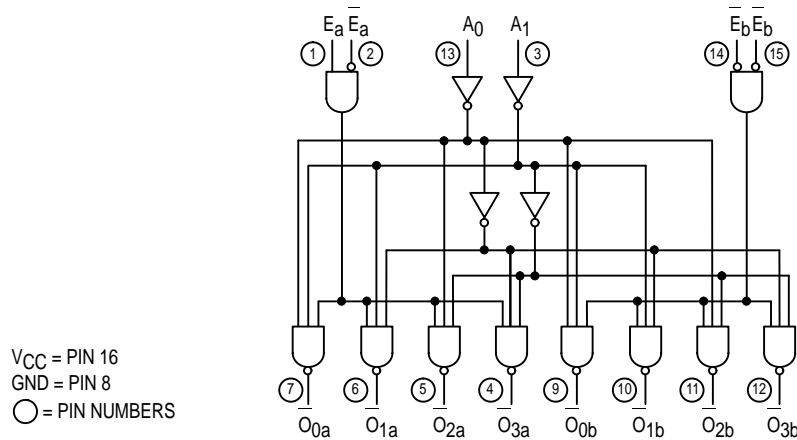
### LOGIC SYMBOL



V<sub>CC</sub> = PIN 16  
GND = PIN 8

# SN54/74LS155 • SN54/74LS156

## LOGIC DIAGRAM



## FUNCTIONAL DESCRIPTION

The LS155 and LS156 are Dual 1-of-4 Decoder/Demultiplexers with common Address inputs and separate gated Enable inputs. When enabled, each decoder section accepts the binary weighted Address inputs ( $A_0, A_1$ ) and provides four mutually exclusive active LOW outputs ( $O_0-O_3$ ). If the Enable requirements of each decoder are not met, all outputs of that decoder are HIGH.

Each decoder section has a 2-input enable gate. The enable gate for Decoder "a" requires one active HIGH input and one active LOW input ( $E_a \bullet \bar{E}_a$ ). In demultiplexing applications, Decoder "a" can accept either true or complemented data by using the  $E_a$  or  $\bar{E}_a$  inputs respectively. The enable gate for Decoder "b" requires two active LOW inputs ( $\bar{E}_b \bullet E_b$ ). The LS155 or LS156 can be used as a 1-of-8 Decoder/Demultiplexer by tying  $\bar{E}_a$  to  $\bar{E}_b$  and relabeling the common connection as ( $A_2$ ). The other  $E_b$  and  $E_a$  are connected together to form the common enable.

The LS155 and LS156 can be used to generate all four minterms of two variables. These four minterms are useful in some applications replacing multiple gate functions as shown in Fig. a. The LS156 has the further advantage of being able to

AND the minterm functions by tying outputs together. Any number of terms can be wired-AND as shown below.

$$f = (\bar{E}_a + A_0 + A_1) \cdot (E + \bar{A}_0 + A_1) \cdot (E + A_0 + \bar{A}_1) \cdot (E + A_0 + A_1)$$

$$\text{where } E = E_a + \bar{E}_a; \bar{E} = E_b + \bar{E}_b$$

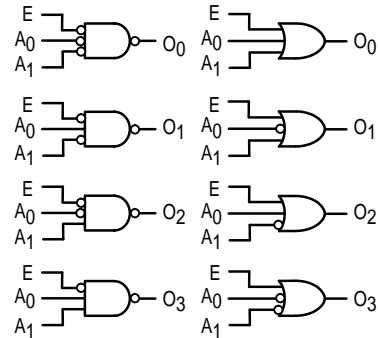


Figure a

## TRUTH TABLE

ADDRESS		ENABLE "a"		OUTPUT "a"				ENABLE "b"		OUTPUT "b"			
$A_0$	$A_1$	$E_a$	$\bar{E}_a$	$O_0$	$O_1$	$O_2$	$O_3$	$\bar{E}_b$	$E_b$	$O_0$	$O_1$	$O_2$	$O_3$
X	X	L	X	H	H	H	H	H	X	H	H	H	H
X	X	X	H	H	H	H	H	X	H	H	H	H	H
L	L	H	L	L	H	H	H	L	L	L	H	H	H
H	L	H	L	H	L	H	H	L	L	H	L	H	H
L	H	H	L	H	H	L	H	L	L	H	H	L	H
H	H	H	L	H	H	H	L	L	L	H	H	H	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care

# SN54/74LS155

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T <sub>A</sub>	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
I <sub>OH</sub>	Output Current — High	54, 74			-0.4	mA
I <sub>OL</sub>	Output Current — Low	54, 74			4.0 8.0	mA

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA	
V <sub>OH</sub>	Output HIGH Voltage	54	2.5	3.5	V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> per Truth Table	
		74	2.7	3.5	V		
V <sub>OL</sub>	Output LOW Voltage	54, 74		0.25	0.4	V	V <sub>CC</sub> = V <sub>CC</sub> MIN, V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> per Truth Table
		74		0.35	0.5	V	
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V	
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V	
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V	
I <sub>OS</sub>	Short Circuit Current (Note 1)	-20		-100	mA	V <sub>CC</sub> = MAX	
I <sub>CC</sub>	Power Supply Current			10	mA	V <sub>CC</sub> = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Address, E <sub>a</sub> or E <sub>b</sub> to Output		10 19	15 30	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Address to Output		17 19	26 30	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E <sub>a</sub> to Output		18 18	27 27	ns	

## AC WAVEFORMS

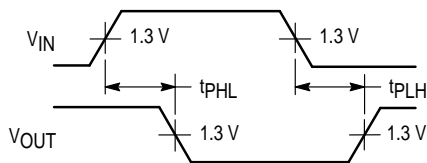


Figure 1

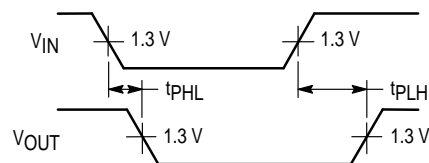


Figure 2

# SN54/74LS156

## GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V <sub>CC</sub>	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T <sub>A</sub>	Operating Ambient Temperature Range	54	-55	25	125	°C
		74	0	25	70	
V <sub>OH</sub>	Output Voltage — High	54, 74			5.5	V
I <sub>OL</sub>	Output Current — Low	54			4.0	mA
		74			8.0	

## DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V <sub>IH</sub>	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V <sub>IL</sub>	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74		0.8		
V <sub>IK</sub>	Input Clamp Diode Voltage		-0.65	-1.5	V	V <sub>CC</sub> = MIN, I <sub>IN</sub> = -18 mA
I <sub>OH</sub>	Output HIGH Current	54, 74		100	μA	V <sub>CC</sub> = MIN, V <sub>OH</sub> = MAX
V <sub>OL</sub>	Output LOW Voltage	54, 74	0.25	0.4	V	I <sub>OL</sub> = 4.0 mA
		74	0.35	0.5	V	I <sub>OL</sub> = 8.0 mA
I <sub>IH</sub>	Input HIGH Current			20	μA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 2.7 V
				0.1	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 7.0 V
I <sub>IL</sub>	Input LOW Current			-0.4	mA	V <sub>CC</sub> = MAX, V <sub>IN</sub> = 0.4 V
I <sub>CC</sub>	Power Supply Current			10	mA	V <sub>CC</sub> = MAX

## AC CHARACTERISTICS (T<sub>A</sub> = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Address, E <sub>a</sub> or E <sub>b</sub> to Output		25 34	40 51	ns	V <sub>CC</sub> = 5.0 V C <sub>L</sub> = 15 pF R <sub>L</sub> = 2.0 kΩ
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Address to Output		31 34	46 51	ns	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay E <sub>a</sub> to Output		32 32	48 48	ns	

## AC WAVEFORMS

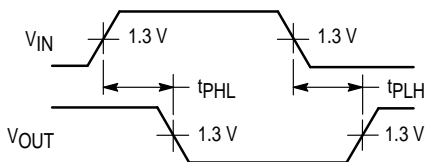


Figure 1

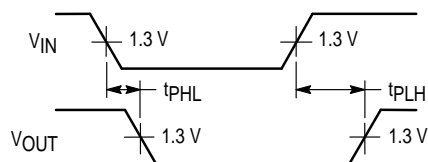


Figure 2