Product Preview

Dual Differential 2:1 Multiplexer

The MC10EP56 is a dual, fully differential 2:1 multiplexer. The differential data path makes the device ideal for multiplexing low skew clock or other skew sensitive signals. Multiple V_{BB} pins are provided to ease AC coupling of input signals. If used, the V_{BB} output should be bypassed to ground with a $0.01\mu F$ capacitor.

The device features both individual and common select inputs to address both data path and random logic applications.

- 350ps Typical Propagation Delays
- Typical Frequency 3.0GHz
- 20-Lead TSSOP Package
- PECL mode: 3.0V to 5.5V V_{CC} with $V_{EE} = 0V$
- ECL mode: $0V V_{CC}$ with $V_{EE} = -3.0V$ to -5.5V
- Separate and Common Select
- Internal Input Resistors: Pulldown on D, \overline{D}
- Q Output will default LOW with inputs open or at VEE
- ESD Protection: >4KV HBM, >200V MM
- VBB Outputs
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack.
 For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 140 devices

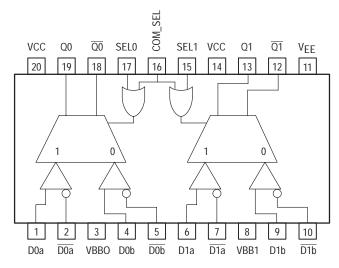


Figure 1. 20-Lead TSSOP (Top View) and Logic Diagram

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TSSOP-20 DT SUFFIX CASE 948E

MARKING DIAGRAM*

MC10 EP56 ALYW

A = Assembly Location

L = Wafer Lot

Y = Year W = Work Week

*For additional information, see Application Note AND8002/D

PIN DESCRIPTION								
PIN	FUNCTION							
D0a-D1a	ECL Input Data a							
D0a-D1a	ECL Input Data a Invert							
D0b-D1b	ECL Input Data b							
D0b-D1b	ECL Input Data b Invert							
SEL0-SEL1	ECL Indiv. Select Input							
COM_SEL	ECL Common Select Input							
V _{BB0} , V _{BB1}	Output Reference Voltage							
Q0-Q1	ECL True Outputs							
Q0-Q1	ECL Inverted Outputs							
VCC	Positive Supply							
VEE	Negative, 0 Supply							

TRUTH TABLE

SEL0	SEL1	COM_SEL	Q0, Q0	Q1, Q1
Х	Х	Н	а	а
L	L	L	b	b
L	Н	L	b	а
Н	Н	L	а	а
Н	L	L	а	b

ORDERING INFORMATION

Device	Package	Shipping				
MC10EP56DT	TSSOP	75 Units/Rail				
MC10EP56DTR2	TSSOP	2500 Tape & Reel				

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
VEE	Power Supply (V _{CC} = 0V)	-6.0 to 0	VDC
Vcc	Power Supply (V _{EE} = 0V)	6.0 to 0	VDC
V _I	Input Voltage ($V_{CC} = 0V$, V_I not more negative than V_{EE})	-6.0 to 0	VDC
VI	Input Voltage (VEE = 0V, VI not more positive than VCC)	6.0 to 0	VDC
lout	Output Current Continuous Surge		mA
I _{BB}	V _{BB} Sink/Source Current†	± 0.5	mA
TA	Operating Temperature Range	-40 to +85	°C
T _{stg}	Storage Temperature	−65 to +150	°C
θЈΑ	Thermal Resistance (Junction–to–Ambient) Still Air 500lfpm	•	°C/W
θJC	Thermal Resistance (Junction-to-Case)	23 to 41 ± 5%	°C/W
T _{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

^{*} Maximum Ratings are those values beyond which damage to the device may occur.

DC CHARACTERISTICS, ECL/LVECL ($V_{CC} = 0V$; $V_{EE} = -5.5V$ to -3.0V) (Note 4.)

			-40°C 25°C								
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
IEE	Power Supply Current (Note 1.)	50	65	88	50	65	88	50	65	88	mA
VOH	Output HIGH Voltage (Note 2.)	-1135	-1060	-885	-1070	-945	-820	-1010	-885	-760	mV
VOL	Output LOW Voltage (Note 2.)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
VIH	Input HIGH Voltage Single Ended	-1210		-885	-1145		-820	-1085		-760	mV
V _{IL}	Input LOW Voltage Single Ended	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{BB}	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 3.)	VEE	+2.0	0.0	VEE	+2.0	0.0	VEE	+2.0	0.0	V
ΊΗ	Input HIGH Current			150			150			150	μΑ
IIL	Input LOW Current SEL, COM_SEL, D D	0.5 -150			0.5 -150			0.5 -150			μΑ

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.

2. All loading with 50 ohms to V_{CC}-2.0 volts.

3. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.

4. Input and output parameters vary 1:1 with V_{CC}.

[†] Use for inputs of same package only.

DC CHARACTERISTICS, LVPECL ($V_{CC} = 3.3V \pm 0.3V$, $V_{EE} = 0V$) (Note 8.)

		Î	–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
IEE	Power Supply Current (Note 5.)	50	65	88	50	65	88	50	65	88	mA
VOH	Output HIGH Voltage (Note 6.)	2165	2240	2415	2230	2355	2480	2290	2415	2540	mV
VOL	Output LOW Voltage (Note 6.)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
VIH	Input HIGH Voltage Single Ended	2090		2415	2155		2480	2215		2540	mV
VIL	Input LOW Voltage Single Ended	1365		1690	1430		1755	1490		1815	mV
V _{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 7.)	2.0		3.3	2.0		3.3	2.0		3.3	V
lн	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current SEL, COM_SEL, D D	0.5 -150			0.5 -150			0.5 -150			μА

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

- 5. $V_{CC} = 3.3V$, $V_{EE} = 0V$, all other pins floating.
- 6. All loading with 50 ohms to V_{CC}-2.0 volts.
 7. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
- 8. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, PECL ($V_{CC} = 5.0V \pm 0.5V$, $V_{EE} = 0V$) (Note 12.)

			–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
IEE	Power Supply Current (Note 9.)	50	65	88	50	65	88	50	65	88	mA
Vон	Output HIGH Voltage (Note 10.)	3865	3940	4115	3930	4055	4180	3990	4115	4240	mV
V _{OL}	Output LOW Voltage (Note 10.)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
VIH	Input HIGH Voltage Single Ended	3790		4115	3855		4180	3915		4240	mV
V _{IL}	Input LOW Voltage Single Ended	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Note 11.)	2.0		5.0	2.0		5.0	2.0		5.0	V
lн	Input HIGH Current			150			150			150	μΑ
I _{IL}	Input LOW Current SEL, COM_SEL, D D	0.5 -150			0.5 -150			0.5 -150			μА

NOTE: 10EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

- 9. V_{CC} = 5.0V, V_{EE} = 0V, all other pins floating. 10. All loading with 50 ohms to V_{CC} -2.0 volts.
- 11. V_{IHCMR} min varies 1:1 with V_{EE} , max varies 1:1 with V_{CC} .
- 12. Input and output parameters vary 1:1 with V_{CC}.

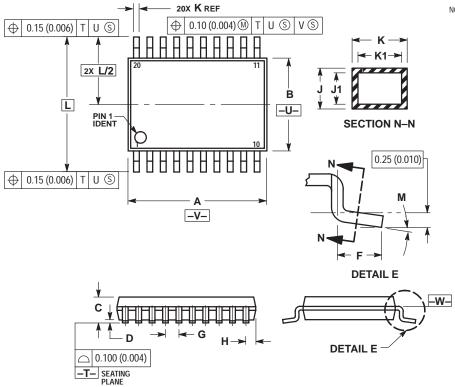
AC CHARACTERISTICS ($V_{CC} = 0V$; $V_{EE} = -3.0V$ to -5.5V) or ($V_{CC} = 3.0V$ to 5.5V; $V_{EE} = 0V$)

	1										i —
			–40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Toggle Frequency (Note 13.)					3.0					GHz
tPLH, ^t PHL	Propagation Delay to Output Differential $\begin{array}{c} \text{D->Q,} \ \overline{\mathbf{Q}} \ \ (\text{Diff}) \\ \text{D->Q,} \ \overline{\mathbf{Q}} \ \ (\text{SE}) \\ \text{SEL->Q,} \ \overline{\mathbf{Q}} \\ \text{COM_SEL->Q,} \ \overline{\mathbf{Q}} \end{array}$	250 250 200 200	340 340 340 350	480 480 550 580	250 250 200 200	360 360 340 360	480 480 550 580	300 300 200 200	400 400 390 400	520 520 650 675	ps
tSKEW	Within–Device Skew (Note 14.) Duty Cycle Skew (Note 15.)		TBD TBD			TBD TBD			TBD TBD		ps
^t JITTER	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
VPP	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t _r	Output Rise/Fall Times Q, Q (20% – 80%)	100	150	200	100	150	200	100	160	220	ps

^{13.} F_{max} guaranteed for functionality only.
14. Within–Device Skew is defined as identical transitions on similar paths through a device.
15. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

PACKAGE DIMENSIONS

TSSOP-20 **DT SUFFIX** 20 PIN PLASTIC TSSOP PACKAGE CASE 948E-02 **ISSUE A**



- 11ES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED
- 1.15 (0.006) PER SIDE.

 1.006) PER SIDE.

 1. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT
- INTERLEAD FLASH OR PROTRUSION SHALL NOT
 EXCEED 0.25 (0.010) PER SIDE.

 5. DIMENSION K DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION. SHALL BE 0.08 (0.03) TOTAL IN
 EXCESS OF THE K DIMENSION AT MAXIMUM
 MATERIAL CONDITION.

 6. TERMINAL NUMBERS ARE SHOWN FOR
 REFERENCE ONLY.

 7. DIMENSION A AND B ARE TO BE
 DETERMINED AT DATIM PI ANF -W-
- DETERMINED AT DATUM PLANE -W-

	MILLIN	IETERS	INC	HES						
DIM	MIN	MAX	MIN	MAX						
Α	6.40	6.60	0.252	0.260						
В	4.30	4.50	0.169	0.177						
С		1.20		0.047						
D	0.05	0.15	0.002	0.006						
F	0.50	0.75	0.020	0.030						
G	0.65	BSC	0.026 BSC							
Н	0.27	0.37	0.011	0.015						
J	0.09	0.20	0.004	0.008						
J1	0.09	0.16	0.004	0.006						
K	0.19	0.30	0.007	0.012						
K1	0.19	0.25	0.007	0.010						
L	6.40		0.252 BSC							
M	0°	8°	0 °	8°						

Notes

Notes

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