

MC74HCT245A

Octal 3-State Noninverting Bus Transceiver with LSTTL Compatible Inputs

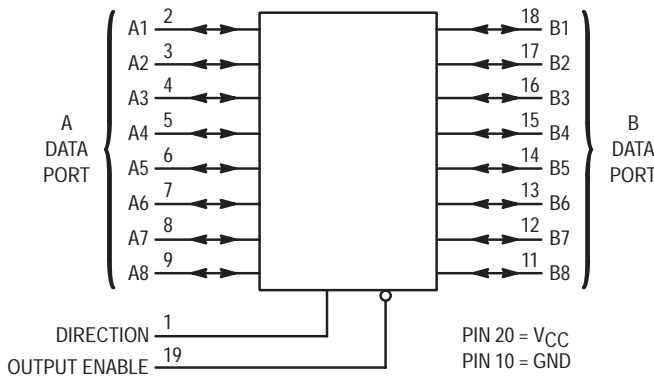
High-Performance Silicon-Gate CMOS

The MC74HCT245A is identical in pinout to the LS245. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

The MC74HCT245A is a 3-state noninverting transceiver that is used for 2-way asynchronous communication between data buses. The device has an active-low Output Enable pin, which is used to place the I/O ports into high-impedance states. The Direction control determines whether data flows from A to B or from B to A.

- Output Drive Capability: 15 LSTTL Loads
- TTL/NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μ A
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 304 FETs or 76 Equivalent Gates

LOGIC DIAGRAM



| Design Criteria | Value | Units |
|---------------------------------|-------|---------|
| Internal Gate Count* | 76 | ea |
| Internal Gate Propagation Delay | 1.0 | ns |
| Internal Gate Power Dissipation | 5.0 | μ W |
| Speed Power Product | 0.005 | pJ |

*Equivalent to a two-input NAND gate.

FUNCTION TABLE

| Control Inputs | | Operation |
|----------------|-----------|---------------------------------------|
| Output Enable | Direction | |
| L | L | Data Transmitted from Bus B to Bus A |
| L | H | Data Transmitted from Bus A to Bus B |
| H | X | Buses Isolated (High-Impedance State) |

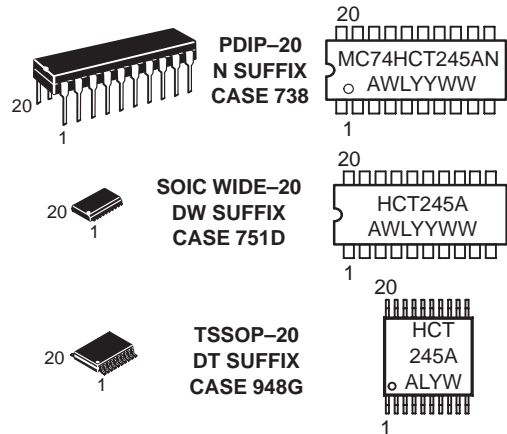
X = Don't Care



ON Semiconductor

<http://onsemi.com>

MARKING DIAGRAMS



A = Assembly Location
 WL = Wafer Lot
 YY = Year
 WW = Work Week

PIN ASSIGNMENT

| DIRECTION | 1 | 20 | |
|-----------|----|----|-----------------|
| | • | | V _{CC} |
| A1 | 2 | 19 | OUTPUT ENABLE |
| A2 | 3 | 18 | B1 |
| A3 | 4 | 17 | B2 |
| A4 | 5 | 16 | B3 |
| A5 | 6 | 15 | B4 |
| A6 | 7 | 14 | B5 |
| A7 | 8 | 13 | B6 |
| A8 | 9 | 12 | B7 |
| GND | 10 | 11 | B8 |

ORDERING INFORMATION

| Device | Package | Shipping |
|-----------------|-----------|-------------|
| MC74HCT245AN | PDIP-20 | 1440 / Box |
| MC74HCT245ADW | SOIC-WIDE | 38 / Rail |
| MC74HCT245ADWR2 | SOIC-WIDE | 1000 / Reel |
| MC74HCT245ADT | TSSOP-20 | 75 / Rail |
| MC74HCT245ADTR2 | TSSOP-20 | 2500 / Reel |

MC74HCT245A

MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|-----------|---|-------------------------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | - 0.5 to + 7.0 | V |
| V_{in} | DC Input Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| V_{out} | DC Output Voltage (Referenced to GND) | - 0.5 to $V_{CC} + 0.5$ | V |
| I_{in} | DC Input Current, per Pin | ± 20 | mA |
| I_{out} | DC Output Current, per Pin | ± 35 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 75 | mA |
| P_D | Power Dissipation in Still Air, Plastic DIP† SOIC Package† TSSOP Package† | 750 | mW |
| | | 500 | |
| | | 450 | |
| T_{stg} | Storage Temperature | - 65 to + 150 | °C |
| T_L | Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP, SOIC, SSOP or TSSOP Package) | 260 | °C |

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

*Maximum Ratings are those values beyond which damage to the device may occur.

Functional operation should be restricted to the Recommended Operating Conditions.

†Derating — Plastic DIP: - 10 mW/°C from 65° to 125°C

SOIC Package: - 7 mW/°C from 65° to 125°C

TSSOP Package: - 6.1 mW/°C from 65° to 125°C

For high frequency or heavy load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|-------------------|--|------|----------|------|
| V_{CC} | DC Supply Voltage (Referenced to GND) | 4.5 | 5.5 | V |
| V_{in}, V_{out} | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | V_{CC} | V |
| T_A | Operating Temperature, All Package Types | - 55 | + 125 | °C |
| t_r, t_f | Input Rise and Fall Time (Figure 1) | 0 | 500 | ns |

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | V_{CC} V | Guaranteed Limit | | | Unit |
|-----------------|--|---|---------------|--------------------------|--|--------------------------|---------------|
| | | | | - 55 to 25°C | $\leq 85^\circ\text{C}$ | $\leq 125^\circ\text{C}$ | |
| V_{IH} | Minimum High-Level Input Voltage | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 4.5 | 2.0 | 2.0 | 2.0 | V |
| | | | 5.5 | 2.0 | 2.0 | 2.0 | |
| V_{IL} | Maximum Low-Level Input Voltage | $V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \leq 20 \mu\text{A}$ | 4.5 | 0.8 | 0.8 | 0.8 | V |
| | | | 5.5 | 0.8 | 0.8 | 0.8 | |
| V_{OH} | Minimum High-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$ | 4.5 | 4.4 | 4.4 | 4.4 | V |
| | | | 5.5 | 5.4 | 5.4 | 5.4 | |
| V_{OL} | Maximum Low-Level Output Voltage | $V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \leq 20 \mu\text{A}$ | 4.5 | 0.1 | 0.1 | 0.1 | V |
| | | | 5.5 | 0.1 | 0.1 | 0.1 | |
| I_{in} | Maximum Input Leakage Current | $V_{in} = V_{CC} \text{ or } GND, \text{ Pins } 1 \text{ or } 19$ | 4.5 | 0.26 | 0.33 | 0.4 | μA |
| | | | 5.5 | ± 0.1 | ± 1.0 | ± 1.0 | |
| I_{CC} | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC} \text{ or } GND$ $I_{out} = 0 \mu\text{A}$ | 5.5 | 4.0 | 40 | 160 | μA |
| I_{OZ} | Maximum Three-State Leakage Current | Output in High-Impedance State $V_{in} = V_{IL} \text{ or } V_{IH}$ $V_{out} = V_{CC} \text{ or } GND, \text{ I/O Pins}$ | 5.5 | ± 0.5 | ± 5.0 | ± 10 | μA |
| ΔI_{CC} | Additional Quiescent Supply Current | $V_{in} = 2.4 \text{ V, Any One Input}$ $V_{in} = V_{CC} \text{ or } GND, \text{ Other Inputs}$ $I_{out} = 0 \mu\text{A}$ | 5.5 | $\geq -55^\circ\text{C}$ | $25^\circ\text{C to } 125^\circ\text{C}$ | | mA |
| | | | | | 2.9 | 2.4 | |

NOTE: Information on typical parametric values can be found in Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

MC74HCT245A

AC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0\text{ V} \pm 10\%$, $C_L = 50\text{ pF}$, Input $t_r = t_f = 6.0\text{ ns}$)

| Symbol | Parameter | Guaranteed Limit | | | Unit |
|--|--|------------------|--------|---------|------|
| | | - 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| t _{PLH} , t _{PHL} | Maximum Propagation Delay, A to B or B to A (Figures 1 and 3) | 22 | 28 | 33 | ns |
| t _{PLZ} , t _{PHZ} | Maximum Propagation Delay, Direction or Output Enable to A or B (Figures 2 and 4) | 30 | 36 | 42 | ns |
| t _{PZL} , t _{PZH} | Maximum Propagation Delay, Output Enable to A or B (Figures 2 and 4) | 30 | 36 | 42 | ns |
| t _{TLH} , t _{THL} | Maximum Output Transition Time, any Output (Figures 1 and 3) | 12 | 15 | 18 | ns |
| C _{in} | Maximum Input Capacitance (Pin 1 or 19) | 10 | 10 | 10 | pF |
| C _{out} | Maximum Three-State I/O Capacitance, (I/O in High-Impedance State) | 15 | 15 | 15 | pF |

NOTE: For propagation delays with loads other than 50 pF, and information on typical parametric values, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

| C _{PD} | Power Dissipation Capacitance (Per Enabled Output)* | Typical @ 25°C, V _{CC} = 5.0 V | pF |
|-----------------|---|---|----|
| | | 97 | |

* Used to determine the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the ON Semiconductor High-Speed CMOS Data Book (DL129/D).

MC74HCT245A

SWITCHING WAVEFORMS

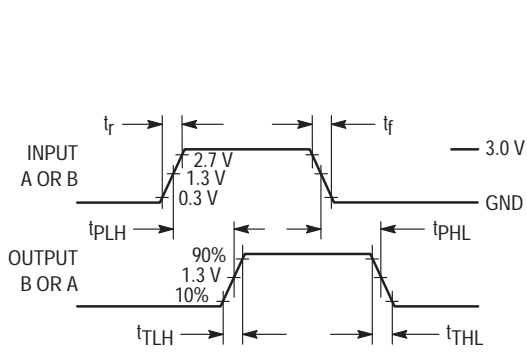


Figure 1.

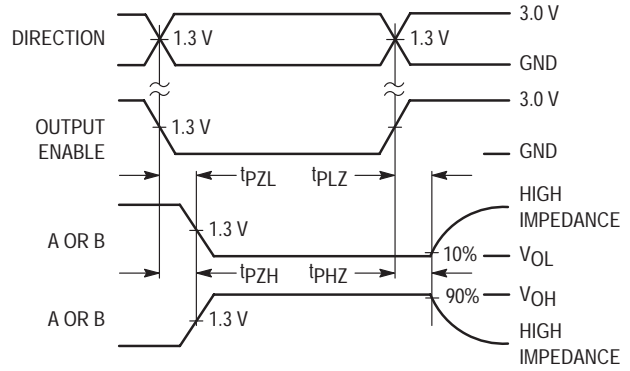
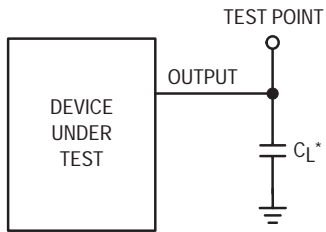
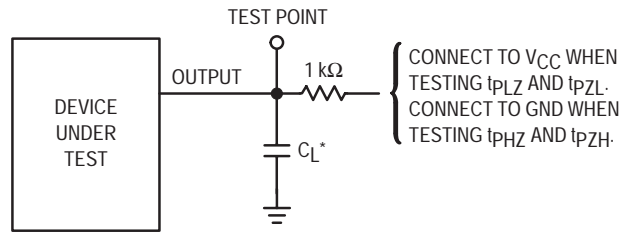


Figure 2.



*Includes all probe and jig capacitance

Figure 3.

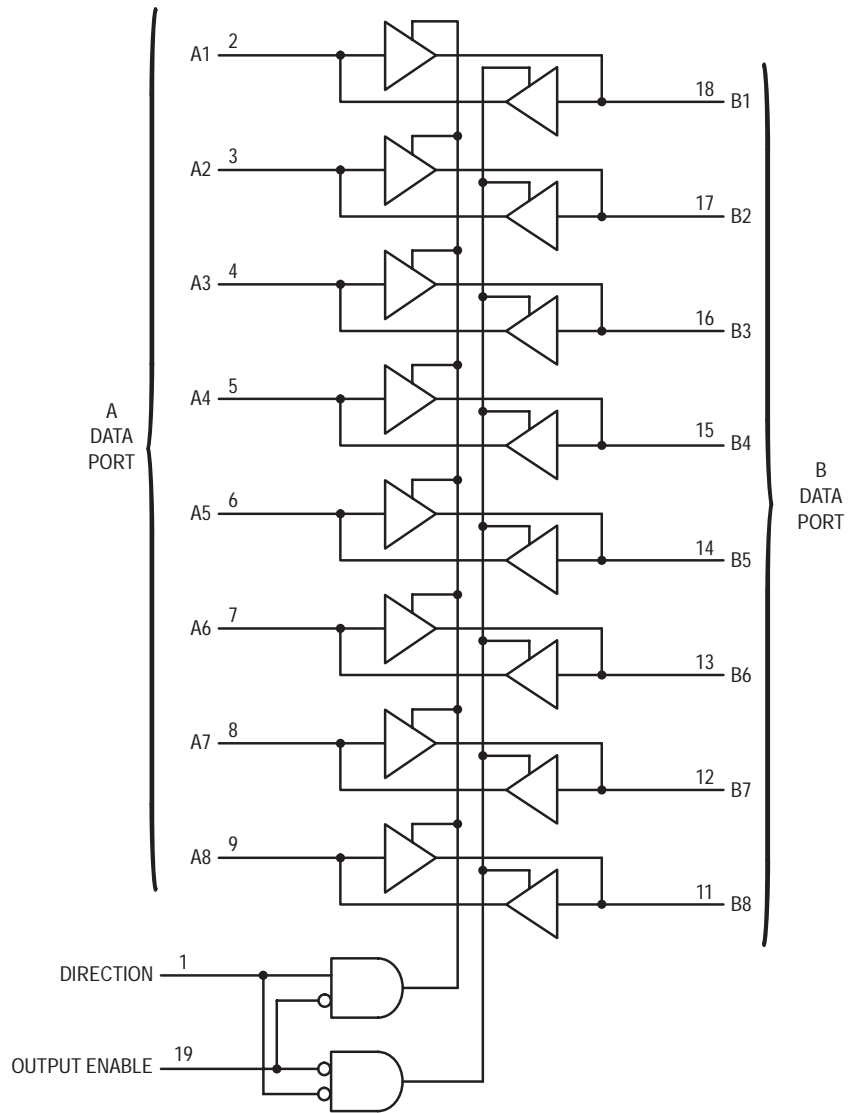


*Includes all probe and jig capacitance

Figure 4. Test Circuit

MC74HCT245A

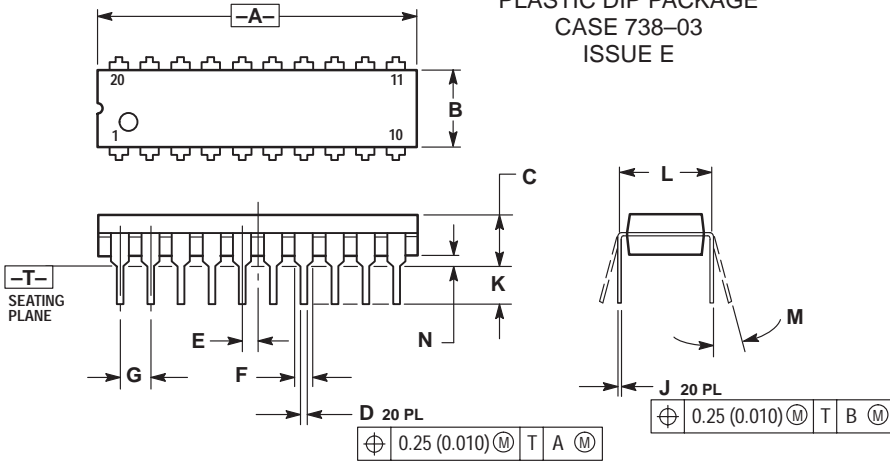
EXPANDED LOGIC DIAGRAM



MC74HCT245A

PACKAGE DIMENSIONS

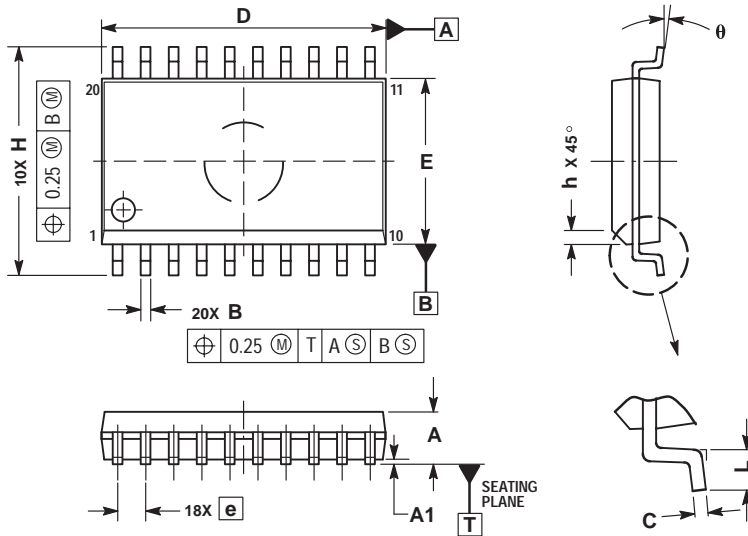
**PDIP-20
N SUFFIX**
PLASTIC DIP PACKAGE
CASE 738-03
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
 4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 1.010 | 1.070 | 25.66 | 27.17 |
| B | 0.240 | 0.260 | 6.10 | 6.60 |
| C | 0.150 | 0.180 | 3.81 | 4.57 |
| D | 0.015 | 0.022 | 0.39 | 0.55 |
| E | 0.050 BSC | | 1.27 BSC | |
| F | 0.050 | 0.070 | 1.27 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.140 | 2.80 | 3.55 |
| L | 0.300 BSC | | 7.62 BSC | |
| M | 0° | 15° | 0° | 15° |
| N | 0.020 | 0.040 | 0.51 | 1.01 |

**SO-20
DW SUFFIX**
CASE 751D-05
ISSUE F



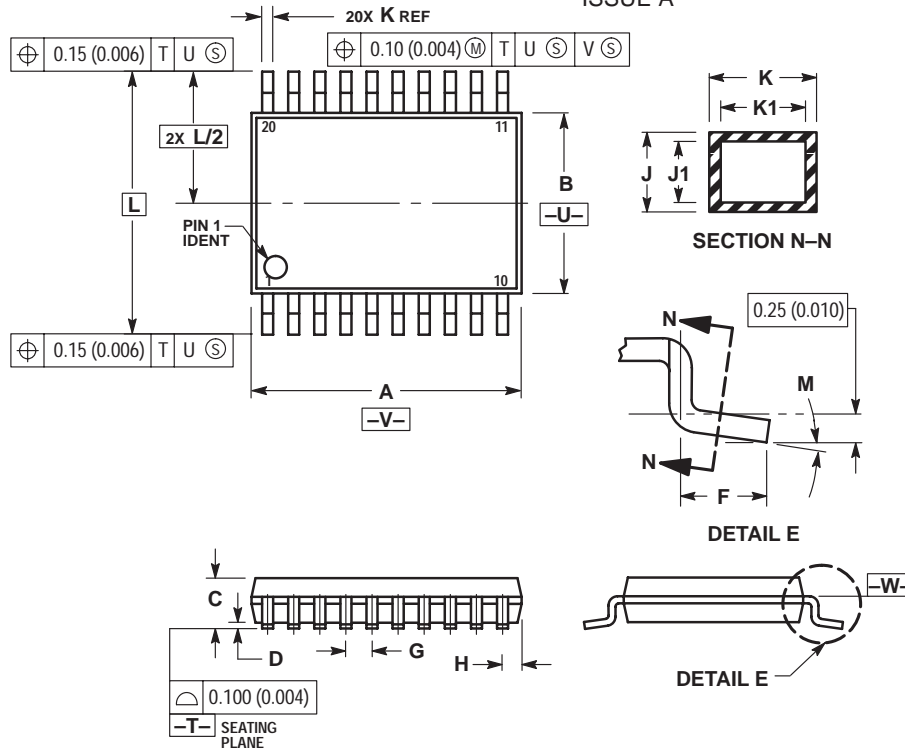
- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | |
|-------|-------------|-------|
| | MIN | MAX |
| A | 2.35 | 2.65 |
| A1 | 0.10 | 0.25 |
| B | 0.35 | 0.49 |
| C | 0.23 | 0.32 |
| D | 12.65 | 12.95 |
| E | 7.40 | 7.60 |
| e | 1.27 BSC | |
| H | 10.05 | 10.55 |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| theta | 0° | 7° |

MC74HCT245A

PACKAGE DIMENSIONS

TSSOP-20
DT SUFFIX
CASE 948E-02
ISSUE A




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 6.40 | 6.60 | 0.252 | 0.260 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | — | 1.20 | — | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.27 | 0.37 | 0.011 | 0.015 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

MC74HCT245A

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