

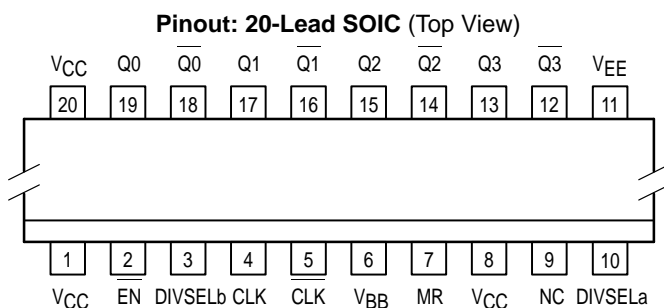
## ÷2/4, ÷4/6 Clock Generation Chip

The MC100LVEL39 is a low skew ÷2/4, ÷4/6 clock generation chip designed explicitly for low skew clock generation applications. The MC100EL39 is pin and functionally equivalent to the MC100LVEL39 but is specified for operation at the standard 100K ECL voltage supply. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The device can be driven by either a differential or single-ended LVECL or, if positive power supplies are used, LVPECL input signal. In addition, by using the  $V_{BB}$  output, a sinusoidal source can be AC coupled into the device (see Interfacing section of the ECLinPS™ Data Book DL140/D). If a single-ended input is to be used, the  $V_{BB}$  output should be connected to the CLK input and bypassed to ground via a 0.01µF capacitor. The  $V_{BB}$  output is designed to act as the switching reference for the input of the LVEL39 under single-ended input conditions, as a result, this pin can only source/sink up to 0.5mA of current.

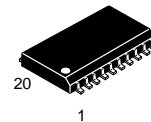
The common enable ( $\overline{EN}$ ) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

Upon startup, the internal flip-flops will attain a random state; therefore, for systems which utilize multiple LVEL39s, the master reset (MR) input must be asserted to ensure synchronization. For systems which only use one LVEL39, the MR pin need not be exercised as the internal divider design ensures synchronization between the ÷2/4 and the ÷4/6 outputs of a single device.

- 50ps Output-to-Output Skew
- Synchronous Enable/Disable
- Master Reset for Synchronization
- 75kΩ Internal Input Pulldown Resistors
- >2000V ESD Protection
- Low Voltage  $V_{EE}$  Range of -3.0 to -3.8V



## MC100LVEL39 MC100EL39



**DW SUFFIX**  
PLASTIC SOIC PACKAGE  
CASE 751D-04

### PIN DESCRIPTION

PIN	FUNCTION
CLK	Diff Clock Inputs
EN	Sync Enable
MR	Master Reset
$V_{BB}$	Reference Output
Q <sub>0</sub> , Q <sub>1</sub>	Diff ÷2/4 Outputs
Q <sub>2</sub> , Q <sub>3</sub>	Diff ÷4/6 Outputs
DIVSEL	Frequency Select Input

### FUNCTION TABLE

CLK	$\overline{EN}$	MR	FUNCTION
Z	L	L	Divide
ZZ	H	L	Hold Q <sub>0-3</sub>
X	X	H	Reset Q <sub>0-3</sub>

Z = Low-to-High Transition  
ZZ = High-to-Low Transition

DIVSEL <sub>a</sub>	Q <sub>0</sub> , Q <sub>1</sub> OUTPUTS
0	Divide by 2
1	Divide by 4
DIVSEL <sub>b</sub>	Q <sub>2</sub> , Q <sub>3</sub> OUTPUTS
0	Divide by 4
1	Divide by 6



MC100LVEL39 MC100EL39

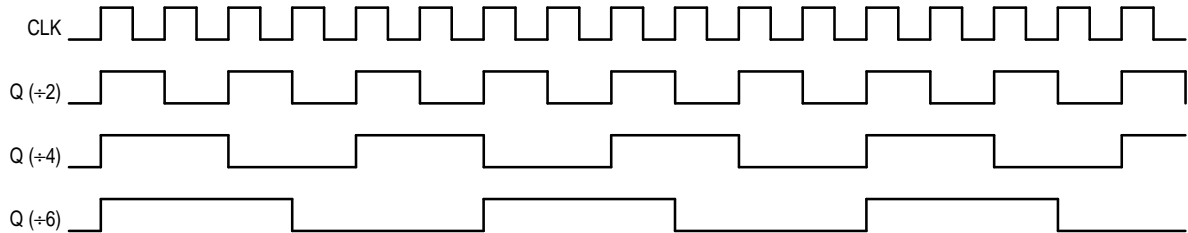
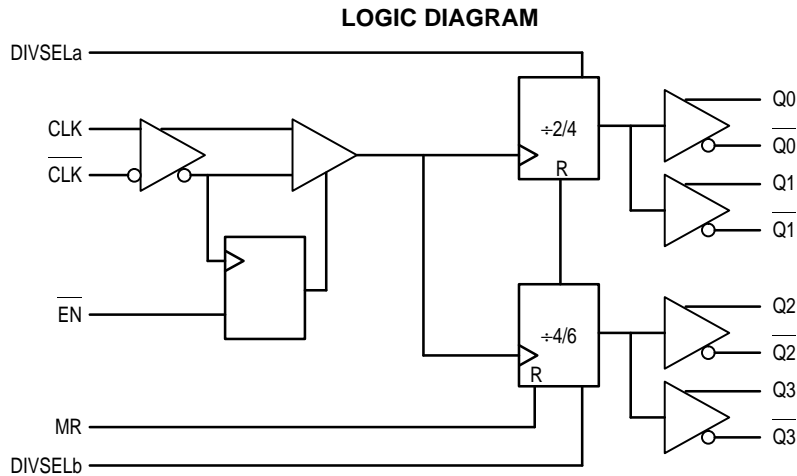


Figure 1. Timing Diagrams

**MC100LVEL39**

**DC CHARACTERISTICS** ( $V_{EE} = -3.8V$  to  $-3.0$ ;  $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		50	59		50	59		50	59		54	61	mA
$V_{BB}$	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$I_{IH}$	Input High Current			150			150			150			150	$\mu A$

**MC100LVEL39**

**AC CHARACTERISTICS** ( $V_{EE} = -3.8V$  to  $-3.0$ ;  $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency	1000			1000			1000			1000			MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay to Output	760 710 600		960 1010 900	780 730 600		980 1030 900	800 750 610		1000 1050 910	850 800 630		1050 1100 930	ps
$t_{SKEW}$	Within-Device Skew <sup>1</sup>			50			50			50			50	ps
	Part-to-Part			200			200			200			200	
$t_S$	Setup Time	EN $\rightarrow$ CLK	250		250		250		250		250		250	ps
		DIVSEL $\rightarrow$ CLK	400		400		400		400		400		400	
$t_H$	Hold Time	CLK $\rightarrow$ EN	100		100		100		100		100		100	ps
		CLK $\rightarrow$ Div_Sel	150		150		150		150		150		150	

**MC100LVEL39** (continued)**AC CHARACTERISTICS** ( $V_{EE} = -3.8V$  to  $-3.0$ ;  $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{PP}$	Minimum Input Swing CLK	250			250			250			250			mV
$V_{CMR}$	Common Mode Range <sup>3</sup> $V_{PP} < 500mV$ $V_{PP} \geq 500mV$	-2.0 -1.8		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	-2.1 -1.9		-0.4 -0.4	V
$t_{RR}$	Reset Recovery Time			100			100			100			100	ps
$t_{PW}$	Minimum Pulse Width CLK MR	500 700			500 700			500 700			500 700			ps
$t_r, t_f$	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	280		550	ps

- Skew is measured between outputs under identical transitions.
- Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1V. The lower end of the CMR range varies 1:1 with  $V_{EE}$ . The numbers in the spec table assume a nominal  $V_{EE} = -3.3V$ . Note for PECL operation, the  $V_{CMR(min)}$  will be fixed at  $3.3V - |V_{CMR(min)}|$ .

**MC100EL39****DC CHARACTERISTICS** ( $V_{EE} = -4.2V$  to  $-5.46$ ;  $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current		50	59		50	59		50	59		54	61	mA
$V_{BB}$	Output Reference Voltage	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	-1.38		-1.26	V
$I_{IH}$	Input High Current			150			150			150			150	$\mu A$

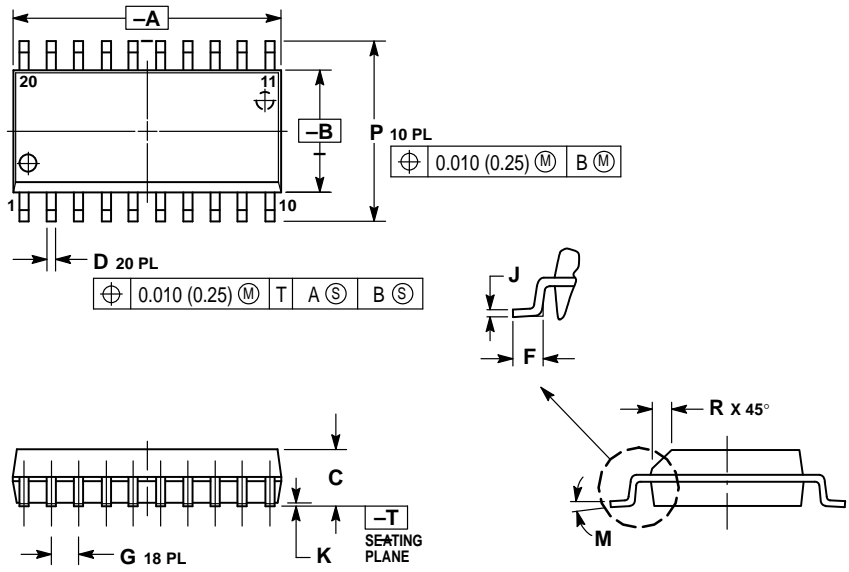
**MC100EL39****AC CHARACTERISTICS** ( $V_{EE} = -4.2V$  to  $-5.46$ ;  $V_{CC} = GND$ )

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{MAX}$	Maximum Toggle Frequency	1000			1000			1000			1000			MHz
$t_{PLH}$ $t_{PHL}$	Propagation Delay CLK → Q (Diff) to Output CLK → Q (S.E.) MR → Q	760 710 600		960 1010 900	780 730 600		980 1030 900	800 750 610		1000 1050 910	850 800 630		1050 1100 930	ps
$t_{SKEW}$	Within-Device Skew <sup>1</sup> $Q_0 - Q_3$ Part-to-Part $Q_0 - Q_3$ (Diff)			50			50			50			50	ps
$t_S$	Setup Time EN → CLK DIVSEL → CLK	250 400			250 400			250 400			250 400			ps
$t_H$	Hold Time CLK → EN CLK → Div_Sel	100 150			100 150			100 150			100 150			ps
$V_{PP}$	Minimum Input Swing CLK	250			250			250			250			mV
$V_{CMR}$	Common Mode Range <sup>3</sup> $V_{PP} < 500mV$ $V_{PP} \geq 500mV$	-3.2 -3.0		-0.4 -0.4	-3.3 -3.1		-0.4 -0.4	-3.3 -3.1		-0.4 -0.4	-3.3 -3.1		-0.4 -0.4	V
$t_{RR}$	Reset Recovery Time			100			100			100			100	ps
$t_{PW}$	Minimum Pulse Width CLK MR	500 700			500 700			500 700			500 700			ps
$t_r, t_f$	Output Rise/Fall Times Q (20% – 80%)	280		550	280		550	280		550	280		550	ps

- Skew is measured between outputs under identical transitions.
- Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between  $V_{ppmin}$  and 1V. The lower end of the CMR range varies 1:1 with  $V_{EE}$ . The numbers in the spec table assume a nominal  $V_{EE} = -4.5V$ . Note for PECL operation, the  $V_{CMR(min)}$  will be fixed at  $5.0V - |V_{CMR(min)}|$ .

OUTLINE DIMENSIONS

DW SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751D-04  
ISSUE E



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
  5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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