

# MC100EPT21

## Differential LVPECL to LVTTTL Translator

The MC100EPT21 is a Differential LVPECL to LVTTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3V and ground are required. The small outline 8-lead SOIC package makes the EPT21 ideal for applications which require the translation of a clock or data signal.

The VBB output allows the EPT21 to also be used in a single-ended input mode. In this mode the VBB output is tied to the  $\overline{D0}$  input for a non-inverting buffer or the D0 input for an inverting buffer. If used, the VBB pin should be bypassed to ground via a 0.01 $\mu$ F capacitor.

- 1.4ns Typical Propagation Delay
- 275MHz Fmax (Clock bit stream, not pseudo-random)
- Differential LVPECL inputs
- Small Outline SOIC Package
- 24mA TTL outputs
- Flow Through Pinouts
- Internal Input Resistors: Pulldown on D, Pulldown and Pullup on  $\overline{D}$
- Q Output will default LOW with inputs open or at GND
- ESD Protection: >1500V HBM, >100V MM
- VBB Output
- New Differential Input Common Mode Range
- Moisture Sensitivity Level 1, Indefinite Time Out of Drypack.  
For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL-94 code V-0 @ 1/8",  
Oxygen Index 28 to 34
- Transistor Count = 81 devices

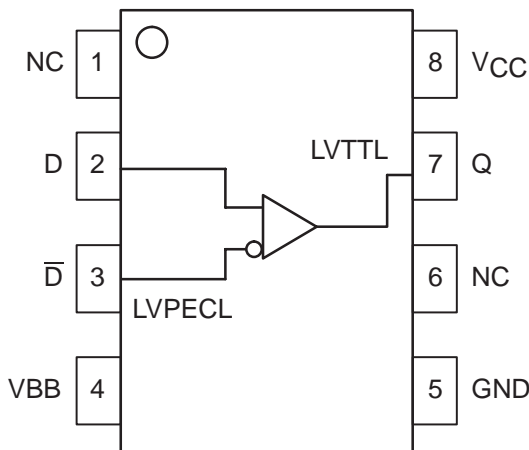
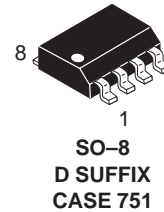


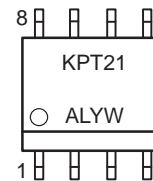
Figure 1. 8-Lead Pinout (Top View) and Logic Diagram



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### MARKING DIAGRAM



A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional information, see Application Note AND8002/D

PIN DESCRIPTION	
PIN	FUNCTION
Q	LVTTTL Output
D, $\overline{D}$	Differential LVPECL Input Pair
VCC	Positive Supply
VBB	Output Reference Voltage
GND	Ground

### ORDERING INFORMATION

Device	Package	Shipping
MC100EPT21D	SOIC	98 Units/Rail
MC100EPT21DR2	SOIC	2500 Tape & Reel

# MC100EPT21

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	Power Supply (GND = 0V)	0 to 3.8	VDC
V <sub>I</sub>	Input Voltage (GND = 0V, V <sub>I</sub> not more positive than V <sub>CC</sub> )	0 to 3.8	VDC
I <sub>out</sub>	Output Current Continuous Surge	50 100	mA
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source Current†	± 0.5	mA
T <sub>A</sub>	Operating Temperature Range	-40 to +85	°C
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient) Still Air 500lfpm	190 130	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	41 to 44 ± 5%	°C/W
T <sub>sol</sub>	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

\* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

## DC CHARACTERISTICS (V<sub>CC</sub> = 3.3V ± 0.3V; GND = 0V; T<sub>A</sub> = -40°C to 85°C)

Symbol	Characteristic	Min	Typ	Max	Unit
I <sub>CCH</sub>	Power Supply Current (Outputs set to HIGH)	5.0	12	20	mA
I <sub>CCL</sub>	Power Supply Current (Outputs set to LOW)	8.0	18	26	mA
V <sub>IH</sub>	Input HIGH Voltage (V <sub>CC</sub> = 3.3) (Note 1.)	2135		2420	mV
V <sub>IL</sub>	Input LOW Voltage (V <sub>CC</sub> = 3.3) (Note 1.)	1490		1825	mV
I <sub>IH</sub>	Input HIGH Current			150	μA
I <sub>IL</sub>	Input LOW Current	$\frac{D}{D}$ -150		0.5	μA
V <sub>OH</sub>	Output HIGH Voltage (I <sub>OH</sub> = -3.0mA) (Note 2.)	2.4			V
V <sub>OL</sub>	Output LOW Voltage (I <sub>OL</sub> = 24mA) (Note 2.)			0.5	V
I <sub>OS</sub>	Output Short Circuit Current	-130		-80	mA
V <sub>IHCMR</sub>	Input HIGH Voltage Common Mode Range (Note 3.)	2.0		3.3	V
V <sub>BB</sub>	Output Voltage Reference		2.0		V

NOTE: 100EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

1. All values vary 1:1 with V<sub>CC</sub>.
2. All loading with 500 ohms to GND, CL = 20pF.
3. V<sub>IHCMR</sub> min varies 1:1 with GND, max varies 1:1 with V<sub>CC</sub>.

## AC CHARACTERISTICS (V<sub>CC</sub> = 3.3V ± 0.3V; GND = 0V)

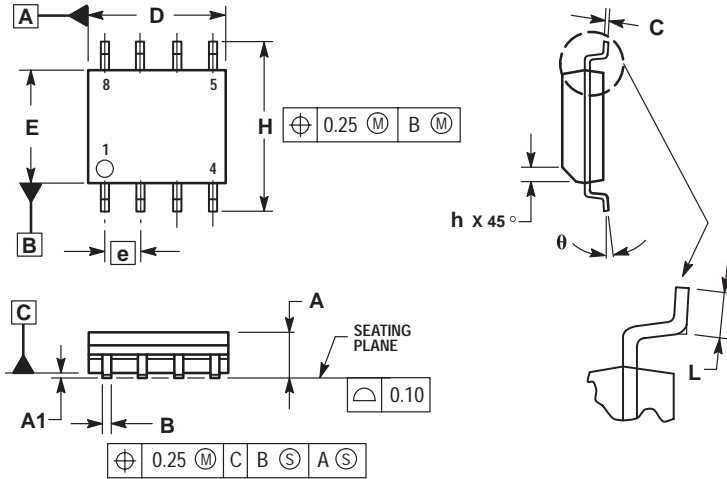
Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f <sub>max</sub>	Maximum Toggle Frequency (Note 4.)	275	350		275	350		275	350		MHz
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay to Output Differential	1000	1450	1800	1000	1450	1800	1000	1450	1900	ps
t <sub>SK++</sub> , t <sub>SK--</sub> , t <sub>SKPP</sub>	Output-to-Output Skew++ Output-to-Output Skew-- Part-to-Part Skew (Note 5.)		60 25 500			60 25 500			60 25 500		ps
t <sub>JITTER</sub>	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps
V <sub>PP</sub>	Input Voltage Swing (Diff.)	150	800	1200	150	800	1200	150	800	1200	mV
t <sub>r</sub> , t <sub>f</sub>	Output Rise/Fall Times (0.8V – 2.0V) Q, $\bar{Q}$	330	500	900	330	500	900	330	500	900	ps

4. F<sub>max</sub> guaranteed for functionality only. V<sub>OL</sub> and V<sub>OH</sub> levels are guaranteed at DC only.
5. Skews are measured between outputs under identical transitions.

# MC100EPT21

## PACKAGE DIMENSIONS


SO-8  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-06  
ISSUE T



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
$\theta$	0°	7°

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