MC100LVEP111

Low-Voltage 1:10 Differential LVECL/LVPECL/LVEPECL/HSTL Clock Driver

The MC100LVEP111 is a low skew 1–to–10 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The LVECL/LVPECL input signals can be either differential or single–ended (if the V_{BB} output is used). HSTL inputs can be used when the LVEP111 is operating under LVPECL conditions.

The LVEP111 specifically guarantees low output–to–output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into 50Ω even if only one side is being used. When fewer than all ten pairs are used, identically terminate all the output pairs on the same package side whether used or unused. If no outputs on a single side are used, then leave these outputs open (unterminated). This will maintain minimum output skew. Failure to do this will result in a 10–20ps loss of skew margin (propagation delay) in the output(s) in use.

The MC100LVEP111, as with most other LVECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVEP111 to be used for high performance clock distribution in +3.3V or +2.5V systems. Single ended input operation is limited to a $V_{CC} \geq 3.0V$ in LVPECL mode, or $V_{EE} \leq -3.0V$ in LVECL mode. Designers can take advantage of the LVEP111's performance to distribute low skew clocks across the backplane or the board. In a PECL environment, series or Thevenin line terminations are typically used as they require no additional power supplies. For more information on using LVPECL, designers should refer to Application Note AN1406/D.

- 100ps Part–to–Part Skew
- 25ps Output–to–Output Skew
- Differential Design
- V_{BB} Output
- 430ps Typical Propagation Delay
- High Bandwidth to 1.5 Ghz Typical
- LVPECL and HSTL mode: +2.375V to +3.8V V_{CC} with V_{EE} = 0V
- LVECL mode: 0V V_{CC} with V_{EE} = –2.375V to –3.8V
- 75kΩ Internal Input Pulldown Resistors on CLKs, Pull up & Pulldown resistors on $\overline{\text{CLKs}}$
- ESD Protection: >2KV HBM; >100V MM
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 602 devices

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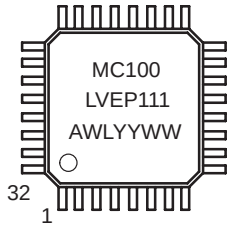
32–LEAD TQFP
FA SUFFIX
CASE 873A

MARKING DIAGRAM*



A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEP111FA	TQFP	250 Units/Tray
MC100LVEP111FAR2	TQFP	2000 Tape & Reel

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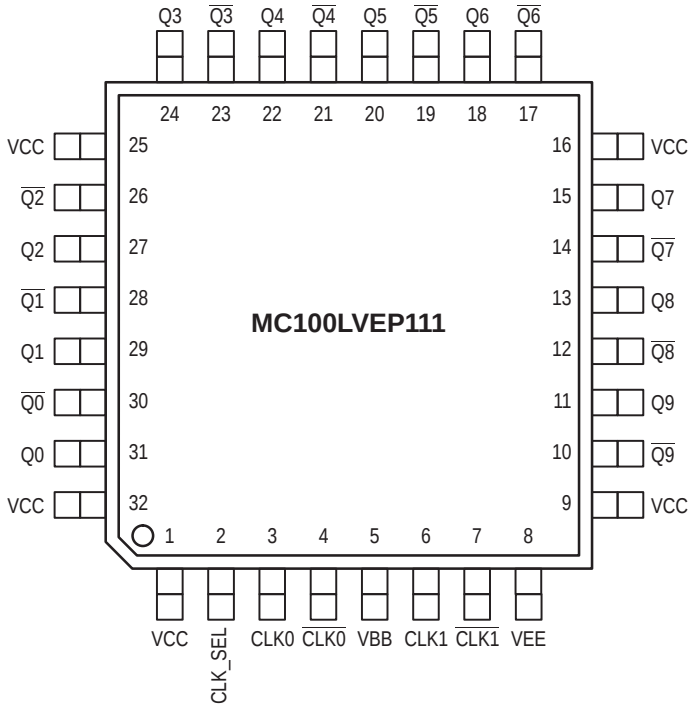


Figure 1. 32–Lead TQFP Pinout
(Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

Pins	Function
CLK0, $\overline{\text{CLK0}}$	LVECL/LVPECL/HSTL CLK Input
CLK1, $\overline{\text{CLK1}}$	LVECL/LVPECL/HSTL CLK Input
Q0:9, $\overline{\text{Q0:9}}$	LVECL/LVPECL Outputs
CLK_SEL	LVECL/LVPECL Active Clock Select Input
VBB	Reference Voltage Output
VCC	Positive Supply
VEE	Negative, 0 Supply

FUNCTION TABLE

CLK_SEL	Active Input
0	CLK0, $\overline{\text{CLK0}}$
1	CLK1, $\overline{\text{CLK1}}$

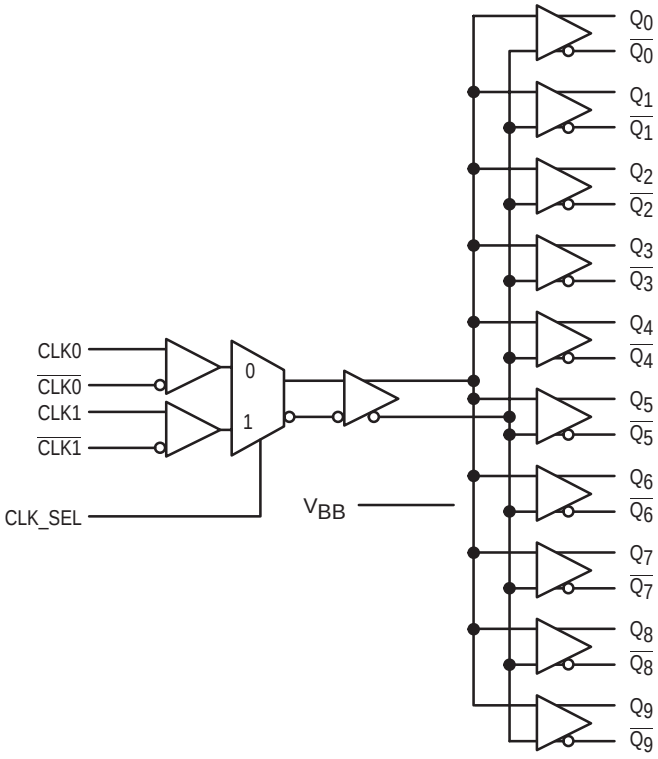


Figure 2. Logic Symbol

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	80 55	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	12 to 17	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V, V_{EE} = –3.3(+0.925, –0.5)V) (Note 5.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current (Note 1.)	70	100	120	70	100	120	70	100	120	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1145	–1020	–0895	–1145	–1020	–0895	–1145	–1020	–0895	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1995	–1820	–1650	–1995	–1820	–1650	–1995	–1820	–1650	mV
V_{IH}	Input HIGH Voltage	–1165		–0880	–1165		–0880	–1165		–0880	mV
V_{IL}	Input LOW Voltage	–1810		–1625	–1810		–1625	–1810		–1625	mV
V_{BB}	Output Reference Voltage (Note 3.)	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 4.)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	μA

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Single ended input operation is limited $V_{EE} \leq$ –3.0V in ECL/LVECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
5. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, HSTL (V_{CC} = 2.5(–0.125, +1.3)V, V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage				1200						mV
V_{IL}	Input LOW Voltage						400				mV
$V_{\cancel{X}}$	Input Crossover Voltage				680		900				mV
I_{CC}	Power Supply Current (Note 6.)	70	100	120	70	100	120	70	100	120	mA

6. V_{CC} = 2.375V to 3.8V, V_{EE} = 0V, all other pins floating.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.5V, V_{EE} = 0V) (Note 11.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current (Note 7.)	70	100	120	70	100	120	70	100	120	mA
V_{OH}	Output HIGH Voltage (Note 8.)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8.)	1305	1480	1650	1305	1480	1650	1305	1480	1650	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1675	1490		1675	1490		1675	mV
V_{BB}	Output Reference Voltage (Note 9.)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 10.)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	μA

7. V_{CCmin} to V_{CCmax}.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Single ended input operation is limited $V_{CC} \geq$ 3.0V in PECL mode.
10. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
11. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVEPECL (V_{CC} = 2.5V ± 0.125V, V_{EE} = 0V) (Note 15.)

		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current (Note 12.)	70	100	120	70	100	120	70	100	120	mA
V_{OH}	Output HIGH Voltage (Note 13.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 13.)	505	680	850	505	680	850	505	680	850	mV
V_{IH}	Input HIGH Voltage	1335		1620	1335		1620	1335		1620	mV
V_{IL}	Input LOW Voltage	690		875	690		875	690		875	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 14.)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	μA

12. V_{CCmin} to V_{CCmax}.
13. All loading with 50 ohms to V_{EE}.
14. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
15. Input and output parameters vary 1:1 with V_{CC}.

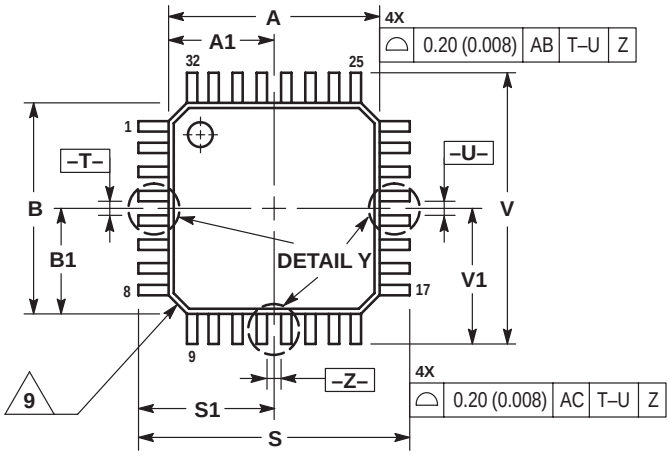
AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –2.5(+0.125, –1.3)V)

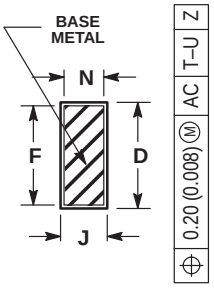
		–40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
$f_{maxLVPECL}$	Maximum Input Frequency for LVECL and LVPECL		1.5			1.5			1.5		GHz
$f_{maxHSTL}$	Maximum Input Frequency for HSTL		250			250			250		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential)	300	400	500	310	430	550	350	510	625	ps
t_{skew}	Within–Device Skew (17.) Part–to–Part Skew (Diff) (18.)		20 100			20 100	25		20 100		ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	100	180	300	120	200	320	130	230	375	ps

16. F_{max} guaranteed for functionality only.
17. Skew is measured between outputs under identical transitions and conditions on any one device.
18. Part–to–part skew for identical transitions at identical V_{CC} levels.

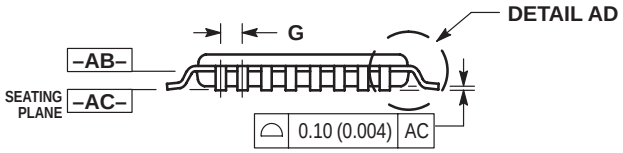
PACKAGE DIMENSIONS

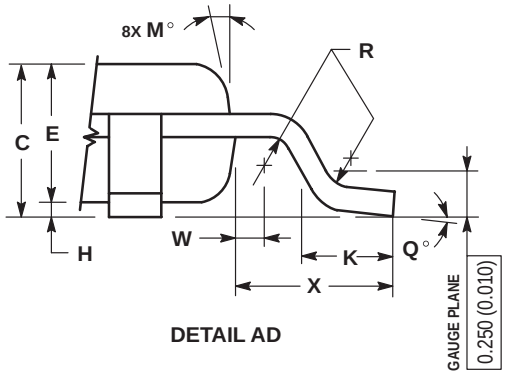
FA SUFFIX
PLASTIC TQFP PACKAGE
CASE 873A–02
ISSUE A



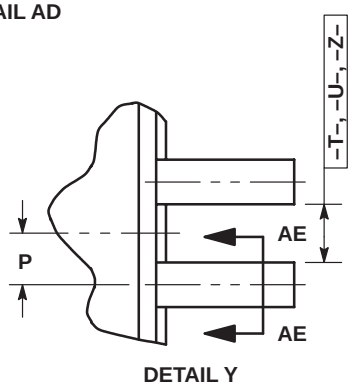


SECTION AE–AE





DETAIL AD



DETAIL Y

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

Notes

Notes

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