MC100LVEP14

Low-Voltage 1:5 Differential LVECL/LVPECL/LVEPECL/HSTL Clock Driver

The MC100LVEP14 is a low skew 1–to–5 differential driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The LVECL/LVPECL input signals can be either differential or single–ended (if the V_{BB} output is used). HSTL inputs can be used when the LVEP14 is operating under LVPECL conditions.

The LVEP14 specifically guarantees low output–to–output skew. Optimal design, layout, and processing minimize skew within a device and from lot to lot.

To ensure that the tight skew specification is realized, both sides of any differential output need to be terminated identically into 50Ω even if only one side is being used. When fewer than all five pairs are used, identically terminate all the output pairs on the same package side whether used or unused. If no outputs on a single side are used, then leave these outputs open (unterminated). This will maintain minimum output skew. Failure to do this will result in a 10–20ps loss of skew margin (propagation delay) in the output(s) in use.

The common enable ($\overline{EN}$) is synchronous, outputs are enabled/disabled in the LOW state. This avoids a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

The MC100LVEP14, as with most other LVECL devices, can be operated from a positive V_{CC} supply in LVPECL mode. This allows the LVEP14 to be used for high performance clock distribution in +3.3V or +2.5V systems. Single ended input operation is limited to a $V_{CC} \geq 3.0V$ in LVPECL mode, or $V_{EE} \leq -3.0V$ in LVECL mode. Designers can take advantage of the LVEP14's performance to distribute low skew clocks across the backplane or the board. For more information, refer to Application Note AN1406/D.

- 100ps Part–to–Part Skew
- 25ps Output–to–Output Skew
- Differential Design
- 400ps Typical Propagation Delay
- High Bandwidth to 1.5 Ghz Typical
- LVPECL and HSTL mode: +2.375V to +3.8V V_{CC} with V_{EE} = 0V
- LVECL mode: 0V V_{CC} with V_{EE} = –2.375V to –3.8V
- 75kΩ Internal Pulldown CLKs, Pull up & Pulldown $\overline{CLK}$s
- ESD Protection: >2KV HBM; >100V MM
- Moisture Sensitivity Level 2
  For Additional Information, See Application Note AND8003/D
- Flammability Rating: UL–94 code V–0 @ 1/8", Oxygen Index 28 to 34
- Transistor Count = 357 devices

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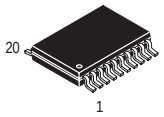
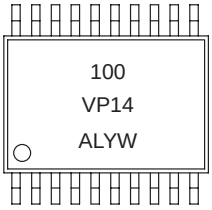


TSSOP–20
DT SUFFIX
CASE 948E

MARKING DIAGRAM*



VP = LVEP
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC100LVEP14DT	TSSOP	75 Units/Tray
MC100LVEP14DTR2	TSSOP	2500 Tape & Reel

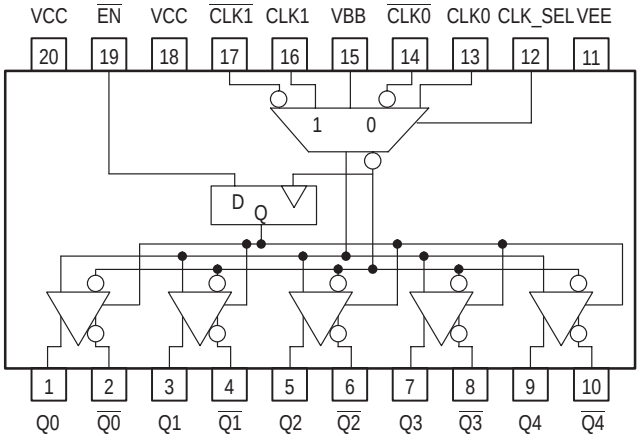


Figure 1. 20–Lead TSSOP and Logic Diagram
(Top View)

Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

PIN DESCRIPTION

Pins	Function
CLK0, $\overline{\text{CLK0}}$	LVECL/LVPECL/HSTL CLK Input
CLK1, $\overline{\text{CLK1}}$	LVECL/LVPECL/HSTL CLK Input
Q0:4, $\overline{\text{Q0:4}}$	LVECL/LVPECL Outputs
CLK_SEL	LVECL/LVPECL Active Clock Select Input
$\overline{\text{EN}}$	Sync Enable
VBB	Reference Voltage Output
VCC	Positive Supply
VEE	Negative, 0 Supply

FUNCTION TABLE

CLK0	CLK1	CLK_SEL	$\overline{\text{EN}}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK0 or CLK1

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–6.0 to 0	VDC
V_{CC}	Power Supply (V_{EE} = 0V)	6.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V, V_I not more negative than V_{EE})	–6.0 to 0	VDC
V_I	Input Voltage (V_{EE} = 0V, V_I not more positive than V_{CC})	6.0 to 0	VDC
I_{out}	Output Current — Continuous Surge	50 100	mA
I_{BB}	V_{BB} Sink/Source Current†	± 0.5	mA
T_A	Operating Temperature Range	–40 to +85	°C
T_{stg}	Storage Temperature	–65 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient) — Still Air 500lfpm	90 60	°C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	30 to 35	°C/W
T_{sol}	Solder Temperature (<2 to 3 Seconds: 245°C desired)	265	°C

* Maximum Ratings are those values beyond which damage to the device may occur.

† Use for inputs of same package only.

DC CHARACTERISTICS, ECL/LVECL (V_{CC} = 0V, V_{EE} = –3.3(+0.925, –0.5)V) (Note 5.)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Power Supply Current (Note 1.)	45	60	75	45	60	75	45	60	95	mA
V_{OH}	Output HIGH Voltage (Note 2.)	–1145	–1020	–0895	–1145	–1020	–0895	–1145	–1020	–0895	mV
V_{OL}	Output LOW Voltage (Note 2.)	–1995	–1820	–1650	–1995	–1820	–1650	–1995	–1820	–1650	mV
V_{IH}	Input HIGH Voltage	–1165		–0880	–1165		–0880	–1165		–0880	mV
V_{IL}	Input LOW Voltage	–1810		–1625	–1810		–1625	–1810		–1625	mV
V_{BB}	Output Reference Voltage (Note 3.)	–1525	–1425	–1325	–1525	–1425	–1325	–1525	–1425	–1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 4.)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	μA

1. V_{CC} = 0V, V_{EE} = V_{EEmin} to V_{EEmax}, all other pins floating.
2. All loading with 50 ohms to V_{CC}–2.0 volts.
3. Single ended input operation is limited $V_{EE} \leq$ –3.0V in ECL/LVECL mode.
4. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
5. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, HSTL (V_{CC} = 2.5(–0.125, +1.3)V, V_{EE} = 0V)

		–40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{IH}	Input HIGH Voltage				1200						mV
V_{IL}	Input LOW Voltage						400				mV
$V_{\mathfrak{B}}$	Input Crossover Voltage				680		900				mV
I_{CC}	Power Supply Current (Note 6.)		100			100			100		mA

6. V_{CC} = 2.375V to 3.8V, V_{EE} = 0V, all other pins floating.

DC CHARACTERISTICS, LVPECL (V_{CC} = 3.3V ± 0.5V, V_{EE} = 0V) (Note 11.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (Note 7.)	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 8.)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 8.)	1305	1480	1650	1305	1480	1650	1305	1480	1650	mV
V_{IH}	Input HIGH Voltage	2135		2420	2135		2420	2135		2420	mV
V_{IL}	Input LOW Voltage	1490		1675	1490		1675	1490		1675	mV
V_{BB}	Output Reference Voltage (Note 9.)	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 10.)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	μA

7. V_{CCmin} to V_{CCmax}.
8. All loading with 50 ohms to V_{CC}–2.0 volts.
9. Single ended input operation is limited $V_{CC} \geq$ 3.0V in PECL mode.
10. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
11. Input and output parameters vary 1:1 with V_{CC}.

DC CHARACTERISTICS, LVEPECL (V_{CC} = 2.5V ± 0.125V, V_{EE} = 0V) (Note 15.)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (Note 12.)	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 13.)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{OL}	Output LOW Voltage (Note 13.)	505	680	850	505	680	850	505	680	850	mV
V_{IH}	Input HIGH Voltage	1335		1620	1335		1620	1335		1620	mV
V_{IL}	Input LOW Voltage	690		875	690		875	690		875	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Note 14.)	1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5 –150			0.5 –150			0.5 –150		150	μA

12. V_{CCmin} to V_{CCmax}.
13. All loading with 50 ohms to V_{EE}.
14. V_{IHCMR} min varies 1:1 with V_{EE}, max varies 1:1 with V_{CC}.
15. Input and output parameters vary 1:1 with V_{CC}.

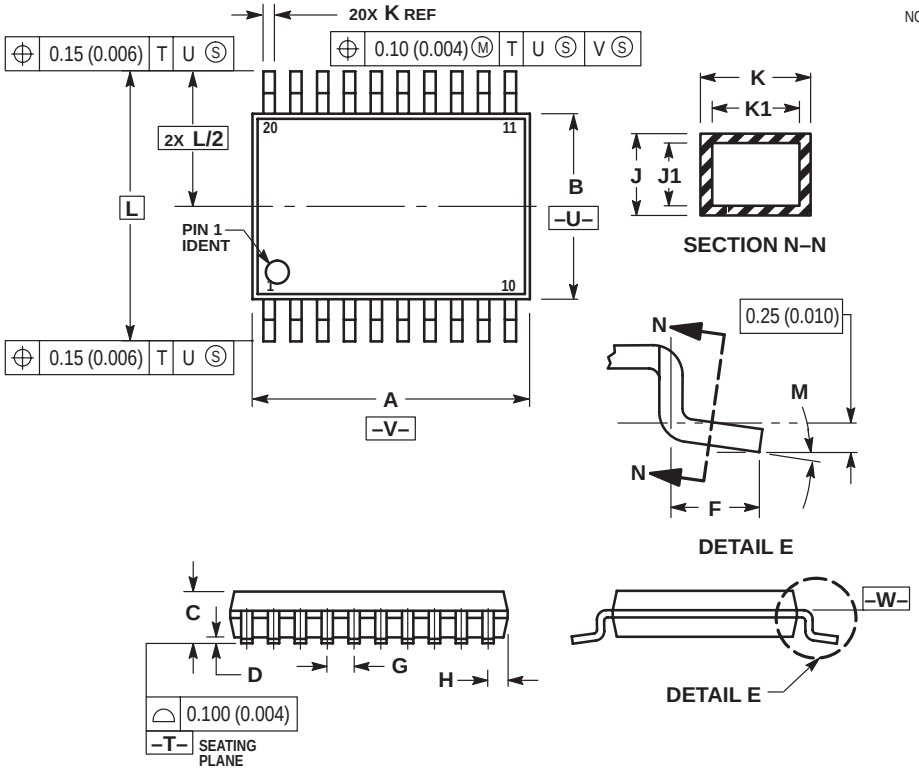
AC CHARACTERISTICS (V_{CC} = 0V; V_{EE} = –2.5(+0.125, –1.3)V)

Symbol	Characteristic	–40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{maxLVPECL}$	Maximum Input Frequency for LVECL and LVPECL		1.5			1.5			1.5		GHz
$f_{maxHSTL}$	Maximum Input Frequency for HSTL		250			250			250		MHz
t_{PLH} t_{PHL}	Propagation Delay to Output IN (differential) IN (single–ended)	275	375	475	300	400 400	500	300	430	550	ps
t_{skew}	Within–Device Skew Part–to–Part Skew (Diff)		TBD TBD			25 100	35		TBD TBD		ps
t_{JITTER}	Cycle–to–Cycle Jitter		TBD			TBD			TBD		ps
V_{PP}	Minimum Input Swing	150	800	1200	150	800	1200	150	800	1200	mV
t_r/t_f	Output Rise/Fall Time (20%–80%)	100	165	250	110	180	275	110	200	290	ps

16. F_{max} guaranteed for functionality only.
17. Skew is measured between outputs under identical transitions.

PACKAGE DIMENSIONS

TSSOP–20
DT SUFFIX
20 PIN PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	—	1.20	—	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

Notes

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