

# 1:9 Differential Clock Driver

The MC10E/100E111 is a low skew 1-to-9 differential driver, designed with clock distribution in mind. It accepts one signal input, which can be either differential or else single-ended if the  $V_{BB}$  output is used. The signal is fanned out to 9 identical differential outputs. An enable input is also provided. A HIGH disables the device by forcing all Q outputs LOW and all  $\bar{Q}$  outputs HIGH.

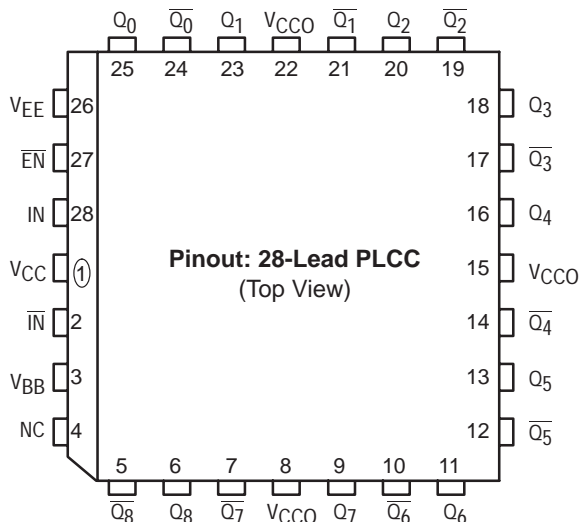
- Low Skew
- Guaranteed Skew Spec
- Differential Design
- $V_{BB}$  Output
- Enable
- Extended 100E  $V_{EE}$  Range of  $-4.2$  to  $-5.46V$
- $75k\Omega$  Input Pulldown Resistors

The device is specifically designed, modeled and produced with low skew as the key goal. Optimal design and layout serve to minimize gate to gate skew within-device, and empirical modeling is used to determine process control limits that ensure consistent  $t_{pd}$  distributions from lot to lot. The net result is a dependable, guaranteed low skew device.

To ensure that the tight skew specification is met it is necessary that both sides of the differential output are terminated into  $50\Omega$ , even if only one side is being used. In most applications, all nine differential pairs will be used and therefore terminated. In the case where fewer than nine pairs are used, it is necessary to terminate at least the output pairs on the same package side (i.e. sharing the same  $V_{CC0}$ ) as the pair(s) being used on that side, in order to maintain minimum skew. Failure to do this will result in small degradations of propagation delay (on the order of 10–20ps) of the output(s) being used which, while not being catastrophic to most designs, will mean a loss of skew margin.

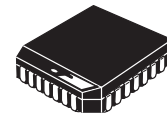
### PIN NAMES

Pin	Function
IN, $\bar{IN}$	Differential Input Pair
$\bar{EN}$	Enable
$Q_0, \bar{Q}_0$ – $Q_8, \bar{Q}_8$	Differential Outputs
$V_{BB}$	$V_{BB}$ Output



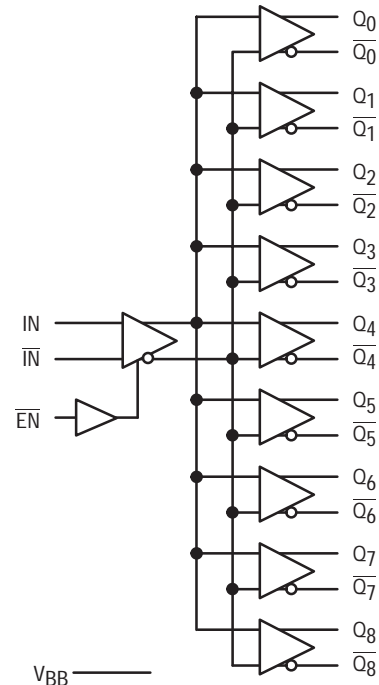
**MC10E111**  
**MC100E111**

**1:9 DIFFERENTIAL  
CLOCK DRIVER**



**FN SUFFIX**  
PLASTIC PACKAGE  
CASE 776-02

### LOGIC SYMBOL



# MC10E111 MC100E111

## DC CHARACTERISTICS (V<sub>EE</sub> = V<sub>EE</sub> (min) to V<sub>EE</sub> (max); V<sub>CC</sub> = V<sub>CCO</sub> = GND)

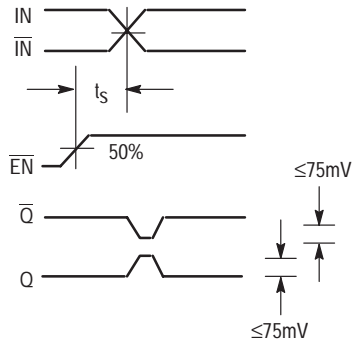
Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit	Cond
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
V <sub>BB</sub>	Output Reference Voltage	10E	-1.43	-1.30	-1.38	-1.27	-1.35	-1.25	-1.31	-1.19	V				
		100E	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26	-1.38	-1.26					
I <sub>IH</sub>	Input HIGH Current		150		150		150		150		150	μA			
I <sub>EE</sub>	Power Supply Current	10E	48	60	48	60	48	60	48	60	mA				
		100E	48	60	48	60	48	60	55	69					
V <sub>PP(DC)</sub>	Input Sensitivity	50		50		50		50		mV	1				
V <sub>CMR</sub>	Common Mode Range	-1.6	-0.4	-1.6	-0.4	-1.6	-0.4	-1.6	-0.4	V	2				

1. Differential input voltage required to obtain a full ECL swing on the outputs.
2. V<sub>CMR</sub> is defined as the range within which the V<sub>IH</sub> level may vary, with the device still meeting the propagation delay specification. The V<sub>IL</sub> level must be such that the peak to peak voltage is less than 1.0 V and greater than or equal to V<sub>pp(min)</sub>.

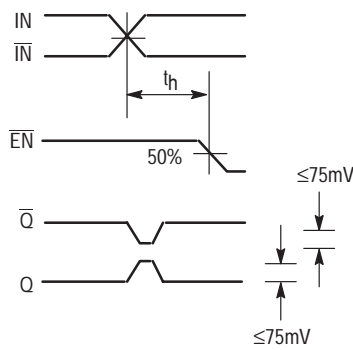
## AC CHARACTERISTICS (V<sub>EE</sub> = V<sub>EE</sub> (min) to V<sub>EE</sub> (max); V<sub>CC</sub> = V<sub>CCO</sub> = GND)

Symbol	Characteristic	-40°C			0°C			25°C			85°C			Unit	Cond
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay to Output			680	460	560	480	580	510	610	ps	1			
	IN (Diff)	380		780	410	610	430	630	460	660					
	IN (SE)	280		900	450	850	450	850	450	850					
	Enable	400		900	450	850	450	850	450	850					
t <sub>s</sub>	Setup Time $\overline{EN}$ to IN	250	0		200	0		200	0		200	0		ps	5
t <sub>H</sub>	Hold Time IN to $\overline{EN}$	50	-200		0	-200		0	-200		0	-200		ps	6
t <sub>R</sub>	Release Time $\overline{EN}$ to IN	350	100		300	100		300	100		300	100		ps	7
t <sub>skew</sub>	Within-Device Skew		25	75		25	50		25	50		25	50	ps	4
V <sub>PP(AC)</sub>	Minimum Input Swing	250			250			250			250			mV	8
t <sub>r</sub> , t <sub>f</sub>	Rise/Fall Time	250	450	650	275	375	600	275	375	600	275	375	600	ps	

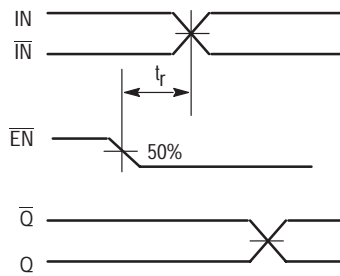
1. The differential propagation delay is defined as the delay from the crossing points of the differential input signals to the crossing point of the differential output signals. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
2. The single-ended propagation delay is defined as the delay from the 50% point of the input signal to the 50% point of the output signal. See *Definitions and Testing of ECLinPS AC Parameters* in Chapter 1 (page 1–12) of the Motorola High Performance ECL Data Book (DL140/D).
3. Enable is defined as the propagation delay from the 50% point of a **negative** transition on  $\overline{EN}$  to the 50% point of a **positive** transition on Q (or a negative transition on  $\overline{Q}$ ). Disable is defined as the propagation delay from the 50% point of a **positive** transition on  $\overline{EN}$  to the 50% point of a **negative** transition on Q (or a positive transition on  $\overline{Q}$ ).
4. The within-device skew is defined as the worst case difference between any two similar delay paths within a single device.
5. The setup time is the minimum time that  $\overline{EN}$  must be asserted prior to the next transition of IN/ $\overline{IN}$  to prevent an output response greater than  $\pm 75$  mV to that IN/ $\overline{IN}$  transition (see Figure 1).
6. The hold time is the minimum time that  $\overline{EN}$  must remain asserted after a negative going IN or a positive going  $\overline{IN}$  to prevent an output response greater than  $\pm 75$  mV to that IN/ $\overline{IN}$  transition (see Figure 2).
7. The release time is the minimum time that  $\overline{EN}$  must be deasserted prior to the next IN/ $\overline{IN}$  transition to ensure an output response that meets the specified IN to Q propagation delay and output transition times (see Figure 3).
8. V<sub>pp(min)</sub> is defined as the minimum input differential voltage which will cause no increase in the propagation delay. The V<sub>pp(min)</sub> is AC limited for the E111 as a differential input as low as 50 mV will still produce full ECL levels at the output.



**Figure 1. Setup Time**



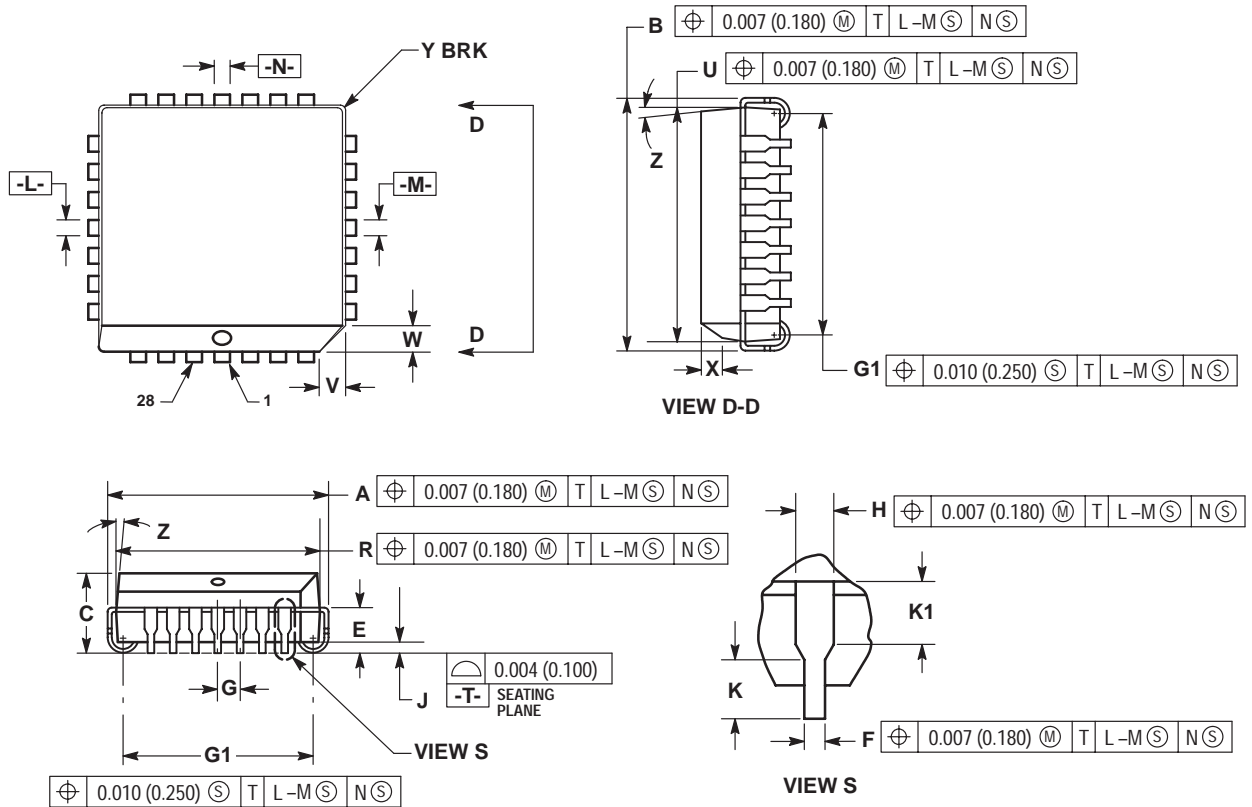
**Figure 2. Hold Time**



**Figure 3. Release Time**

OUTLINE DIMENSIONS


FN SUFFIX  
 PLASTIC PLCC PACKAGE  
 CASE 776-02  
 ISSUE D



NOTES:

- DATUMS -L-, -M-, AND -N- DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
- DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
- DIM R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
- DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	—	0.51	—
K	0.025	—	0.64	—
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	—	0.020	—	0.50
Z	2°		10°	
G1	0.410	0.430	10.42	10.92
K1	0.040	—	1.02	—

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