OXFORD SEMICONDUCTOR

OXFW900

IEEE1394 to ATA/ATAPI Native Bridge

Data Sheet

FEATURES

- S400 compliant 1394-1995 Link and Transaction layers
- Compatible with 1394-1995 and 1394A Phys.
- Buffer Manager with max. RAM bandwidth of 800Mbps
- Microsoft Win98-Second Edition, Win2000 and Apple MacOS 8.5 generic driver support
- SBP-2 Target Revision 4 compliant interface
- Fully ATA-4 compliant (see T13-1153D)
- Sustained IDE transfer rate of 25 Mbytes per second, Peak transfer rate of 50Mbytes per second.
- Supports PIO modes 0 to 4, DMA modes 0 to 2 and Ultra DMA modes 0 to 2
- Integrated 32-bit RISC processor (ARM7TDMI) with on-chip scratch RAM
- ORB co-processor to accelerate translation of ORBs to ATAPI commands
- Supports ORB chaining for increased performance
- High performance ATA command translation in firmware using Reduced Block Command (RBC) set
- Optional External Serial ROM interface for configuration data, user serial number, etc.
- Blank Flash memory programming feature via 1394 bus
- 3.3 Volts operation
- Low Power CMOS
- Firmware and Flash Programming Utilities supplied by Oxford Semiconductor
- ultra-thin 128-TQFP package (14mm x 14mm x 1mm)

DESCRIPTION

The OXFW900 is a high-performance 1394 to ATA/ATAPI (IDE) native bridge with an integrated target Serial Bus Protocol (SBP-2) controller. By supporting the SBP-2 protocol, the device can use generic SBP-2 drivers available in the Microsoft Windows 98SE, Microsoft Windows 2000, Microsoft Millennium and Apple MacOS operating systems.

The device is ideally suited for smart-cable or tailgate interface applications for removable-media drives, compact flash card readers, CD-ROM, CD-R, CD-RW, DVD-ROM, DVD-RAM and hard disk drives, allowing IDE drives to be connected to a 1394 serial bus in a plug-and-play fashion. Both ATA and ATAPI devices are supported using the same firmware.

This highly integrated device offers a three-chip solution to native bridge applications using an external 1394 PHY and Flash ROM. A slow 32Kx8 Flash ROM (up to 120ns) is sufficient for most optical media applications. For applications that need a sustained data rate in excess of 10Mbytes per second, for example high performance disk drives, an 8-bit 50ns FLASH or faster is recommended. The device is compatible with both 1394-1995 and 1394A PHYs.

The LINK controller complies with S400 1394-1995 specification. The 1394 transaction layer and SBP-2 protocol is implemented using a combination of the ARM7TDMI (low-power 32-bit RISC processor), an ORB (Operational Request Block) hardware co-processor and a high performance buffer manager.

The Buffer Manager has a RAM bandwidth of 800Mbps. It provides storage for 1394 and ATA/ATAPI packets, automatically storing them and passing them to the appropriate destinations, without any intervention from the processor. It also provides storage and manages the sequencing of ORB fetching to reduce latency and improve data throughput.

The configuration data including the IEEE OUI (Organisational Unique Identifier) and device serial number is stored in the Flash ROM which may be uploaded from the 1394 bus, even when blank. The device also facilitates firmware uploads from the 1394 bus.

The ORB co-processor translates ORBs as defined in the SBP-2 protocol into ATA/ATAPI commands, and automatically stores error/status messages at an address specified by the host.

Concurrent operation of the ATA/ATAPI and 1394 interfaces are facilitated using the high throughput Buffer Manager where LINK, ATAPI manager and ARM7TDMI can perform interleaved accesses to the on-chip RAM buffer. The high performance processor ensures that no significant latency is incurred. The ATA command translation is performed in firmware to meet RBC (Reduced Block Commands) standard, T10-1228D. The ATA/ATAPI Manager supports PIO modes 0 to 4, DMA modes 0 to 2 and Ultra DMA mode 0 to 2 and provides the interface to the IDE bus. It is compliant with T13-1153D, ATA-4 specification.

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OXFW900 Data Sheet Revision 1.0 – Nov 1999
Part No. OXFW900-TQ-A

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1 BLOCK DIAGRAM

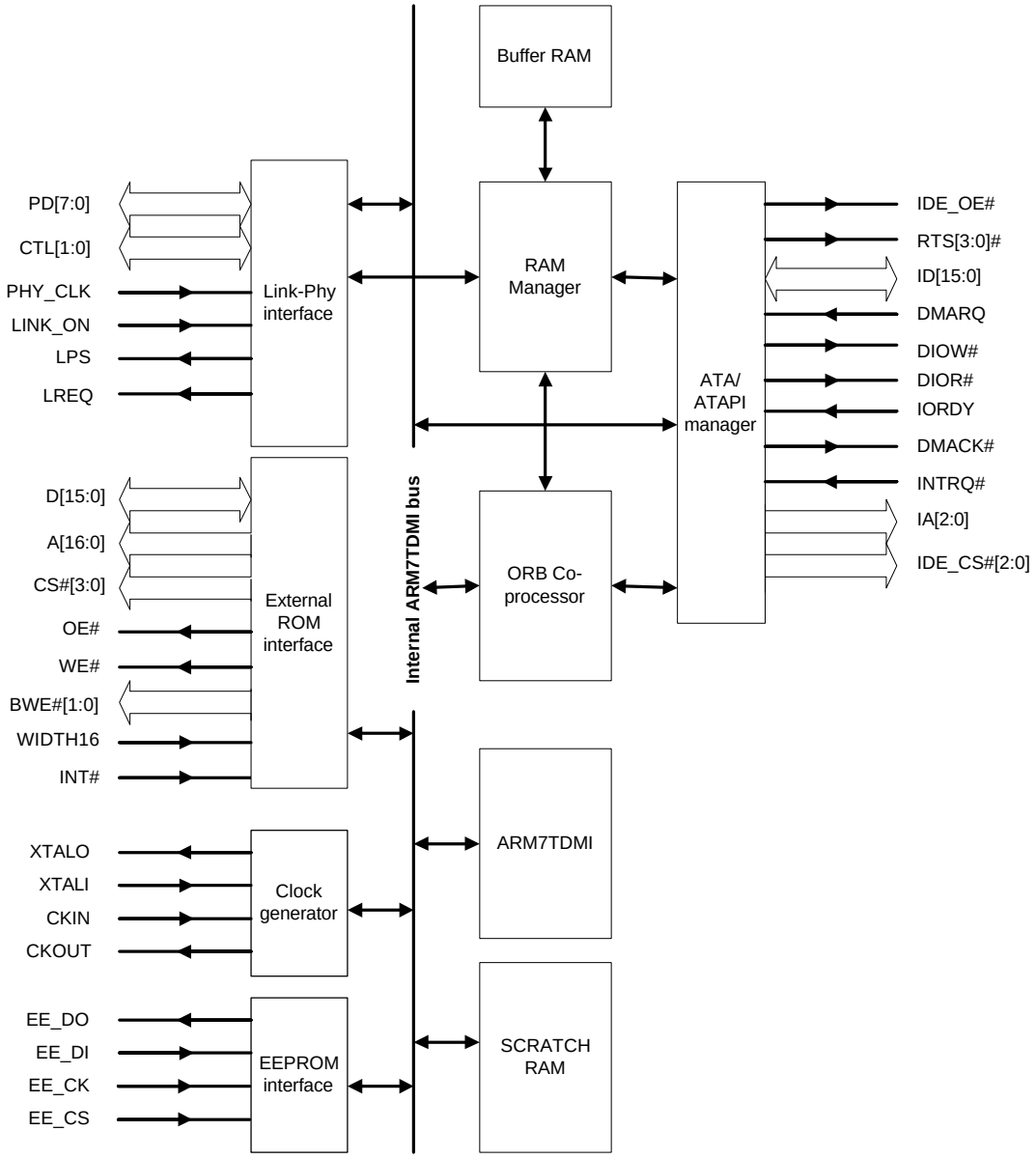


Figure 1: OXFW900 Block Diagram

2 PIN INFORMATION

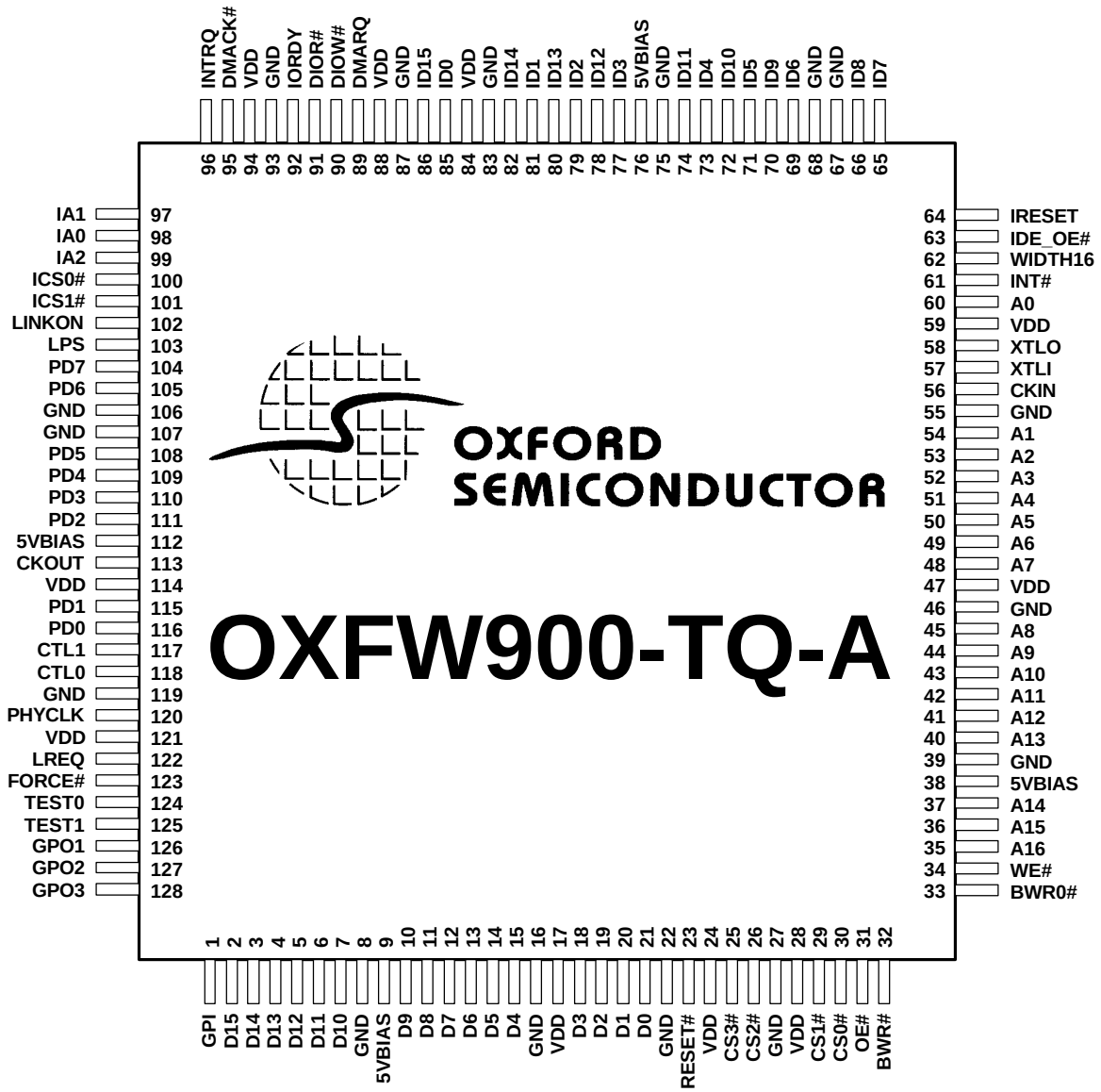


Figure 2: Pinout (package = 128 TQFP)

3 PIN DESCRIPTIONS

1394 PHY-LINK interface	Dir[1]	Name	Description
104, 105, 108, 109, 110, 111, 115, 116	I/O	PD[7:0]	Phy-Link Data Bus
117,118	I/O	CTL[1:0]	Phy-Link Control Bus
120	I	PHYCLK	49.152 MHz clock sourced by PHY
122	O	LREQ	Link Request
102	IU	LINKON	Requests link to power up when in a low power mode
103	O	LPS	Indicates to phy that link is powered and ready
ARM external interface			
2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, 18, 19, 20, 21	T_I/O	D[15:0]	ARM external data bus
35, 36, 37, 40, 41, 42, 43, 44, 45, 48, 49, 50, 51, 52, 53, 54, 60	T_O	A[16:0]	ARM external address bus
25, 26, 29, 30	T_O	CS#[3:0]	ARM external chip selects. CS0# is always used for program ROM.
31	T_O	OE#	ARM external output enable. Active when reading data from external devices including program ROM
32, 33	T_O	BWR#[1:0]	Byte Write enables. For future expansion
34	T_O	WE#	Write Enable. Active when writing to external devices
62	ID	WIDTH16	'1' = 16 bit external ROM '0' = 8 bit external ROM (pulldown)
61	T_IU	INT#	External ARM interrupt
IDE interface			
65, 66, 69, 70, 71, 72, 73, 74, 77, 78, 79, 80, 81, 82, 85, 86	T_I/O	ID[15:0]	IDE data bus
97, 98, 99	T_O	IA[2:0]	IDE address bus
100, 101	T_O	ICS#[1:0]	IDE chip select. Selects IDE drive 0 or 1
63	T_O	IDE_OE#[	IDE output enable. Only used when external buffering is required to drive IDE data bus
64	T_O	IRESET	IDE interface reset
89	T_I	DMARQ	
90	T_O	DIOW#	IDE interface write strobe
91	T_O	DIOR#	IDE interface read strobe
92	T_O	IORDY	
95	T_O	DMACK#	
96	T_I	INTRQ	
EEPROM interface			
128	O	GPO3	General Purpose Output 3
126	O	GPO1	General Purpose Output 1
1	IU	GPI	General Purpose Input
127	O	GPO2	General Purpose Output 2
Miscellaneous Pins			
57	I	XTLI	Crystal Oscillator input. 24.576 MHz crystal required. If a clock module is used rather than a crystal then this input must be tied high for the OXFW900 to operate, and the clock module output connected to the CKIN pin. IMPORTANT - See Application Notes regarding clocking
58	O	XTLO	Crystal Oscillator output. IMPORTANT – See Application Notes regarding clocking.

56	I	CKIN	Direct clock input. Used in conjunction with an external crystal oscillator of 24.576MHz. If a crystal is connected to XTLI and XTLO this input must be tied low for the OXFW900 to operate. Mark space ratio of crystal oscillator must be 45:55 or better. IMPORTANT – Please refer to Application Notes regarding clocking
23	IU	RESET#	Global reset for the OXFW900. Active Low.
113	T_O	CKOUT	Clock output. 24.576 MHz clock output. IMPORTANT – Please refer to Application Notes regarding clocking
123	IU	FORCE#	This input is used to allow the OXFW900 to reprogram a flash which has been loaded with a bad program. A bad program is defined as one that does not have the correct interlocking mechanism for reprogramming flash. This pin forces the ARM watchdog timer to trigger thus allowing the flash to be reprogrammed over the 1394 bus as if the flash were blank.
124, 125	IU	TEST[1:0]	'11' = NORMAL OPERATION. These pins have internal pullup resistors and must be left unconnected. Other settings are for foundry test purposes only.
Power and ground[2]			
28, 47, 94, 114	3V3	3.3V AC VDD	Supplies power to output buffers in switching (AC) state
17, 24, 59, 84, 88, 121	3V3	3.3V DC VDD	Power supply. Supplies power to core logic, input buffers and output buffers in steady state
9, 38, 76, 112	5V	5V BIAS VDD	Supplies 5V reference bias to all 5V tolerant I/O. All four MUST be connected to 5V rail.
8, 27, 46, 67, 75, 93, 106	G	AC GND	Supplies GND to output buffers in switching (AC) state
16, 22, 39, 55, 68, 83, 87, 107, 119	G	DC GND	Ground (0 volts). Supplies GND to core logic, input buffers and output buffers in steady state

Table 1: Pin Descriptions

Note 1: Direction key:

I	Input	T_O	5V tolerant output
IU	Input with internal pull-up	T_I/O	5V tolerant bi-directional
ID	Input with external pull-down		
O	Output		
I/O	Bi-directional	G	Ground
		3V3	3.3V power
T_I	5V tolerant input	5V	5V bias power

Note 2: Power & Ground

There are two GND and three VDD rails internally. One set of rails supply power and ground to output buffers while in switching state (called AC power) and another rail supply the core logic, input buffers and output buffers in steady-state (called DC rail). A third rail provides 5V bias voltage to 5V tolerant IO.

The rails are not connected internally. This precaution reduces the effects of simultaneous switching outputs and undesirable RF radiation from the chip.

4 OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply voltage	-0.3	4.6	V
V_{IN}	DC input voltage	-0.3	V_{DD} + 0.3	V
I_{IN}	DC input current		+/- 10	mA
T_{STG}	Storage temperature	-40	125	°C

Table 2: Absolute maximum ratings

Symbol	Parameter	Min	Max	Units
V_{DD}	DC supply voltage	3.0	3.6	V
V_{BB}	5V PMOS bulk bias	4.75	5.25	V
T_C	Temperature	0	70	°C

Table 3: Recommended operating conditions

5 DC ELECTRICAL CHARACTERISTICS

5.1 I/O Buffers

Symbol	Parameter	Condition	Min	Max	Units
V_{DD}	Supply voltage	Commercial	3.0	3.6	V
V_{IH}	Input high voltage	CMOS Interface CMOS Schmitt trig	0.7 x Vdd 2.1		V
V_{IL}	Input low voltage	CMOS Interface [1] CMOS Schmitt trig		0.3 x Vdd 0.8	V
C_{IL}	Cap of input buffers			5.0	pF
C_{OL}	Cap of output buffers			10.0	pF
I_{IH}	Input high leakage current	$V_{in} = V_{DD}$	-10	10	µA
I_{IL}	Input low leakage current	$V_{in} = V_{SS}$	-10	10	µA
V_{OH}	Output high voltage	I_{OH} = -1 µA	V_{DD} – 0.05		V
V_{OH}	Output high voltage	I_{OH} = -1mA to –24mA	2.4		V
V_{OL}	Output low voltage	I_{OL} = 1 µA		0.05	V
V_{OL}	Output low voltage	I_{OL} = 1mA to 24mA		0.4	V
I_{OZ}	3-state output leakage current		-10	10	µA

Symbol	Parameter	Condition	Typical	Max	Units
I_{CC}	Operating supply current in normal mode				mA
	Operating supply current in Power-down mode				

Table 4: Characteristics of OXFW900 I/O buffers

6 AC ELECTRICAL CHARACTERISTICS

6.1 IDE interface

Symbol	Parameter	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Units
t0	Cycle Time	600	400	360	200	120	ns
t1	Address Valid to DIOR# / DIOW# setup	80	80	40	40	40	ns
t2	DIOR# / DIOW# pulse width	320	320	320	80	80	ns
t2i	DIOR# / DIOW# recovery time	-	-	-	80	40	ns
t3	DIOW# data setup (min)	60	45	30	30	20	ns
t4	DIOW# data hold	40	40	40	40	40	ns
t5	DIOR# data setup (min)	50	35	20	20	20	ns
t6	DIOR# data hold (min)	5	5	5	5	5	ns
t6z	DIOR# data tristate (max)	30	30	30	30	30	ns
t9	DIOR# / DIOW# to address valid hold	40	40	40	40	40	ns
tRD	Read Data Valid to IORDY active if IORDY initially low after tA	0	0	0	0	0	ns
tA	IORDY Setup time	35	35	35	35	35	ns
tB	IORDY Pulse Width (max)	1250	1250	1250	1250	1250	ns
tA	IORDY assertion to release	5	5	5	5	5	ns

Table 5: OXFW900 IDE PIO / Register Transfers

Symbol	Parameter	Mode 0	Mode 1	Mode 2	Units
t0	Cycle time	480	160	120	ns
tD	DIOR# / DIOW#	240	80	80	ns
tE	DIOR# data access (max)	150	60	50	ns
tF	DIOR# data hold (min)	5	5	5	ns
tG	DIOR# / DIOW# data setup	100	30	20	ns
tH	DIOW# data hold	20	15	10	ns
tI	DMACK to DIOR# / DIOW# setup (min)	0	0	0	ns
tJ	DIOR# / DIOW# to DMACK hold (min)	20	5	5	ns
tKr	DIOR# negated pulse width	80	80	40	ns
tKw	DIOW# negated pulse width	240	80	40	ns
tLr	DIOR# to DMARQ delay (max)	120	40	35	ns
tLw	DIOW# to DMARQ delay (max)	40	40	35	ns
tM	IDCS[1:0] valid to DIOR# / DIOW#	80	40	40	ns
tN	IDCS[1:0] hold	40	40	40	ns
tZ	DMACK to tristate (max)	20	25	25	ns

Table 6: OXFW900 Multiword DMA timings

Symbol	Parameter	Mode 0 min	Mode 0 max	Mode 1 min	Mode1 max	Mode 2 min	Mode 2 max	Units
t2cyc	Typical sustained average two cycle time	240		160		120		ns
tcyc	Cycle time allowing for clock variations (refer to ATA spec)	114		75		55		ns
t2cyc	Two cycle time allowing for clock variations (refer to ATA spec)	235		156		117		ns
tds	Data setup time at recipient	15		10		7		ns
tdh	Data hold time at recipient	5		5		5		ns
tdvs	Data valid setup time at sender (from data bus being valid until STROBE edge)	70		48		34		ns
tdvh	Data valid hold time at sender (from STROBE edge until data may become invalid	6		6		6		ns
tfs	First STROBE time (for device to first negate DSTROBE from STOP during a data-in burst)	0	230	0	200	0	170	ns
tli	Limited interlock time	0	150	0	150	0	150	ns
tmli	Interlock time with minimum	20		20		20		ns
tui	Unlimited interlock time	0		0		0		ns
taz	Maximum time allowed for output drivers to release (from being asserted or negated)		10		10		10	ns
tzah tzad	Minimum delay time required for output drivers to assert or negate (from released state)	20 0		20 0		20 0		ns
tenv	Envelope time (from DMACK# to STOP and HDMARDY# during data-out burst initiation	20	70	20	70	20	70	ns
tsr	STROBE to DMARDY time (refer to ATA spec	20		25		25		ns
trfs	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after the negation of DDMARDY#		75		60		50	ns
trp	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY#)	160		125		100		ns
tiordyz	Pull-up time before allowing IORDY to be released		20		20		20	ns
tziordy	Minimum time a device shall wait before driving IORDY	0		0		0		ns
tack	Setup and hold times for DMACK# (before assertion or negation)	20		20		20		ns
tss	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50		50		ns

Table 7: OXFW900 Ultra DMA timings

6.2 1394 Link-Phy interface

The timings for 1394 Link – Phy are shown below :

Symbol	Parameter	Min	Max	Units
tlsu	Setup Time, PD[7:0] and CTL[1:0] before PhyClk	6		ns
tlh	Hold Time, PD[7:0] and CTL[1:0] after PhyClk	0		ns
Tld1	Delay Time, PhyClk input high to initial instance of PD[7:0], CTL[1:0] and Lreq outputs valid	TBD	TBD	ns
Tld2	Delay Time, PhyClk input high to subsequent instance(s) of PD[7:0], CTL[1:0] and Lreq outputs valid	TBD	TBD	ns
Tld3	Delay Time, PhyClk input high to PD[7:0], CTL[1:0] and Lreq outputs invalid (high impedance)	TBD	TBD	ns

Table 8: OXFW900 Link-Phy interface timings

6.3 External Processor Interface

Name	Description	min (ns)	typ (ns)	max (ns)
	Common Timings	-	-	-
tas	Address valid to CSx# and OE# falling	0.3		2.5
tcss	CSx# and OE# falling to WE# or IOR# falling	16		18.5
tws	Wait State Additional Delay	0	0	600
taddr1	Not Last Address Valid			
taddr2	Last Address Valid			
	Common Read Timings	-	-	-
tiorl	IOR# valid			
tah	Address hold after CSx# or OE# rising			
	Single Access Read Timings	-	-	-
tdsa	Data valid and stable to CSx# and OE# rising			
tdha	Data hold after CSx# and OE# rising	0		
tdsb	Data valid and stable to IOR# rising			
tdhb	Data hold after IOR# rising	0		
	Multiple Access Read Timings	-	-	-
dsa1	Data valid and stable to CSx# and OE# rising (not last access)			
dha1	Data hold after CSx# and OE# rising (not last access)	0		
dsb1	Data valid and stable to IOR# rising (not last access)			
dhb1	Data hold after IOR# rising (not last access)	0		
dsa2	Data valid and stable to CSx# and OE# rising (last access)			
dha2	Data hold after CSx# and OE# rising (last access)	0		
dsb2	Data valid and stable to IOR# rising (last access)			
dhb2	Data hold after IOR# rising (last access)	0		
tahr	IOR# rising to next address valid			
tasr	Address valid to IOR# falling			
tiorh	IOR# inactive between reads			
	Common Write Timings	-	-	-
tds	Data valid to WE# rising	39+tws		
tdh	Data hold after WE# rising	13		17
tcsh	CS# hold after WE# rising	20		
tcsa	CS# hold after Address invalid	1		2.5
twel	WE# valid			
	Single Access Write Timings	-	-	-
tah	Address hold after WE# rising	19		60
	Multiple Access Write Timings	-	-	-
tas1	Address valid to CSx# and OE# falling			
tah1	Address hold after WE# rising (not last access)			
tas2	WE# falling after next address valid			
tah2	Address hold after WE# rising (last access)			
tweh	WE# inactive between writes			

Table 9: External Processor Interface timings

All timings are preliminary and are subject to change

7 TIMING WAVEFORMS

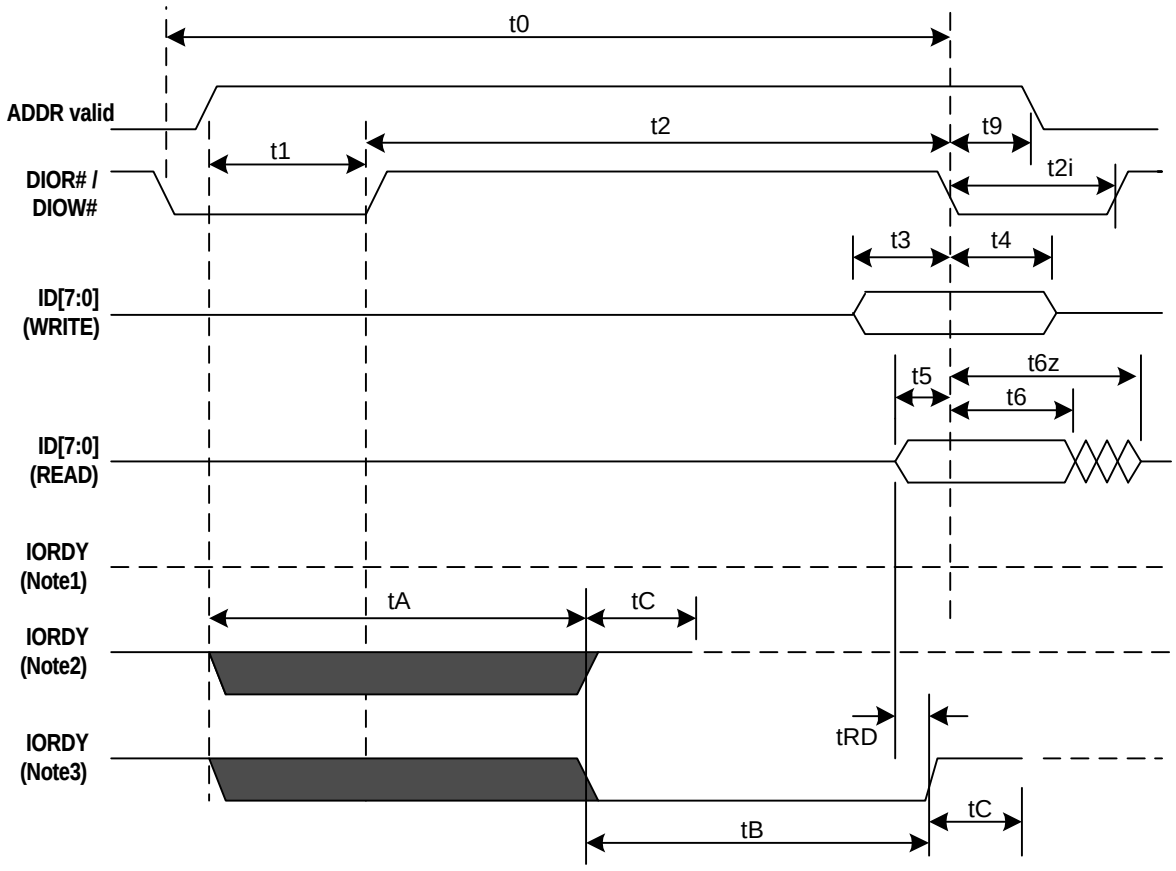


Figure 3: PIO / Register Transfer to / from IDE device

Notes : Negation of IORDY by the drive is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after tA from the Assertion of DIOR# or DIOW#. The assertion and negation of IORDY are described in the following three cases : -

1) Device never negates IORDY and no wait is generated.
2) Device negates IORDY before tA, but causes IORDY to be asserted before tA. IORDY is released prior to negation and may be asserted for no more than 5ns before release : no wait generated.
3) Device negated IORDY before tA. IORDY is released prior to negation and may be asserted for no more than 5ns before release : wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR# is asserted, the device shall place read data on DD[7:0] for tRD before asserting IORDY

TIMING WAVEFORMS

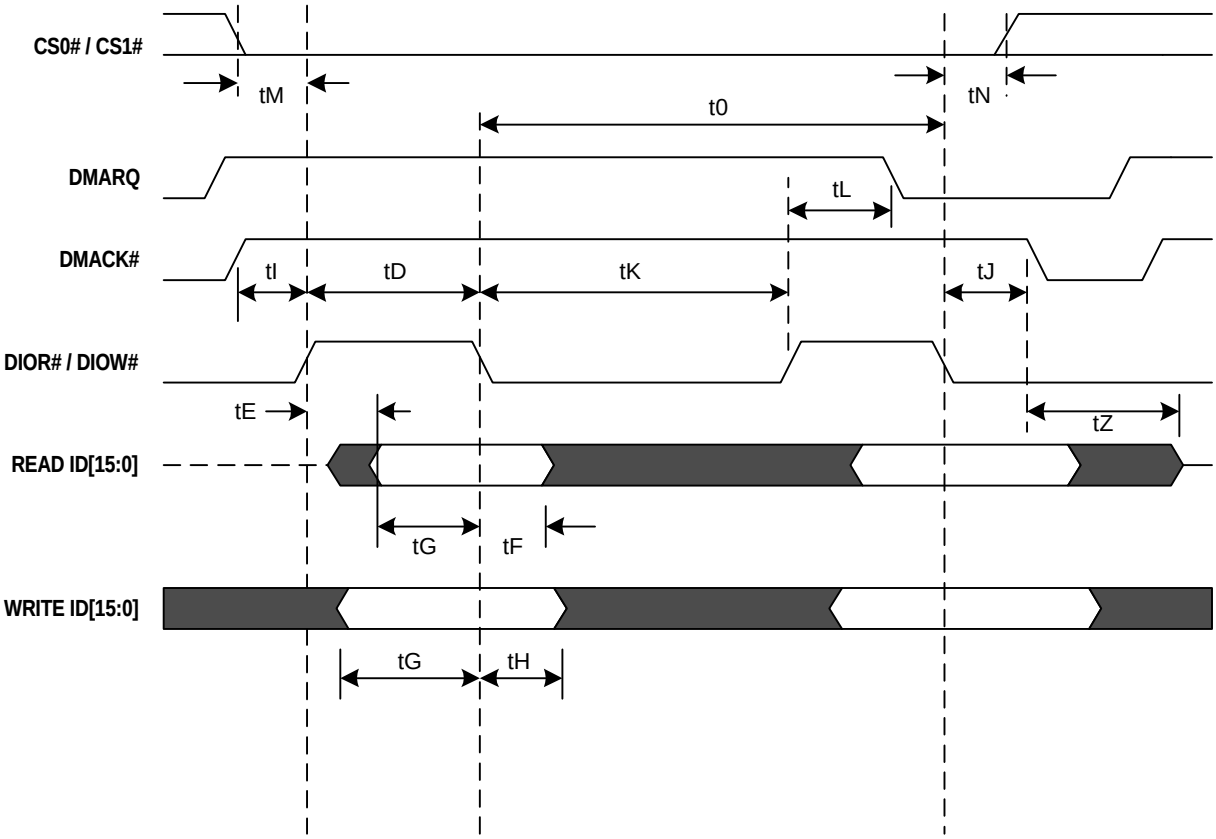


Figure 4: MultiWord DMA transfer to / from IDE device

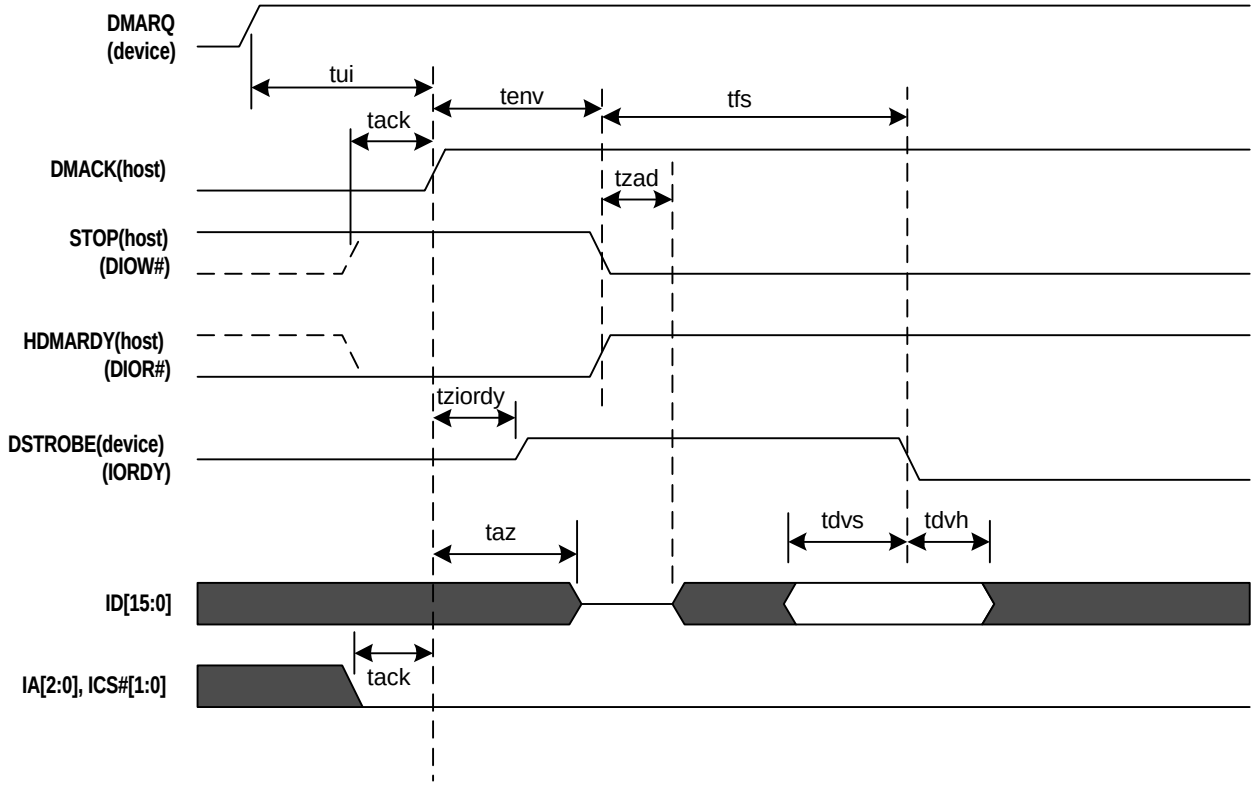


Figure 5: Initiating an Ultra DMA data-in burst

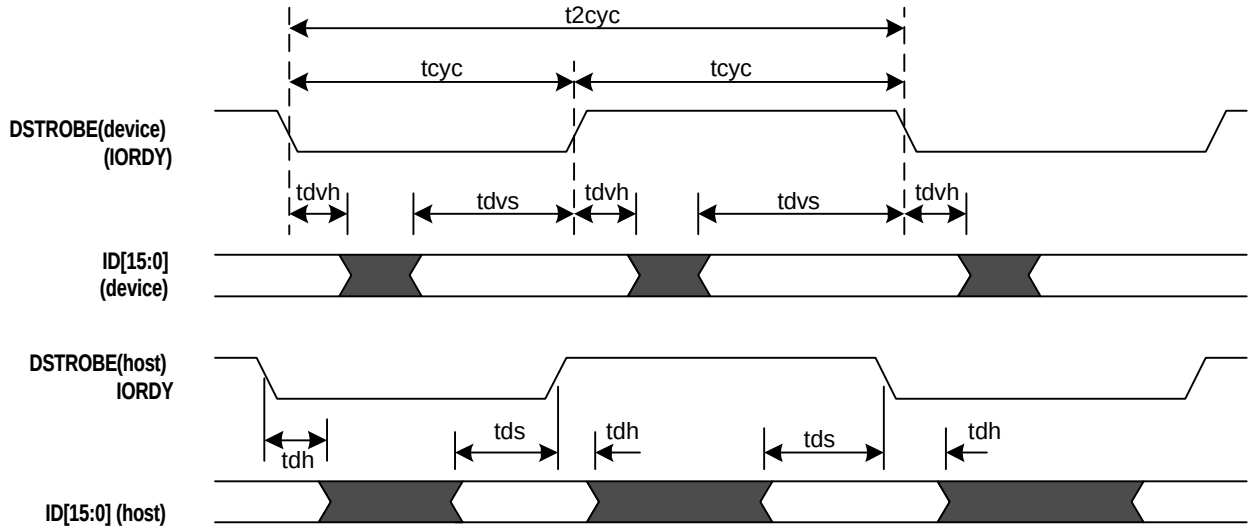


Figure 6: Sustained Ultra DMA data-in burst

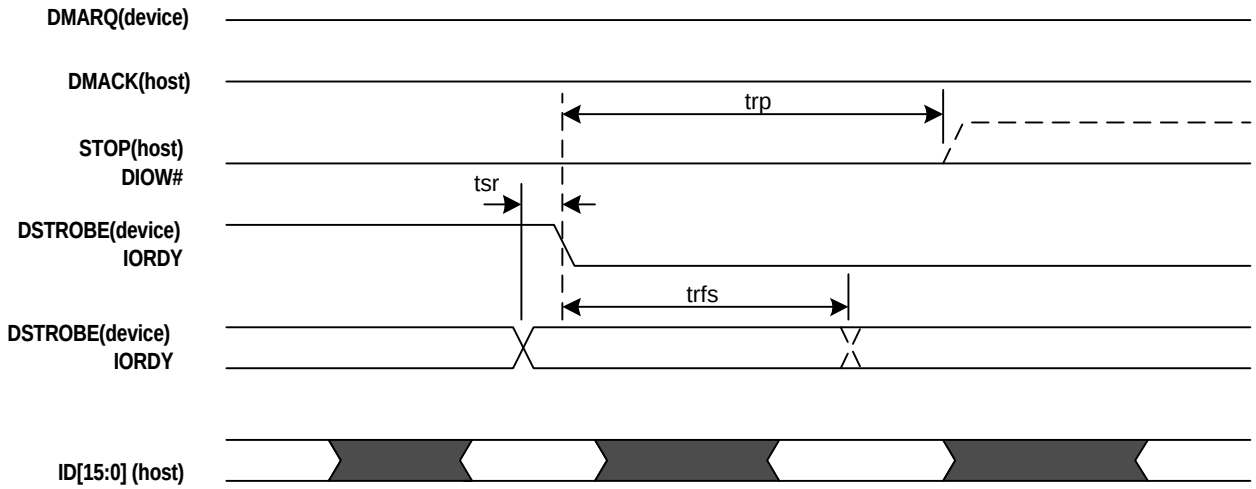


Figure 7: Host pausing an Ultra DMA data-in burst

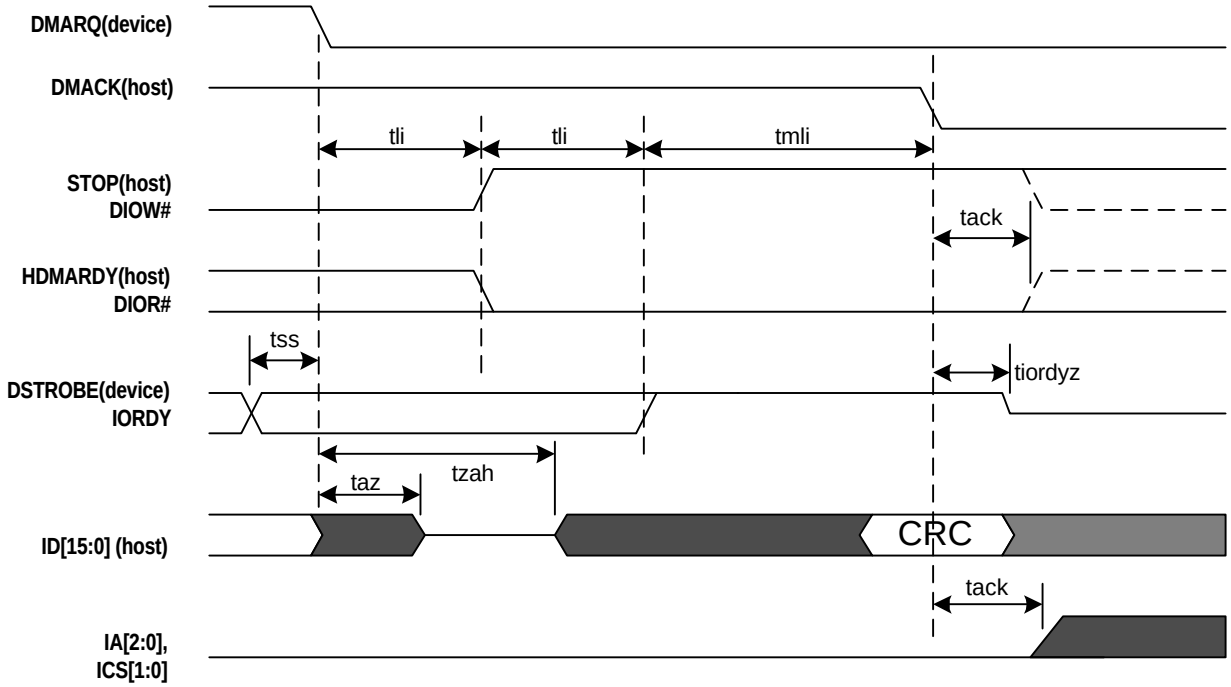


Figure 8: Device terminating an Ultra DMA data-in burst

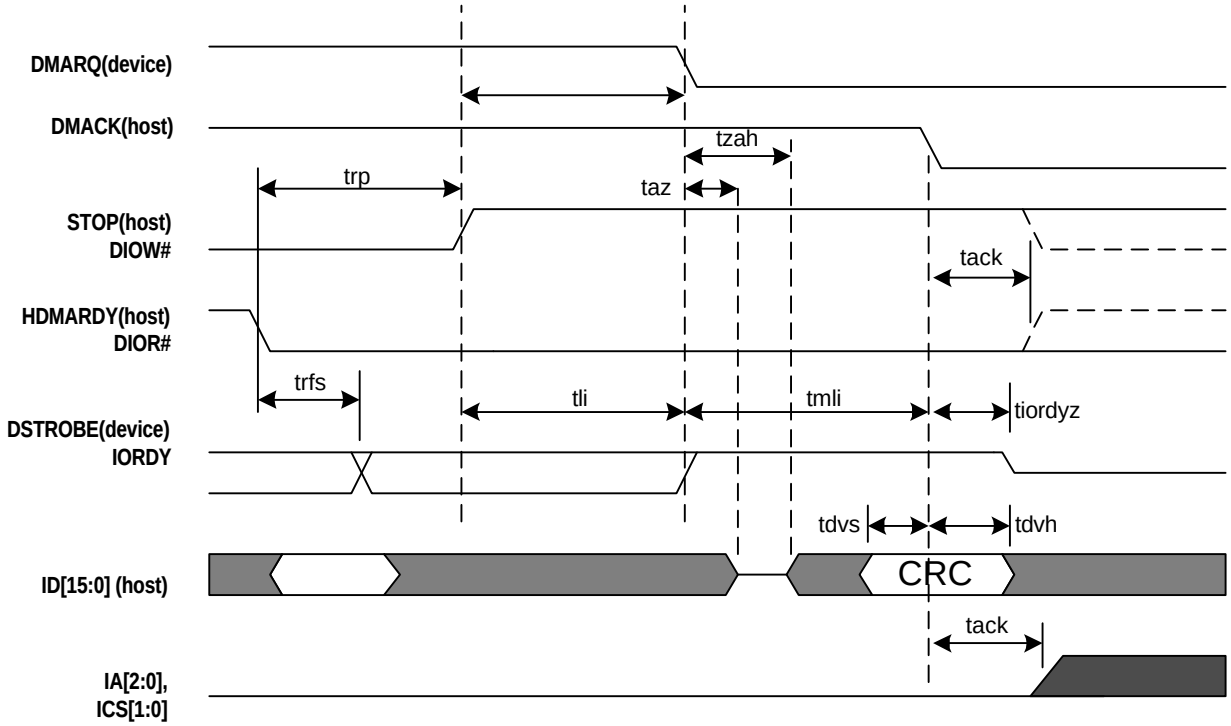


Figure 9: Host terminating an Ultra DMA data-in burst

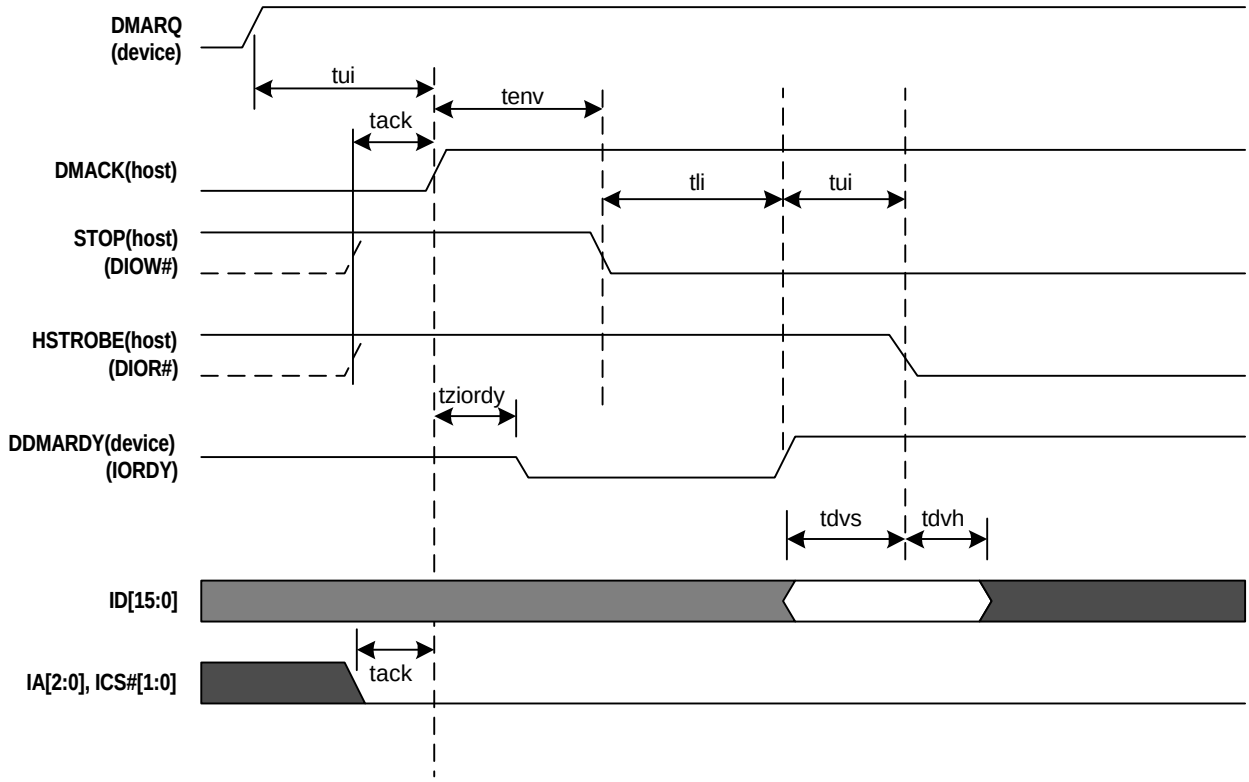


Figure 10: Initiating an Ultra DMA data-out burst

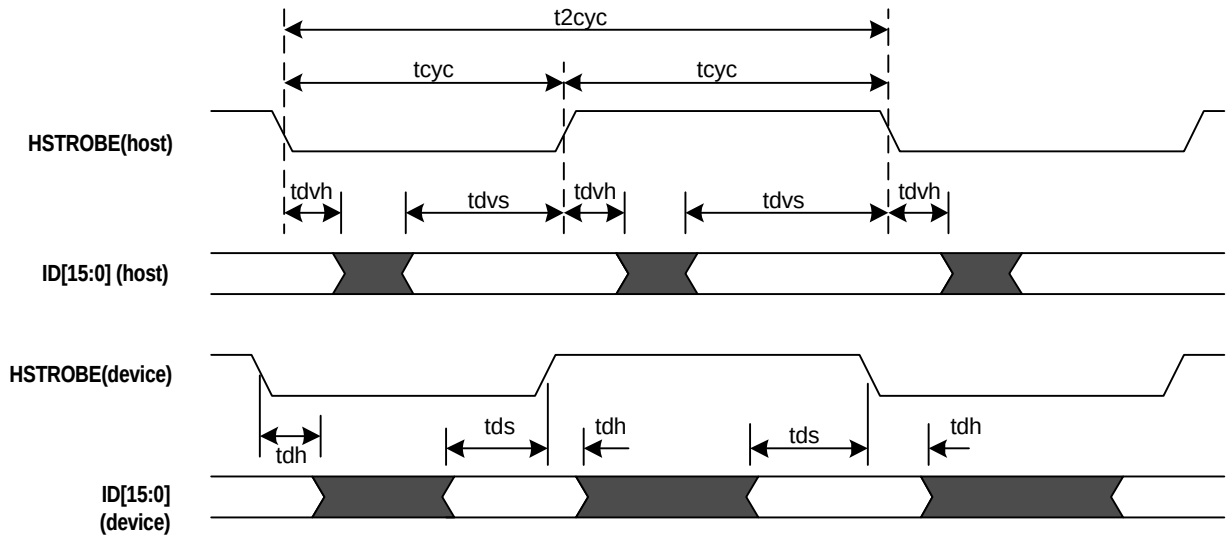


Figure 11: Sustained Ultra DMA data-out burst

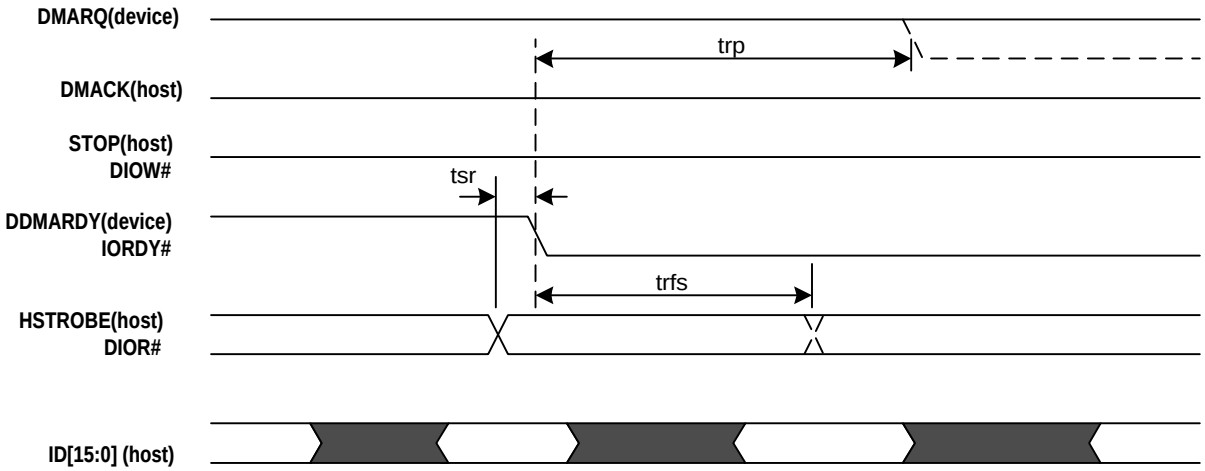


Figure 12: Device pausing an Ultra DMA data-in burst

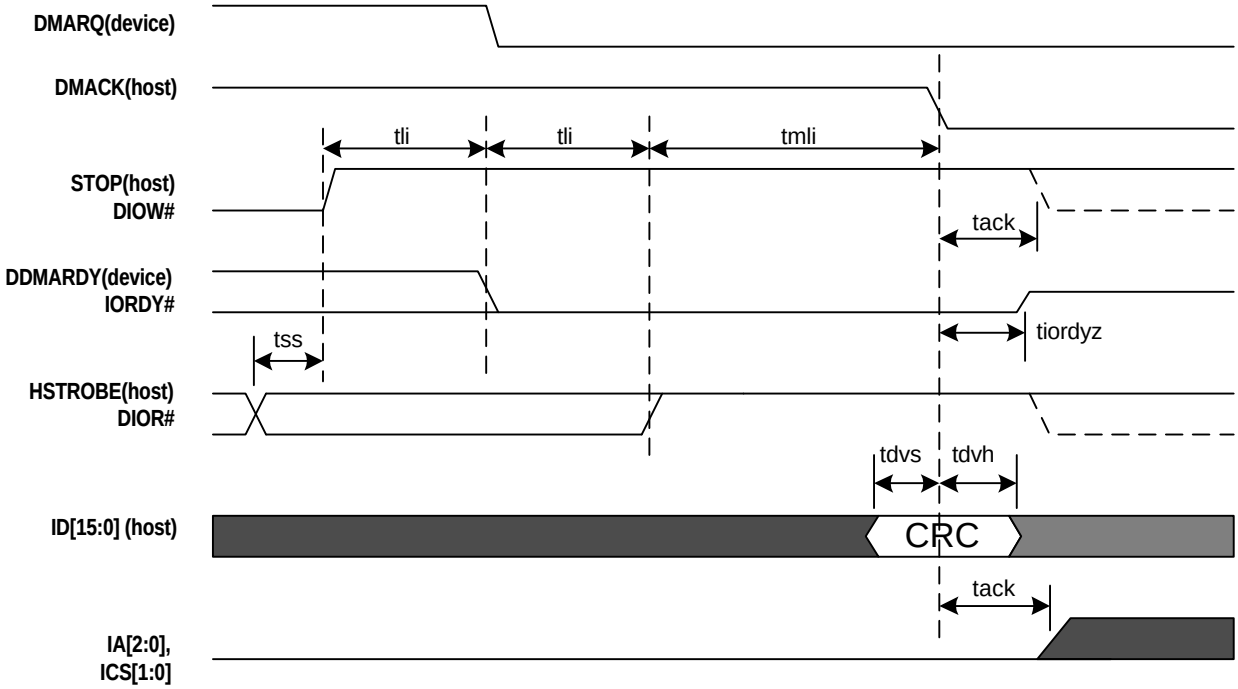


Figure 13: Host Terminating an Ultra DMA data-out burst

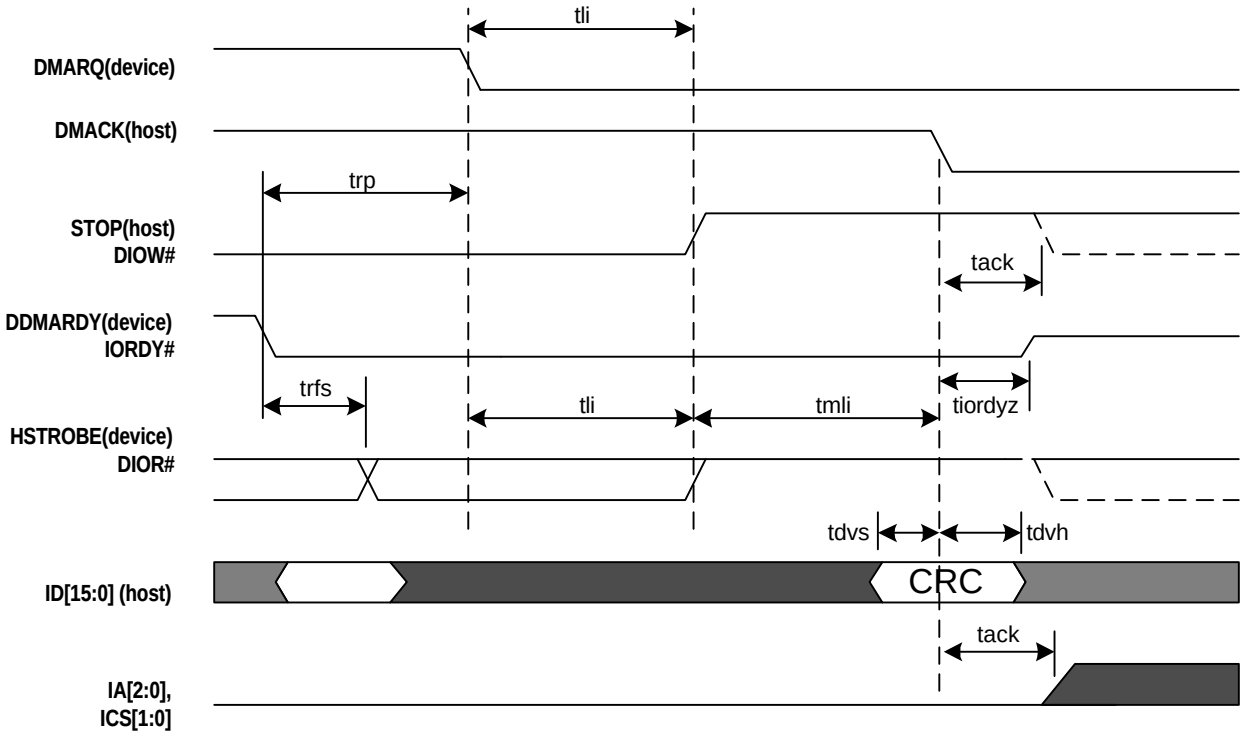


Figure 14: Device Terminating an Ultra DMA data-out burst

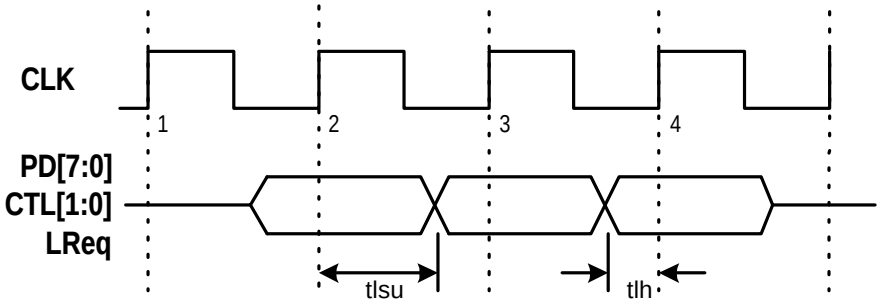


Figure 15: Phy to Link timings

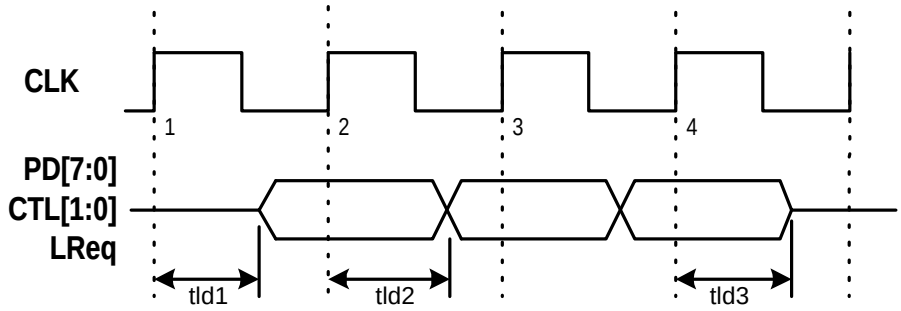


Figure 16: Link to Phy timings

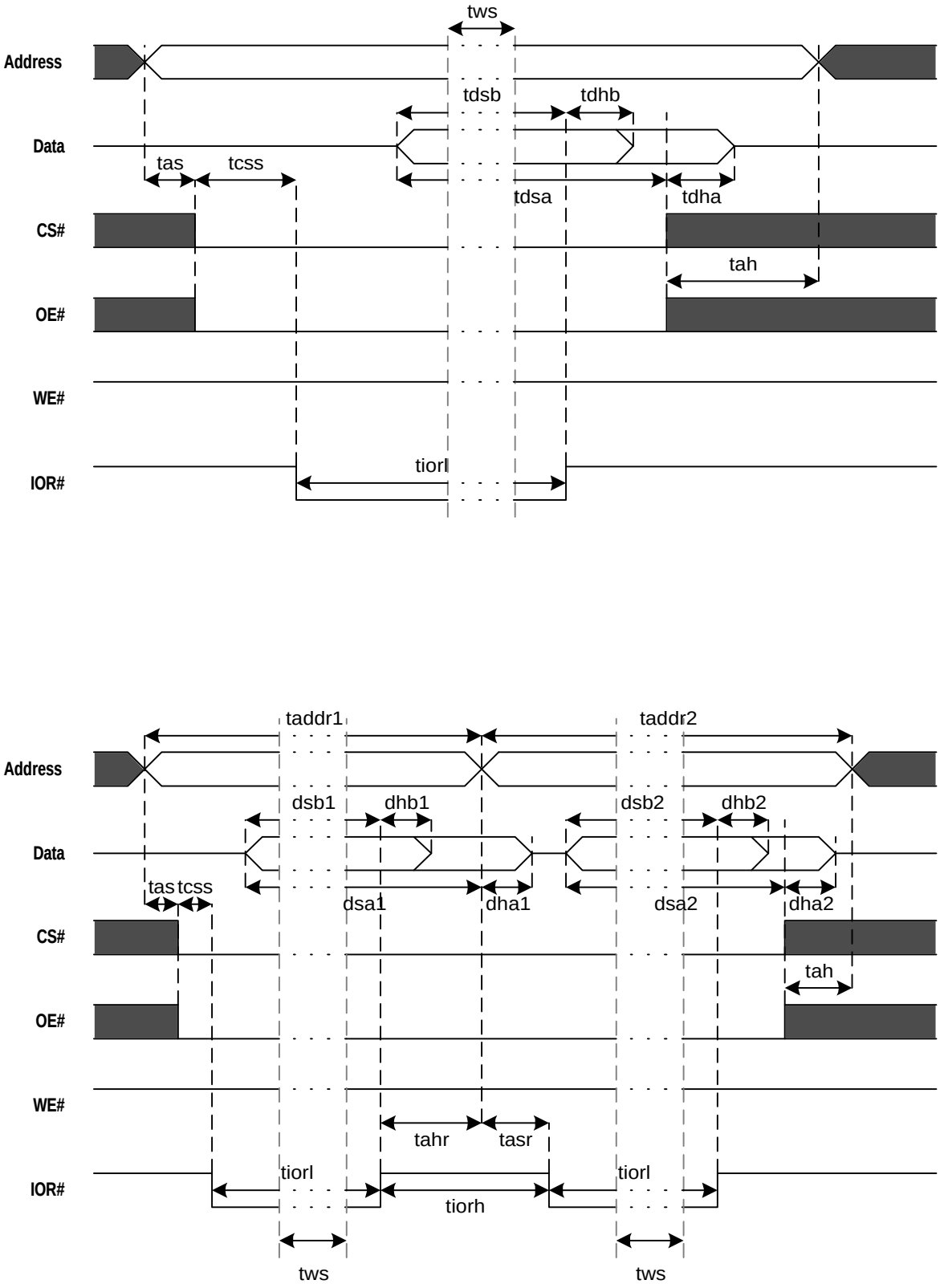


Figure 17: External Processor Bus timings

8 PACKAGE INFORMATION

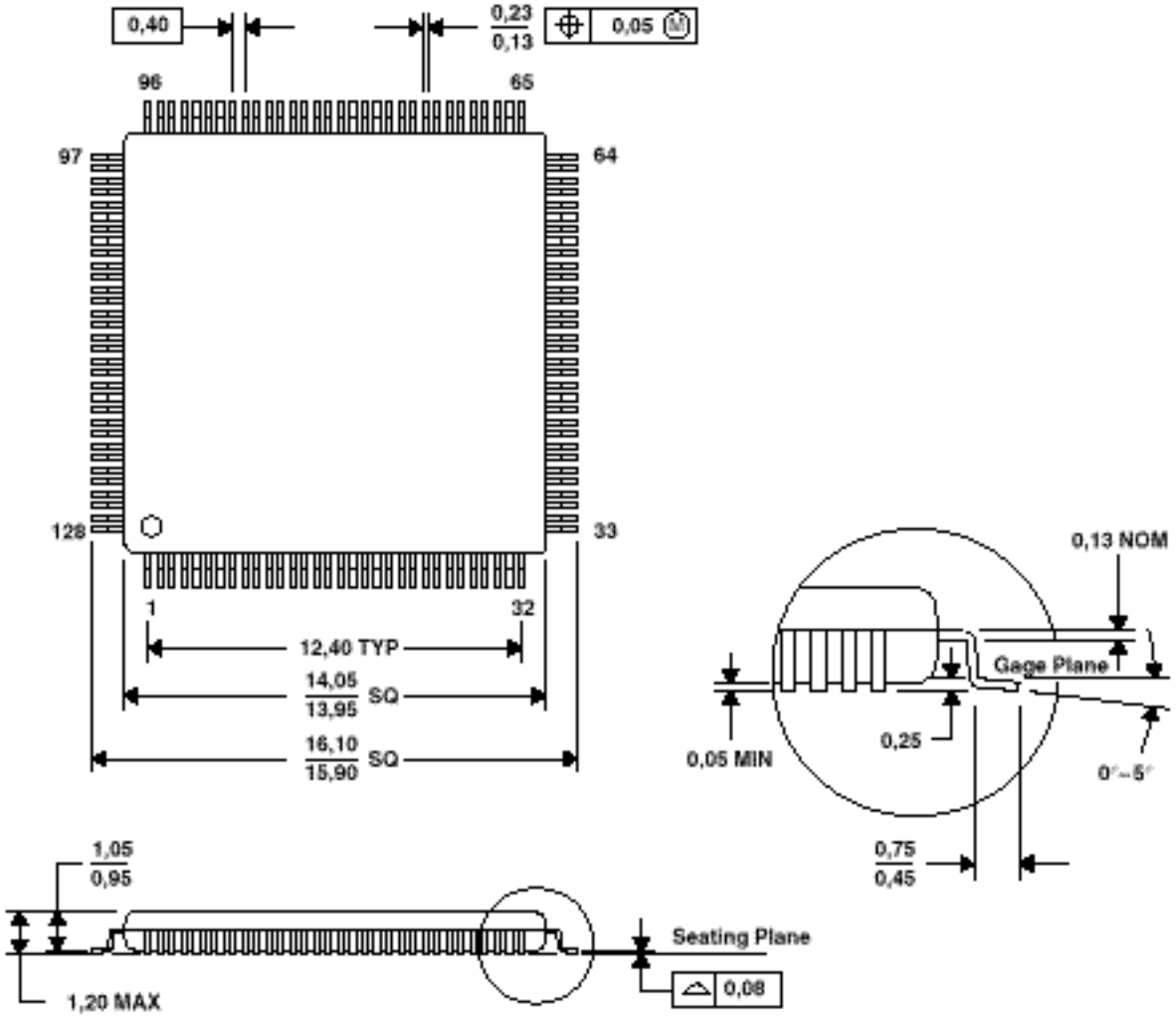
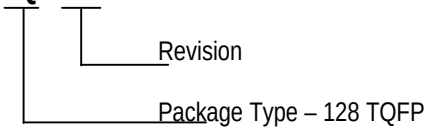


Figure 18: 128 TQFP package information

9 ORDERING INFORMATION

OXFW900-TQ - A



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