PACIFIC MONOLITHICS®

A Division of Richardson Electronics

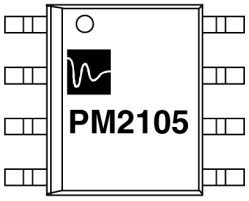
PM 2105

DATA SHEET

1 Watt RFIC Power Amplifier
800 to 2000 MHz Operation

Features

- **>1 Watt Output Power @ 5 V**
- **55% Efficiency**
- **Multiple Biasing Modes**
- **3 to 6 Volt Operation**



SO-8 Plastic Package

Applications

- **Portable Wireless Data Communications**
- **Cordless Telephone**
- **Analog and Digital Cellular**
- **PCS**

Description

The PM2105 is a low cost, high-efficiency 2-stage GaAs MMIC power amplifier for commercial wireless applications. External frequency matching enables high performance to be obtained within a 30 to 100 MHz bandwidth anywhere in the 800 to 2000 MHz frequency range. Performance characteristics of the PM2105 make it well suited for saturated or linear operation. The PM2105 has accessible bias pins that allow for either class AB or class B operation and shutdown/power control functions.

Electrical Characteristics

V_{DD}= 5.0V, V_{GG1}= -1.4V, V_{GG2}=-1.9V, T_A= +25°C, Class AB Operation, 50 Ω System

Characteristics	Symbol	Conditions	Min	Typ	Max	Units
Frequency Range	F		800		2000	MHz
Input Return Loss	RL			10.0		dB
Small Signal Gain	G			27.0		dB
Power Output (P1dB))	P_{1dB}			29.0		dBm
Power Output (Saturated)	P_{SAT}	P_{IN} = 5.0 dBm	29.5	30.5		dBm
Power Added Efficiency	PAE		45	55		%
Supply Current	I_{DD}	$P_{OUT} = P_{SAT}$		400		mA
Gate Current	I_{GG}	$P_{OUT} = P_{SAT}$		0.5	5.0	mA
Thermal Resistance	θ_{JC}	T=85°C, P_{DISS} = 1.9W		35		°C/W

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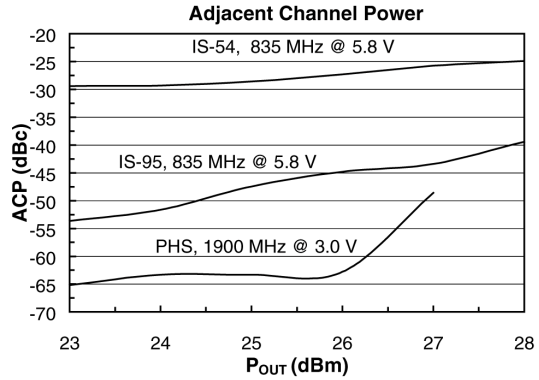
Absolute Maximum Ratings*

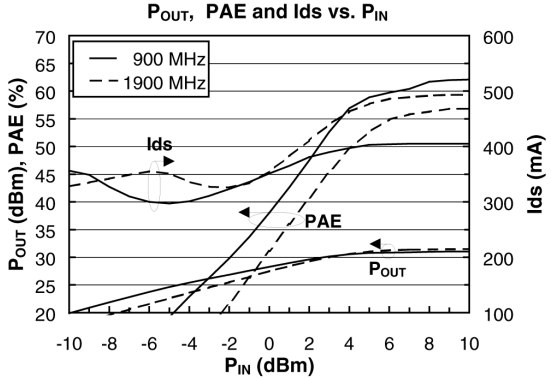
Characteristics	Symbol	Value	Units
DC Drain Voltage	V_{DD}	+9.0	V
DC Gate Voltage	V_{GG}	-5.0	V
DC Drain Current	I_{DS}	900	mA
Average Power Dissipation ($P_{DISS} = P_{DC} - P_{RF}$)	P_{DISS}	1.9	W
RF Input Power	P_{IN}	15.0	dBm
Operating Baseplate Temperature	T_{OP}	-40 to +85	°C
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

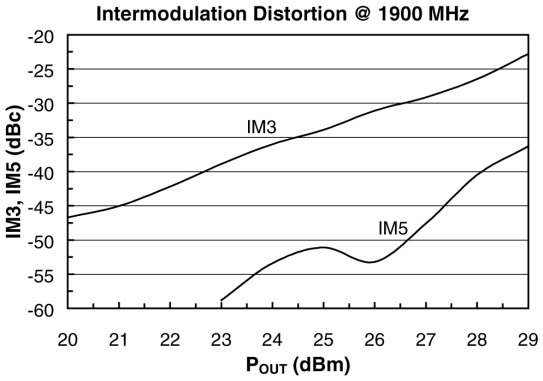
*Operation beyond the ratings for any one of these parameters may cause permanent damage to the device

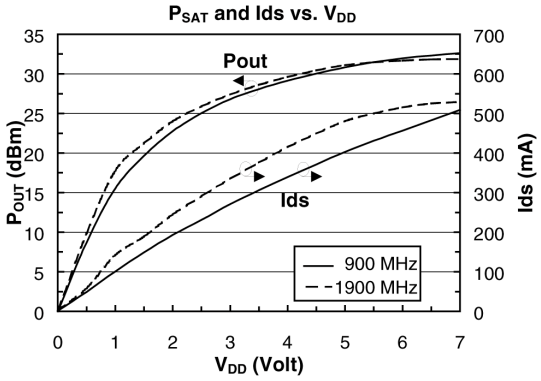
Typical Performance Characteristics

Test Conditions: T_A= +25°C, V_{DD}= 5.0V, 50Ω system, unless otherwise noted.









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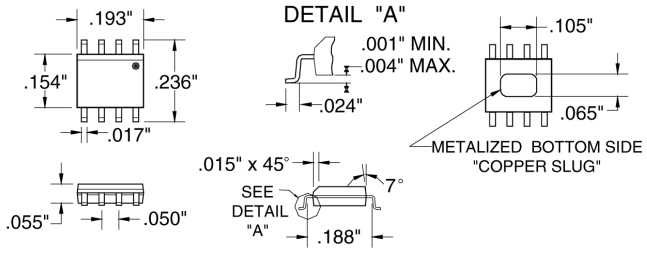
Pin Connections

Pin #	Function
1	GND
2	RF_{IN}/V_{GG1}
3	GND
4	V_{DD1}
5	V_{GG2}
6, 7	RF_{OUT}/V_{DD2}
8	GND
Base	GND

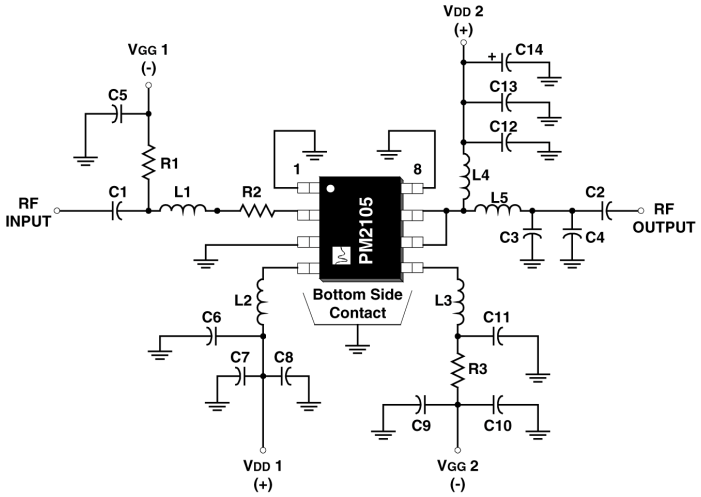
Package

SO-8 Outline Drawing



Specifications

Typical Class AB Matching Network for the PM2105 at 800-950 MHz



List of Components

Part	Value	Size
C1 ,C2	47 pF	0603
C3	2.7 pF	0603
C4	3.0 pF	0603
C8, C10, C13	1000 pF	0603
C5, C6, C11, C12	33 pF	0603
C7, C9	0.1 µF	0603
C14	6.8 µF	1206
R1	470 Ω	0603
R2	39 Ω	0603
R3	47 Ω	0603
L1	12 nH	0805
L2	4.7 nH	0805
L3	6.8 nH	0805
L4	18.5 nH	0805
L5	1.8 nH	0805

Notes:

PCB Material: 0.028 FR4, εr = 4.2
V_{DD1}, V_{DD2}: 3 TO 5 V Typical
V_{GG1}: - 1.4 V Typical
V_{GG2}: - 1.9 V Typical

800 - 950 MHz Tuning Guidelines

The PM2105 requires external input, and interstage and output matching for proper operation. Lumped element networks can be used provided that trace lengths are kept to a minimum. Input match is accomplished using L1 and R2. The lossy matching network provides added stability while maintaining a broadband repeatable return loss. The interstage match consists of L2 and L3. Output match is accomplished by L4, L5, C3 and C4. Paralleling capacitors is recommended to increase Q and self-resonant frequency. L4 must be able to withstand DC currents in excess of 900 mA for reliable operation. Extensive bypassing is recommended for linear digitally modulated applications requiring good IMD performance.

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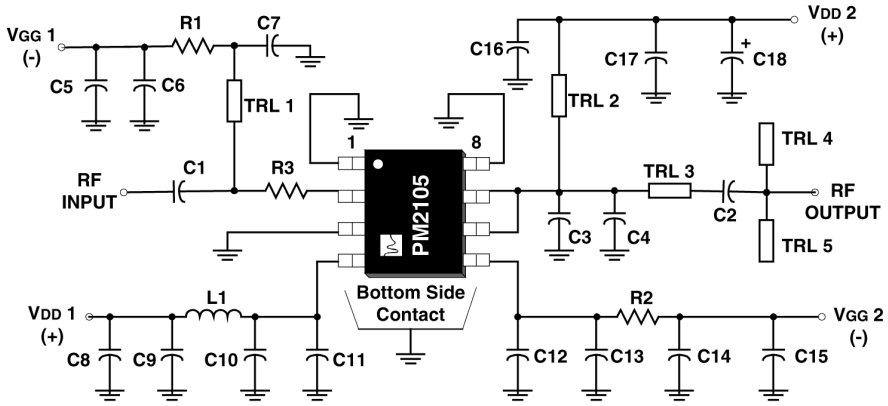
Typical Class AB Matching Network for the PM2105 at 1880-1950 MHz



List of Components

Part	Value	Size
C1, C7, C10, C11, C12, C13, C16	33 pF	0603
C2	6.8 pF	0603
C3, C4	1.5 pF	0603
C18	6.8 µF	1208
C6, C9, C14, C17	1000 pF	0603
C5, C8, C15	0.1 µF	0603
R1, R2	51 Ω	0603
R3	3.3 Ω	0603
L1	39 nH	0805

Notes:

PCB Material: 0.028 FR4, $\varepsilon r = 4.2$
$V_{DD}1$, $V_{DD}2$: 3 TO 5 V Typical
$V_{GG}1$: - 1.4 V Typical
$V_{GG}2$: - 1.9 V Typical

1880-1990 MHz Tuning Guidelines

At higher frequencies, distributed matching networks are required to achieve optimal performance. The input match is provided by TRL1 and R3. Interstage match is achieved using the package pin inductance AC coupled to ground. C3 and C4 in combination with TRL2 provide the output match. Paralleling capacitors are used to increase Q. C2, TRL3, TRL4 and TRL5 provide harmonic termination to improve efficiency. L1, R1 and R2 improve low frequency stability. Extensive bypassing is recommended for linear digitally modulated applications requiring good IMD performance. The TRL values at 1900 MHz are as follows:

TRL 1: W=.050 L=.210 (Z=50Ω, θ=21°) **TRL 3**: W=.050 L=.300 (Z=50Ω, θ=30°)
TRL 2: W=.015 L=.400 (Z=90Ω, θ=39°) **TRL 4, 5**: W=.050 L=.250 (Z=50Ω, θ=25°)

Technical Information

Power up / Power down sequence

The negative gate bias supply should always be applied before or coincident with the application of the positive drain supply voltage. Operating conditions with a DC power input exceeding 1.9W require that RF input of >0 dBm be applied prior to power-up.

The area beneath the amplifier and the associated matching networks must have a continuous ground plane or the resulting performance of the amplifier may be degraded. Terminate pins 1, 3, 8 and package base to a common ground pad. This ground pad must provide a connection to the back side of the ground plane with plated via holes. It is important to provide a good thermal path for the PM2105 since the device can dissipate up to 1.9 Watts of continuous average power.

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