

2SD973, 2SD973A

Silicon NPN epitaxial planer type

For low-frequency power amplification

Features

- Low collector to emitter saturation voltage $V_{CE(sat)}$.
- M type package allowing easy automatic and manual insertion as well as stand-alone fixing to the printed circuit board.

Absolute Maximum Ratings ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Ratings	Unit
Collector to base voltage	2SD973	30	V
	2SD973A	60	
Collector to emitter voltage	2SD973	25	V
	2SD973A	50	
Emitter to base voltage	V_{EBO}	5	V
Peak collector current	I_{CP}	1.5	A
Collector current	I_C	1	A
Collector power dissipation	P_C^*	1	W
Junction temperature	T_j	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 ~ +150	$^\circ\text{C}$

* Printed circuit board: Copper foil area of 1cm^2 or more, and the board thickness of 1.7mm for the collector portion

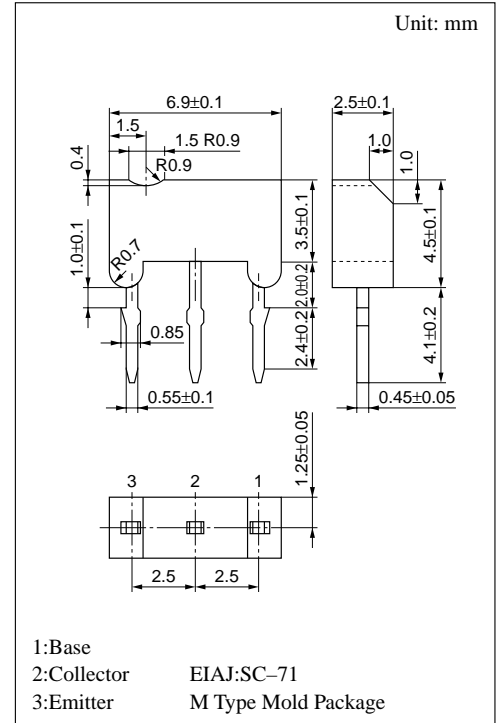
Electrical Characteristics ($T_a=25^\circ\text{C}$)

Parameter	Symbol	Conditions	min	typ	max	Unit
Collector cutoff current	I_{CBO}	$V_{CB} = 20\text{V}, I_E = 0$			0.1	μA
Collector to base voltage	2SD973	$I_C = 10\mu\text{A}, I_E = 0$	30			V
	2SD973A		60			
Collector to emitter voltage	2SD973	$I_C = 2\text{mA}, I_B = 0$	25			V
	2SD973A		50			
Emitter to base voltage	V_{EBO}	$I_E = 10\mu\text{A}, I_C = 0$	5			V
Forward current transfer ratio	h_{FE1}^{*1}	$V_{CE} = 10\text{V}, I_C = 500\text{mA}^{*2}$	85	160	340	
	h_{FE2}	$V_{CE} = 5\text{V}, I_C = 1\text{A}^{*2}$	50	100		
Collector to emitter saturation voltage	$V_{CE(sat)}$	$I_C = 500\text{mA}, I_B = 50\text{mA}^{*2}$		0.2	0.4	V
Base to emitter saturation voltage	$V_{BE(sat)}$	$I_C = 500\text{mA}, I_B = 50\text{mA}^{*2}$		0.85	1.2	V
Transition frequency	f_T	$V_{CB} = 10\text{V}, I_E = -50\text{mA}, f = 200\text{MHz}$		200		MHz
Collector output capacitance	C_{ob}	$V_{CB} = 10\text{V}, I_E = 0, f = 1\text{MHz}$		11	20	pF

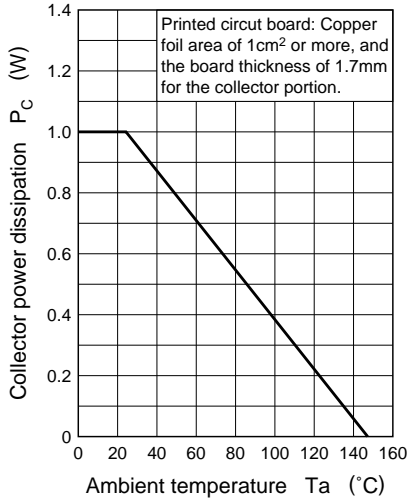
*2 Pulse measurement

*1 h_{FE1} Rank classification

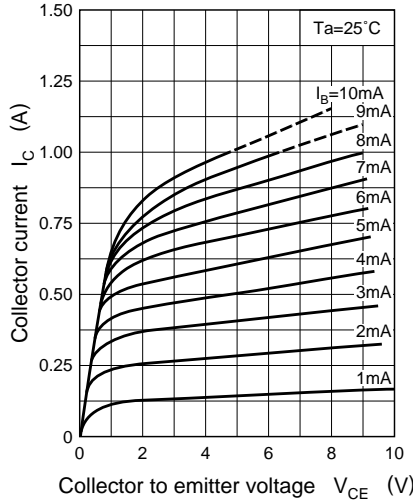
Rank	Q	R	S
h_{FE1}	85 ~ 170	120 ~ 240	170 ~ 340



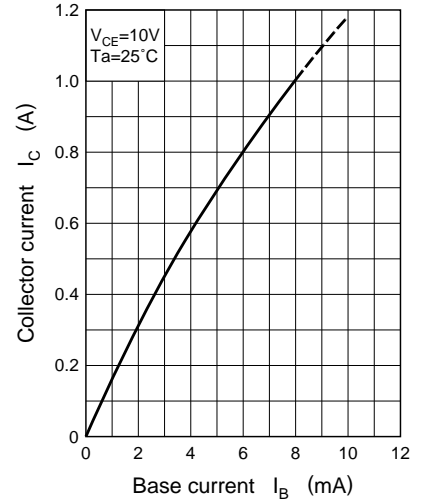
$P_C - T_a$



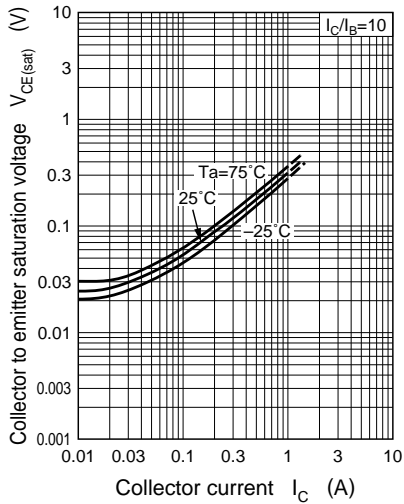
$I_C - V_{CE}$



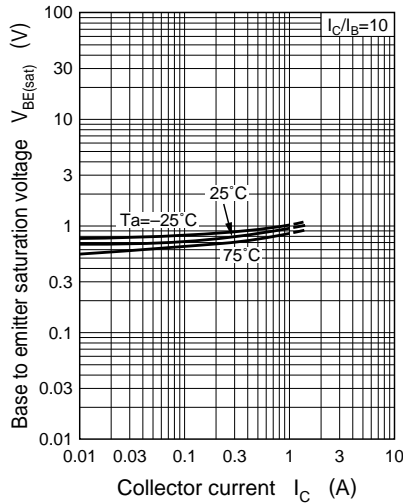
$I_C - I_B$



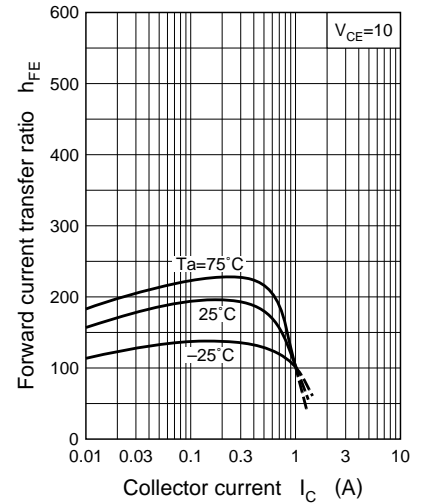
$V_{CE(sat)} - I_C$



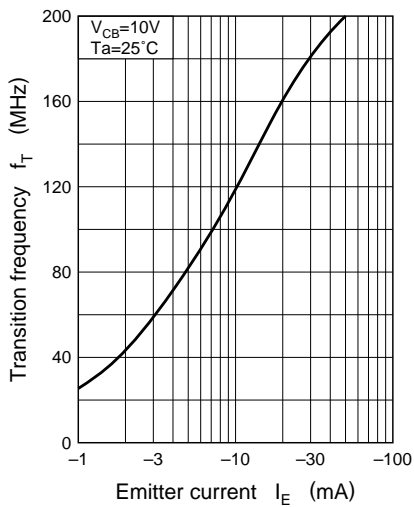
$V_{BE(sat)} - I_C$



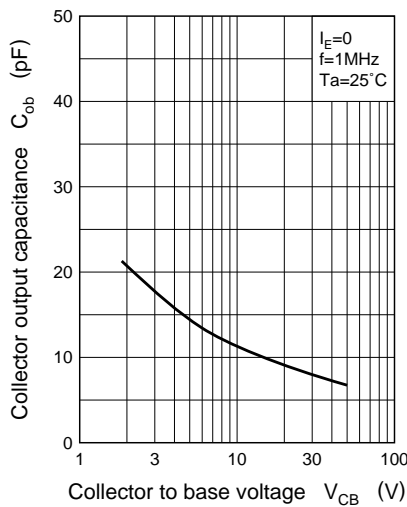
$h_{FE} - I_C$



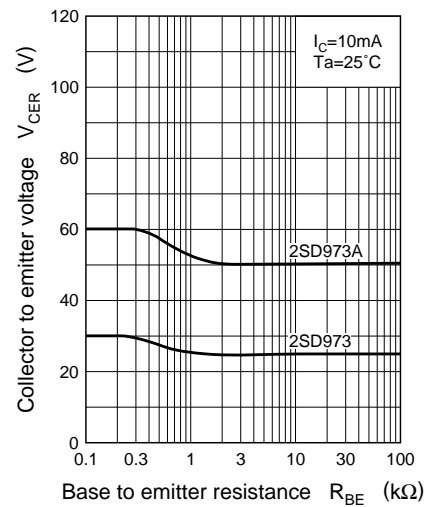
$f_T - I_E$



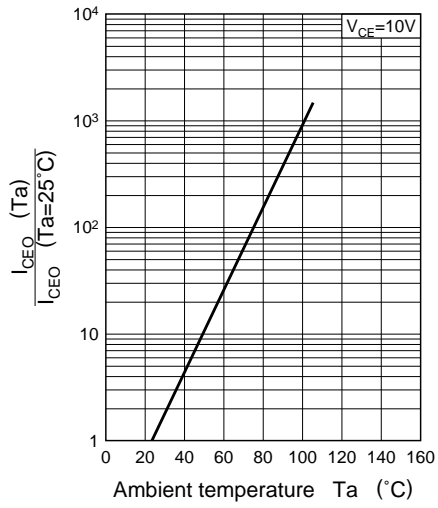
$C_{ob} - V_{CB}$



$V_{CER} - R_{BE}$



$I_{CEO} - T_a$



Area of safe operation (ASO)

