MN67603NS

NTSC Color Camera Synchronizing Signal Generator LSI

■ Overview

The MN67603NS is a CMOS LSI that generates NTSC color camera synchronizing signals as defined by the EIA RS-170A standard.

It features a built-in $4f_{SC}$ (14.31818 MHz) crystal oscillator circuit and divides that frequency to generate the horizontal synchronizing signal f_H (15.7 kHz), the vertical synchronizing signal f_V (60 Hz), and the composite synchronizing signal.

It also divides the $4f_{SC}$ clock signal frequency by four to generate the color subcarrier frequency signals SC1 and SC2.

It includes a vertical reset (VR) input pin for resetting the leading edge of the V-SERATION (3H) signal with the falling edge of the input signal.

It also includes separate clock input pins for the color subcarrier frequency signal circuits and the synchronizing signal circuits to permit synchronization with such external synchronization LSIs as the MN6761S.

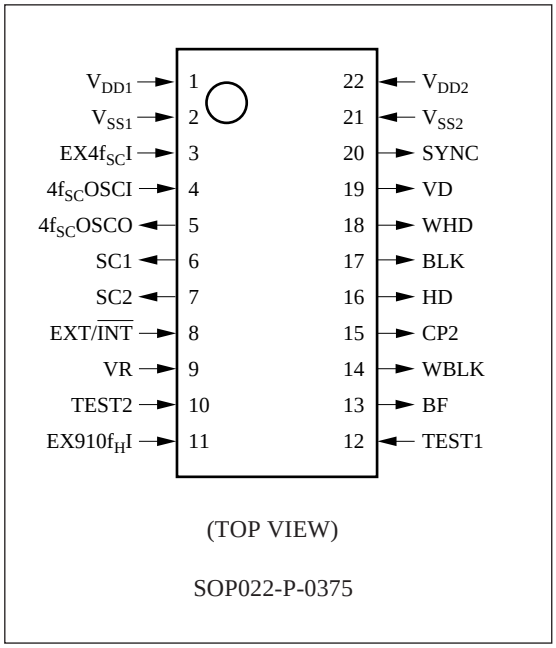
■ Features

- Power-saving CMOS synchronization signal generator (conformed to EIA RS-170A standard)
- Built-in 14.31818 MHz clock generator
- 10 signal outputs including horizontal and vertical synchronization signals and color subcarrier frequency signals

■ Applications

- Color video cameras

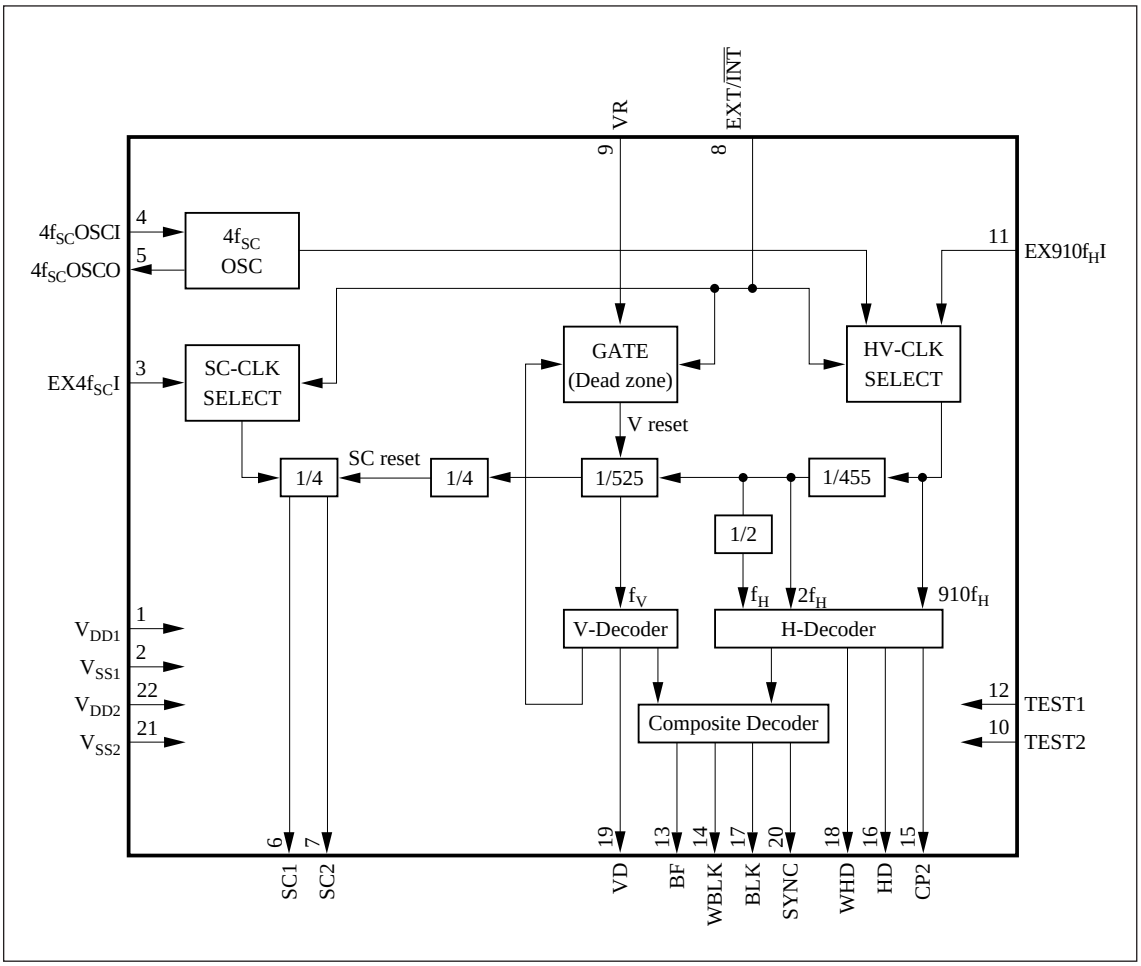
■ Pin Assignment



(TOP VIEW)

SOP022-P-0375

■ Block Diagram



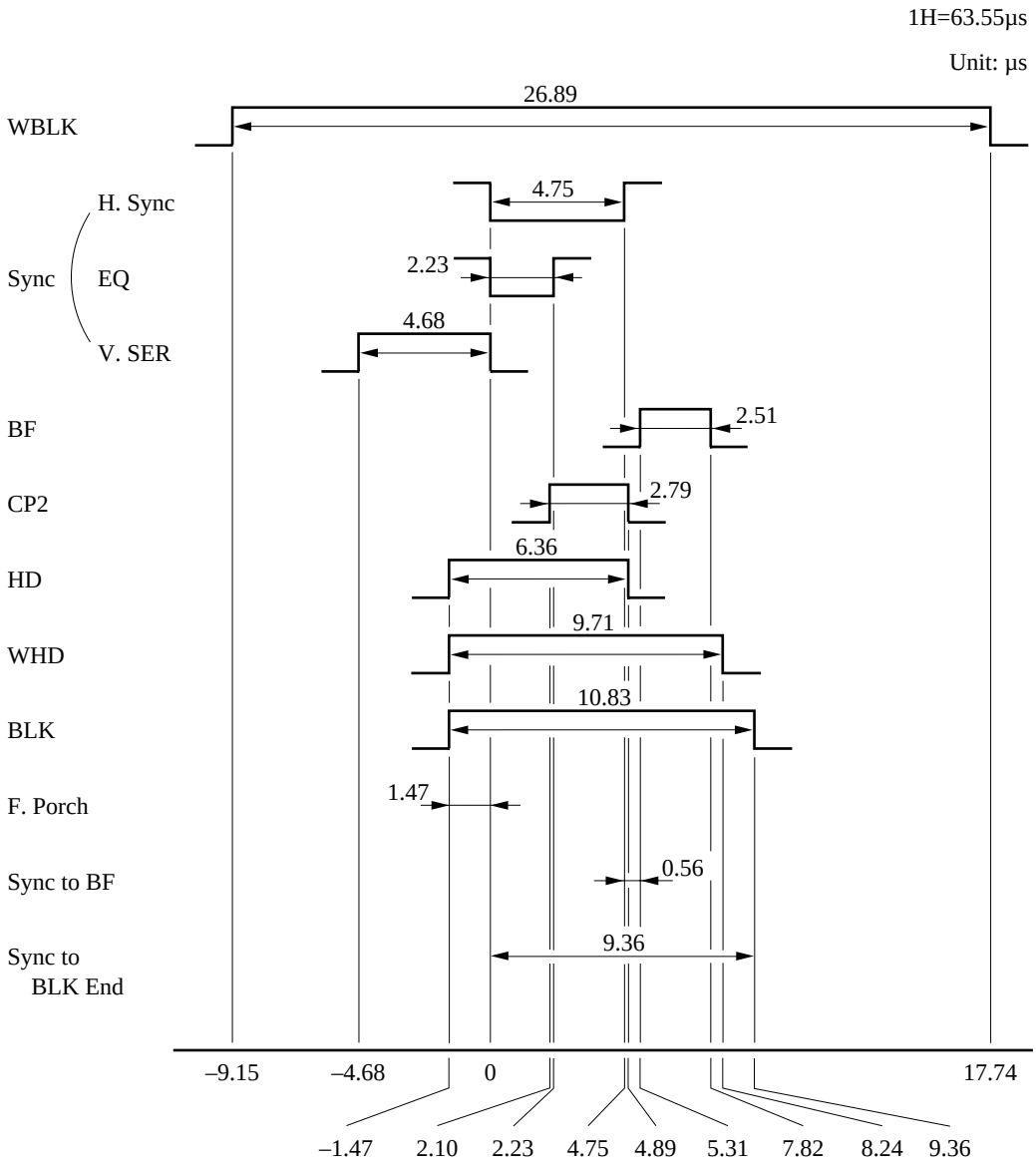
■ Pin Descriptions

Pin No.	Symbol	Pin Name	Function Description
1	V_{DD1}	Power supply	"H" level power supply (Connect this pin to +5.0 ±0.5 V.) Power supply for color subcarrier frequency signal circuits
2	V_{SS1}	Power supply	"L" level power supply (Connect this pin to 0 V.) Power supply for color subcarrier frequency signal circuits
22	V_{DD2}	Power supply	"H" level power supply (Connect this pin to +5.0 ±0.5 V.) Power supply for horizontal and vertical synchronizing signals
21	V_{SS2}	Power supply	"L" level power supply (Connect this pin to 0 V.) Power supply for horizontal and vertical synchronizing signals
4	$4f_{SC}$OSCI	Crystal oscillator input	Connect these pins to a 14.31818-MHz crystal oscillator through capacitors appropriate for V_{SS1}. "L" level input to the EXT/INT pin (which includes a built-in feedback resistor) produces oscillation; "H" level input stops it.
5	$4f_{SC}$OSCO	Crystal oscillator output	

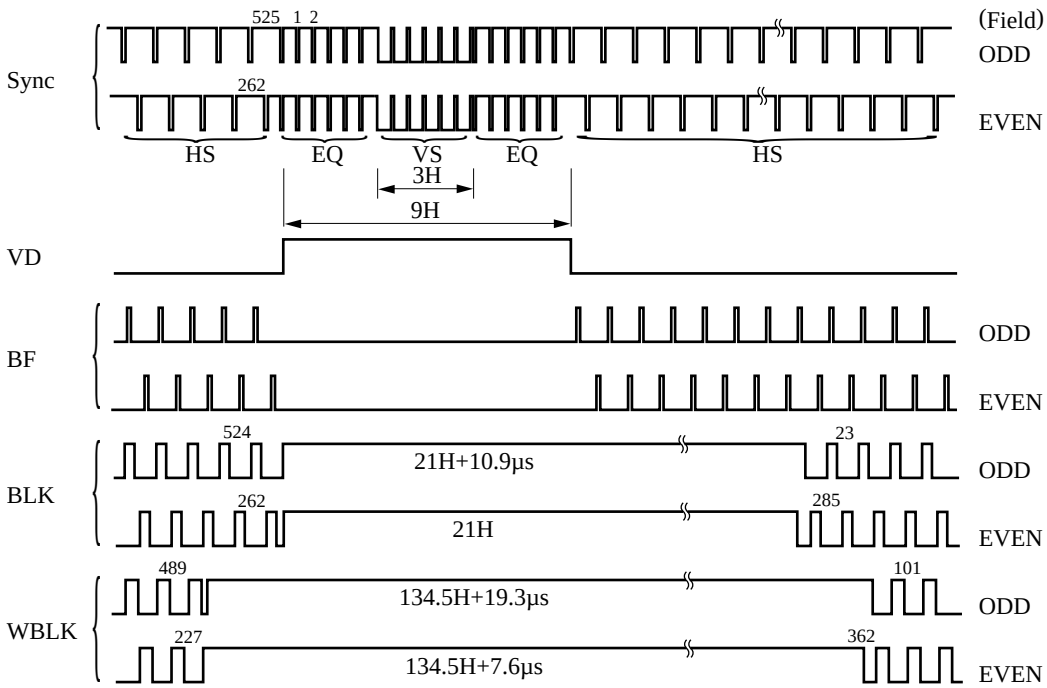
■ Pin Descriptions (continued)

Pin No.	Symbol	Pin Name	Function Description
3	EX4f_{SC}I	External clock input	Color subcarrier frequency ($4f_{SC}$ = 14.31818 MHz) input "H" level input to the EXT/$\overline{INT}$ pin enables external clock input. If this pin is not used, keep it at "L" level.
11	EX910f_{SC}I	External clock input	External 910f_H (14.31818 MHz) input for horizontal and vertical synchronizing signals "H" level input to the EXT/$\overline{INT}$ pin enables external clock input. If this pin is not used, keep it at "L" level.
8	EXT/$\overline{INT}$	External/internal synchronization switch input	This pin switches the chip between external and internal synchronization modes. "H" level input produces external synchronization; "L" level, internal synchronization.
9	VR	Vertical reset input	When this pin detects falling edge input, synchronizing signals are reset to the leading edge of the V-SERATION signal. The pin includes a built-in pull-up resistor.
12	TEST1	Test input	Test input Keep this pin at "H" level. The pin includes a built-in pull-up resistor.
10	TEST2	Test input	Test input Keep this pin at "H" level. The pin includes a built-in pull-up resistor.
6	SC1	f_{SC} (R-Y) output	Color subcarrier frequency signal (3.58 MHz) formed by dividing the crystal oscillator signal ($4f_{SC}$) by four.
7	SC2	f_{SC} (B-Y) output	Color subcarrier frequency signal (3.58 MHz) formed by dividing the crystal oscillator signal ($4f_{SC}$) by four. This signal lags SC1 by 90°.
20	SYNC	Composite synchronizing signal output	Composite synchronizing signal
19	VD	Vertical drive output	Vertical drive output pin (9H)
18	WHD	Wide HD output	Wide HD signal Preblanking signal with pulse width of 9.71 µs
17	BLK	Composite blanking signal output	Composite blanking signal This signal provides a horizontal blanking interval of 10.83 µs and a vertical blanking interval of 21H.
16	HD	Horizontal drive output	Horizontal drive output signal
15	CP2	Clamp pulse output	Clamp pulses for luminance and color difference signals Horizontal deflection start pulses
14	WBLK	Composite wide blanking output	Composite wide blanking signal This signal provides a horizontal blanking interval of 26.89 µs and a vertical blanking interval of 134.5H.
13	BF	Burst flag output	Gate signal for color subcarrier frequencies The pulse width is 2.51 µs with the vertical interval (9H) dropped out.

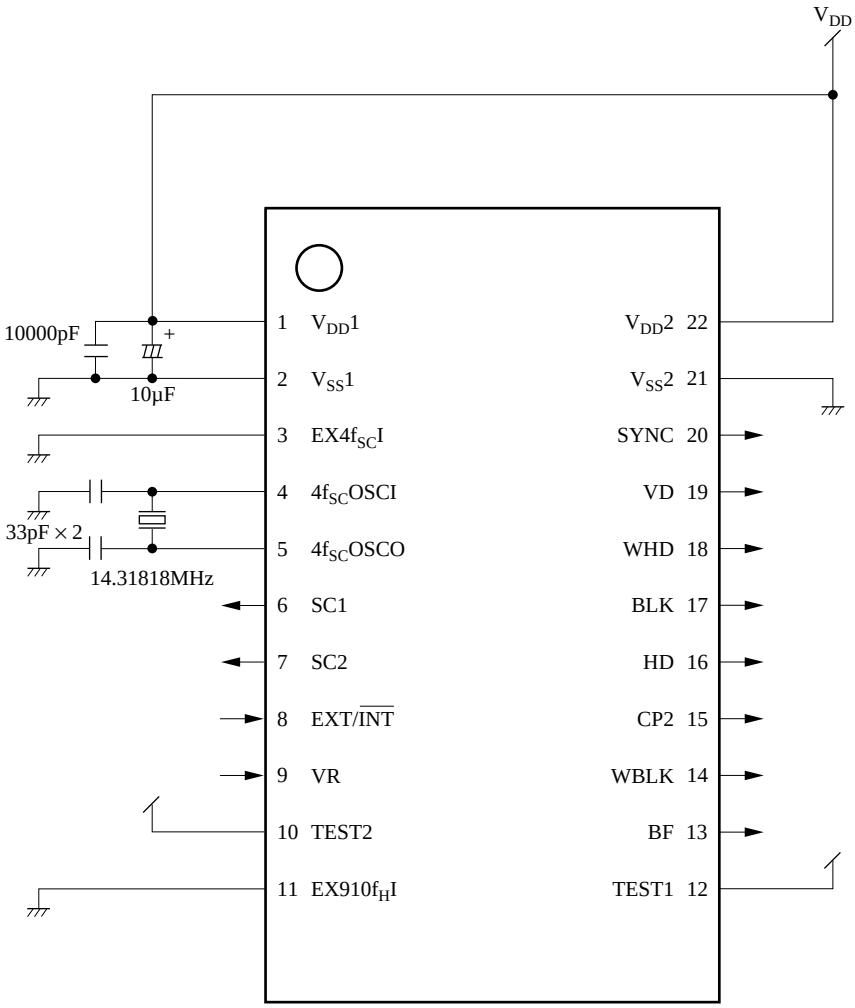
■ H Decoder Pulse Timing Diagram



■ Pulse Timing Diagram for Composite and Vertical Synchronizing Signals



■ Application Circuit Example



■ Package Dimensions (Unit: mm)

SOP022-P-0375