MN6460A

A/D Converter for Digital Audio Equipment

■ Overview

The MN6460A is a 16-bit CMOS analog-to-digital converter designed especially for PCM digital audio equipment. It features a built-in digital filter. It uses noise shaping to convert an analog signal to a 16-bit digital signal.

Incorporating digital filter permits simplification of the analog filter that normally precedes the A/D converter, thus greatly reducing the power consumption of the overall A/D conversion system.

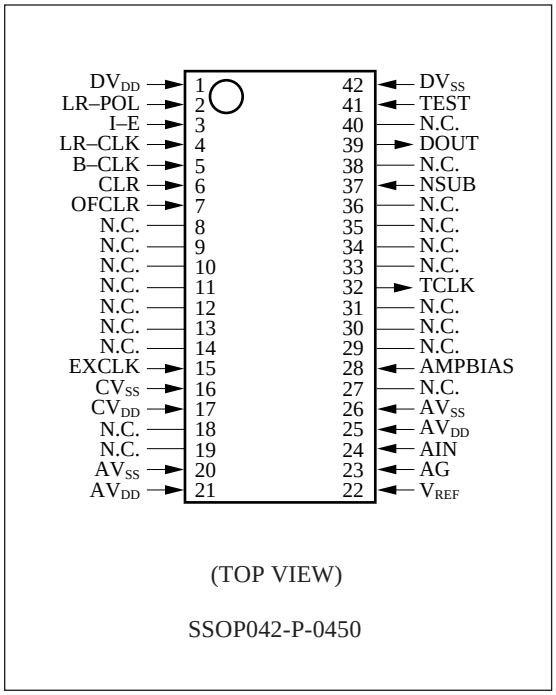
■ Features

- Analog and digital-mixed CMOS LSI
- A/D conversion using noise shaping
- 64-fold oversampling
- Built-in digital filter
- Sample and hold circuit is unnecessary
- Serial output using two's complement code
- Built-in offset compensation circuit
- Built-in overflow limiter
- Single 5-volt power supply (when V_{REF} =1.5 V and AG=2.5 V)

■ Applications

- DAT players and other digital audio equipment

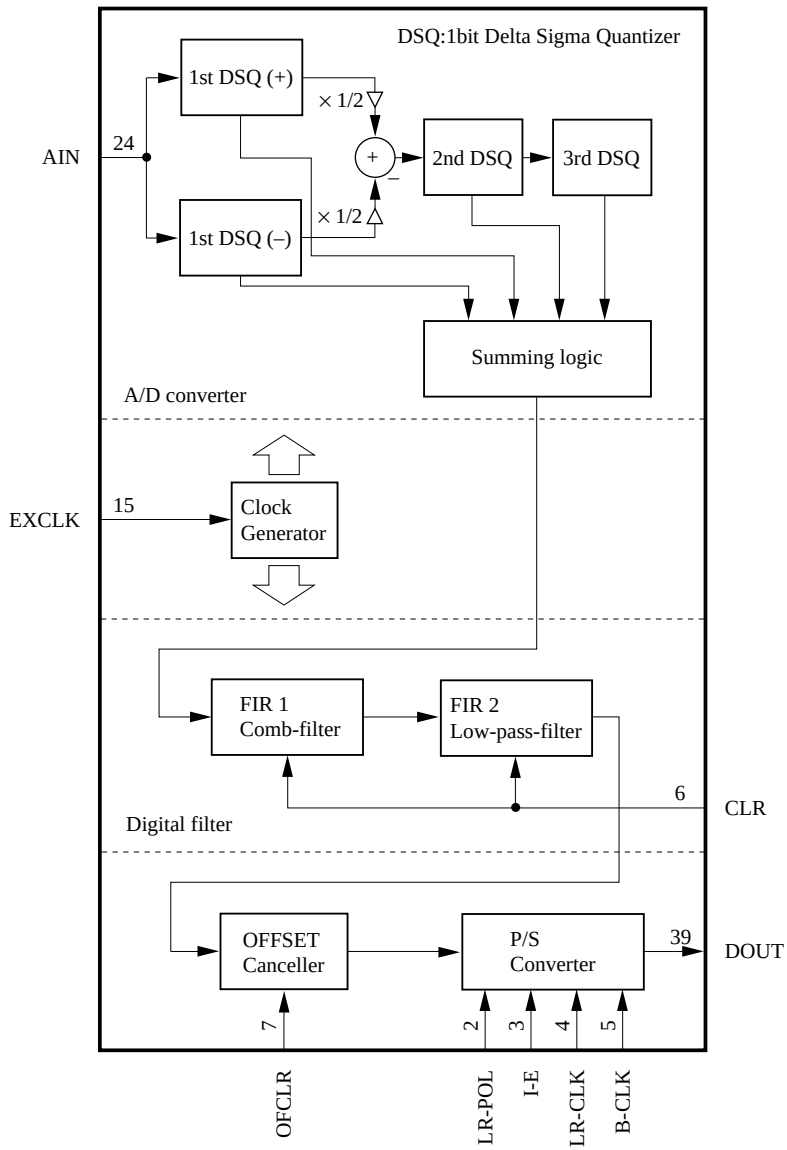
■ Pin Assignment



(TOP VIEW)

SSOP042-P-0450

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Description
1	DV_{DD}	Power supply pin for digital circuits (+5 V)
2	LR-POL	Channel selection pin for stereo operation using two chips. "H" level: right channel. "L" level: left channel.
3	I-E	Format selection pin. "L" level: signal processing LSI format. "H" level: I^2S format.
4	LR-CLK	LRCLK input pin (for stereo operation) If LR-POL is at "H" level, "H" level: right channel data output. "L" level, high-impedance state. If LR-POL is at "L" level, "H" level: high-impedance state. "L" level, left channel data output.
5	B-CLK	Bit transfer command input (At falling edge signal, a bit transfered)
6	CLR	Clear pin. Active high. Driving this pin at "H" level clears internal data. Always this internal data is cleared by feeding a positive pulse to this pin after applying the power.
7	OFCLR	Driving this pin at "L" level enables the offset clear circuit.
8	N.C.	No connection (Leave this pin open.)
9	N.C.	No connection (Leave this pin open.)
10	N.C.	No connection (Leave this pin open.)
11	N.C.	No connection (Leave this pin open.)
12	N.C.	No connection (Leave this pin open.)
13	N.C.	No connection (Leave this pin open.)
14	N.C.	No connection (Leave this pin open.)
15	EXCLK	512 f_s input pin
16	CV_{SS}	Ground pin for digital circuits
17	CV_{DD}	Power supply pin for digital circuits (+5 V)
18	N.C.	No connection (Leave this pin open.)
19	N.C.	No connection (Leave this pin open.)
20	AV_{SS}	Ground pin for analog circuits
21	AV_{DD}	Power supply pin for analog circuits (+5 V)
22	V_{REF}	Analog circuit reference voltage input pin (+1.5 V)
23	AG	Analog ground input pin (+2.5 V)
24	AIN	Analog input pin
25	AV_{DD}	Power supply pin for analog circuits (+5 V)
26	AV_{SS}	Ground pin for analog circuits
27	N.C.	No connection (Leave this pin open.)
28	AMPBIAS	Bias voltage adjustment pin for operational amplifier (Keep this at the same voltage as the AG pin.)
29	N.C.	No connection (Leave this pin open.)
30	N.C.	No connection (Leave this pin open.)
31	N.C.	No connection (Leave this pin open.)

■ Pin Descriptions (continued)

Pin No.	Symbol	Function Description
32	TCLK	LSI test clock output pin. (Leave this pin open.)
33	N.C.	No connection (Leave this pin open.)
34	N.C.	No connection (Leave this pin open.)
35	N.C.	No connection (Leave this pin open.)
36	N.C.	No connection (Leave this pin open.)
37	NSUB	Connect this pin to AV_{DD}.
38	N.C.	No connection (Leave this pin open.)
39	DOUT	Serial output pin. Two's complement. MSB first.
40	N.C.	No connection (Leave this pin open.)
41	TEST	LSI test pin. (Connect this pin to DV_{DD}.)
42	DV_{SS}	Ground pin for digital circuits

■ Electrical Characteristics

Conversion Characteristics

DV_{DD}=5.0V, AV_{DD}=5.0V, V_{AG}=2.5V, V_{REF}=1.5V, f_{EXCLK}=24.576MHz, Ta=25˚C

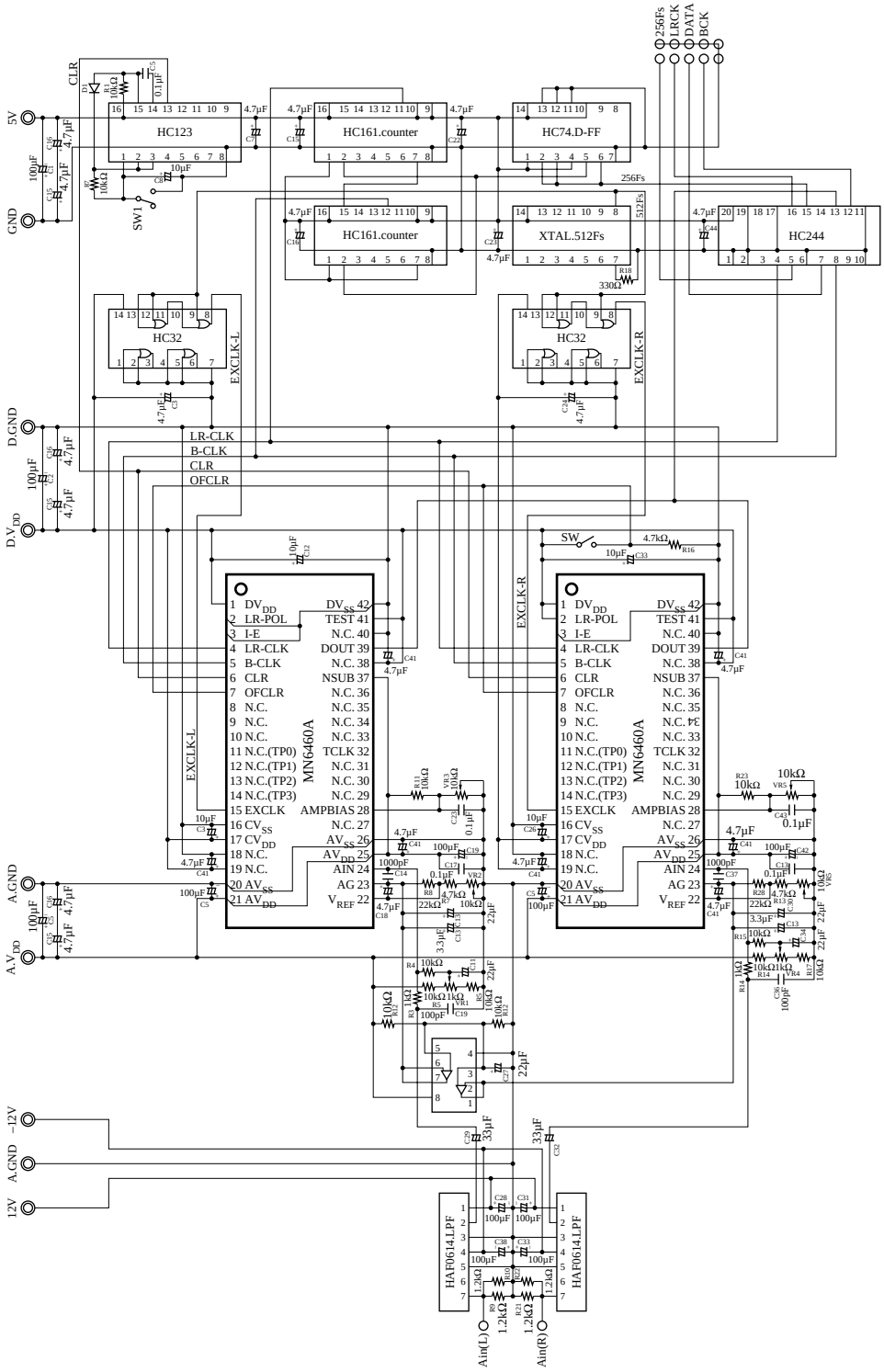
Parameter	Symbol	Test Condition	min	typ	max	Unit
Signal-to-noise ratio	S/N	EIAJ (1kHz)	85	90		dB
Dynamic range	D.R.	EIAJ (1KHZ)	85	90		dB
Total harmonic distortion	THD+N	EIAJ (1kHz)		0.005	0.010	%

Specifications for DC Offset

An A/D converter usually does not produce digital zero output from analog zero input because the operational amplifier inside has an offset. The MN6460A, however, has circuitry for correcting this. The shipping inspection enables this offset correction circuit and confirms that the DC offset is within the lower four bits.

Parameter	Symbol	Test Condition	min	typ	max	Unit
DC offset		OFCLR="H"			±20	mV
		OFCLR="L"			±0.6	mV

■ Application Circuit Example



■ Package Dimensions (Unit: mm)

SSOP042-P-0450