MN662724RPE

Signal Processing LSI for CD Players

■ Overview

The MN662724RPE is a CD signal processing LSI that, on a single chip, combines an optics servo for the CD player (focus, tracking, and traverse servos), digital signal processing (EFM demodulation and error correction), and digital servo processing for the spindle motor.

■ Features

(Optics servo)

- Focus, tracking, and traverse servos
- Automatic adjustment functions for FO/TR gain, FO/TR offset, and FO/TR balance
- Built-in D/A converter for drive voltage output
- Built-in dropout countermeasures
- Anti-shock functions
- Built-in track cross counter

(Digital signal processing)

- Built-in DSL and PLL
- Frame synchronization detection, holding, and insertion
- Subcode data processing
  - Q data CRC check
  - Built-in Q data register
- CIRC error detection and correction
  - C1 decoder: duplex error correction
  - C2 decoder: triplex error correction
  - Built-in 16-K bits of RAM for de-interleaving
- Audio data interpolation
  - Average, hold of previous values
  - Soft muting
  - Digital attenuation (256 levels)
- Software attenuation (256 levels)
- Auto cue detection function
- Digital audio interface (EIAJ format)
- Two audio data serial interfaces:
  - One switchable between bit rates of 64 f_s and 48 f_s; the other fixed at 48 f_s.

(Spindle motor servo)

- CLV digital servo
- Switchable servo gain

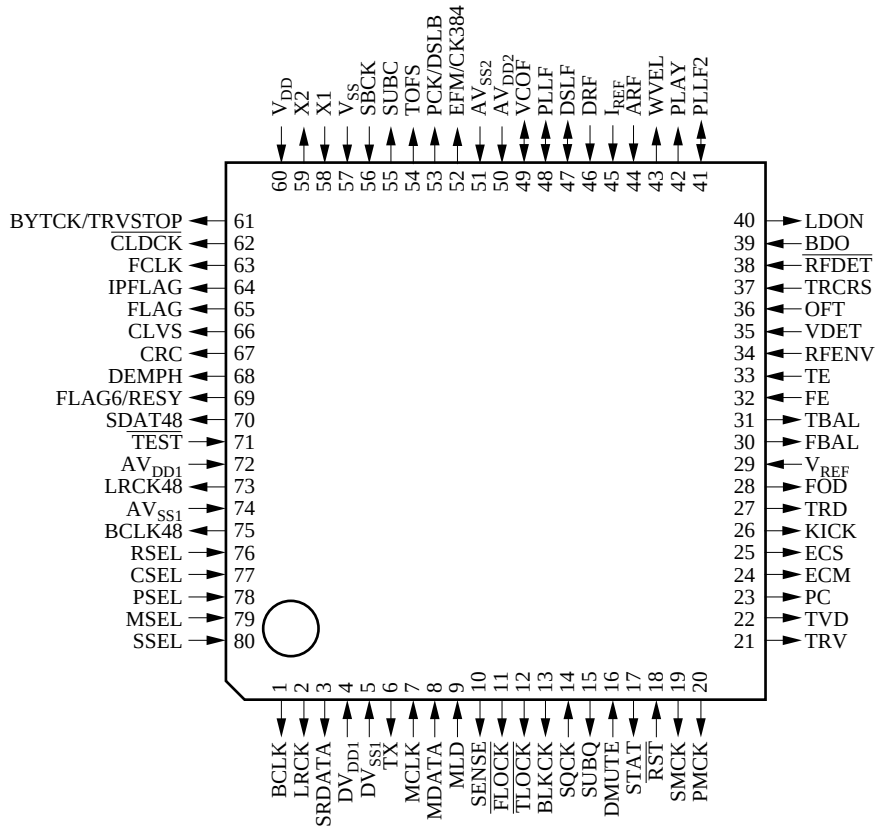
(Other)

- Built-in playback pitch control function (normal speed only)(±13%)
- Built-in support for jitter-free disc rotation synchronization playback
- Oscillator shutdown mode
- Power management mode
- Operating voltage 4.5 to 5.5V

■ Applications

- CD Players

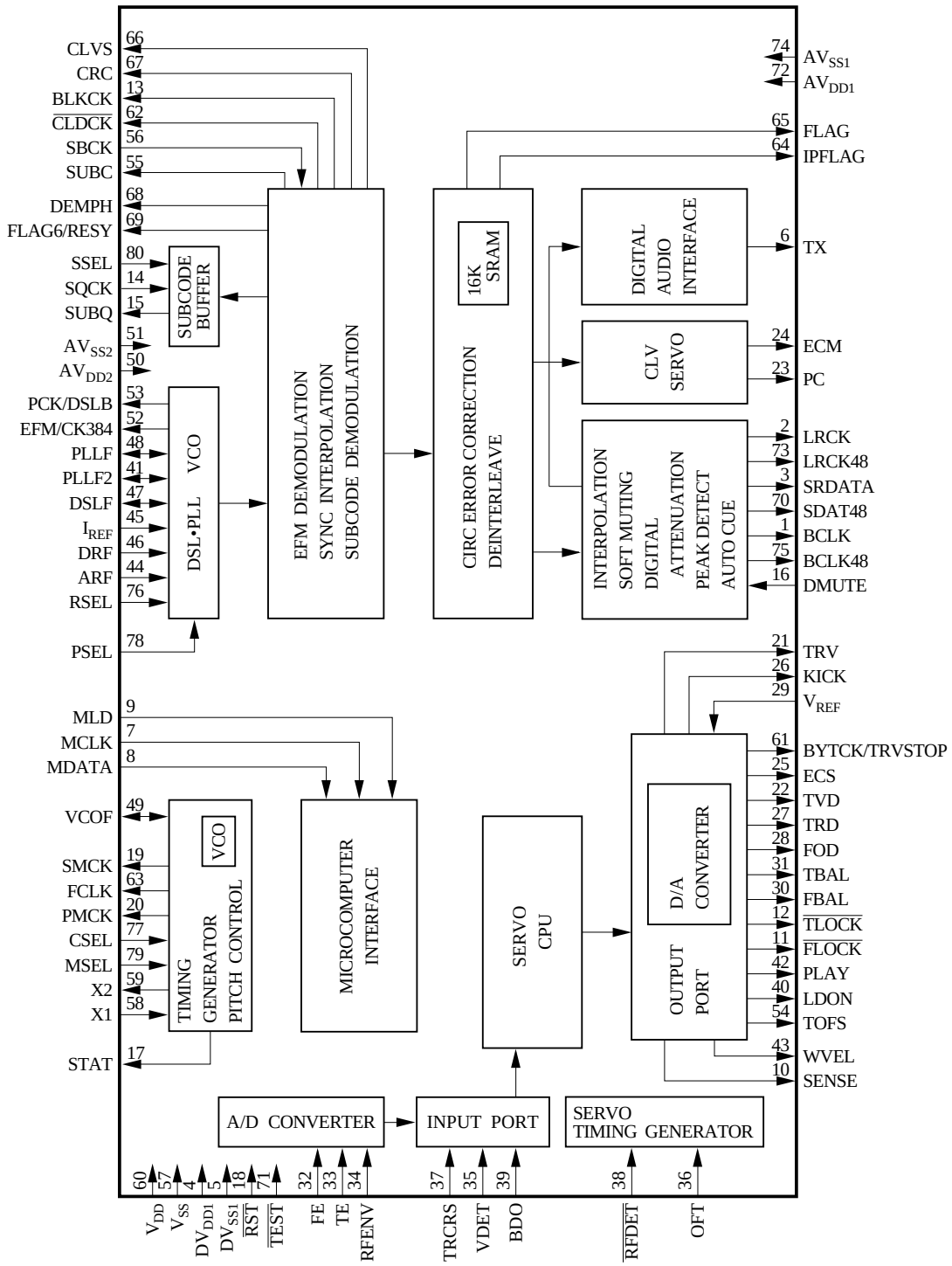
■ Pin Assignment



(TOP VIEW)

QFS080-P-1414

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	I/O	Function Description
1	BCLK	O	SRDATA bit clock output.
2	LRCK	O	Left/right channel discrimination signal output.
3	SRDATA	O	Serial data output.
4	DV_{DD1}	I	Power supply for digital circuits.
5	DV_{SS1}	I	Ground for digital circuits.
6	TX	O	Digital audio interface output signal.
7	MCLK	I	Microcomputer command clock input. (Data is latched at rising edge.)
8	MDATA	I	Microcomputer command data input.
9	MLD	I	Microcomputer command load signal input. "L" level: load.
10	SENSE	O	Sense signal output. (OFT, FESL, NACEND, NAJEND, SFG, and NWTEND)
11	$\overline{\text{FLOCK}}$	O	Focus servo pull-in signal. "L" level: pull-in state.
12	$\overline{\text{TLOCK}}$	O	Tracking servo pull-in signal. "L" level: pull-in state.
13	BLKCK	O	Subcode block clock signal (f_{BLKCK}=75Hz)
14	SQCK	I	External clock input for subcode Q register
15	SUBQ	O	Subcode Q data output
16	DMUTE	I	Muting input. (Effective only for an output bit rate of 64 f_s) "H" level: muting.
17	STAT	O	Status signal. (CRC, CUE, CLVS, TTSTOP, FCLV, SQOK, FLAG6, SENSE, $\overline{\text{FLOCK}}$, and $\overline{\text{TLOCK}}$)
18	$\overline{\text{RST}}$	I	Reset input. "L" level: reset.
19	SMCK	O	If MSEL is "H" level, 8.4672 MHz clock signal is outputted. If MSEL is "L" level, 4.2336 MHz clock signal is outputted.
20	PMCK	O	88.2kHz clock signal output.
21	TRV	O	Traverse forced feed output. (tristate)
22	TVD	O	Traverse drive output.
23	PC	O	Spindle motor ON signal. "L" level: ON (default).
24	ECM	O	Spindle motor drive signal (forced mode output). (tristate)
25	ECS	O	Spindle motor drive signal (servo error signal output)
26	KICK	O	Kick pulse output. (tristate)
27	TRD	O	Tracking drive output.
28	FOD	O	Focus drive output.
29	V_{REF}	I	Reference voltage for D/A output (TVD, ECS, TRD, FOD, FBAL, TBAL, and TOFS).
30	FBAL	O	Focus balance adjustment output.
31	TBAL	O	Tracking balance adjustment output.
32	FE	I	Focus error signal input. (analog input)
33	TE	I	Tracking error signal input. (analog input)
34	RFENV	I	RF envelope signal input. (analog input)
35	VDET	I	Vibration detection signal input. "H" level: vibration detected.
36	OFT	I	Offtrack signal input. "H" level: offtrack.
37	TRCRS	I	Track cross signal input. (analog input)

■ Pins Descriptions (continued)

Pin No.	Symbol	I/O	Function Description
38	$\overline{\text{RFDET}}$	I	RF detection signal input. "L" level: detected.
39	BDO	I	Dropout signal input. "H" level: dropout
40	LDON	O	Laser ON signal output. "H" level: ON.
41	PLLF2	I/O	PLL loop-filter characteristic switching pin.
42	PLAY	O	Play signal output. "H" level: play.
43	WVEL	O	Double-speed status signal output. "H" level: double-speed.
44	ARF	I	RF signal input.
45	I_{REF}	I	Reference current input pin
46	DRF	I	DSL bias pin.
47	DSLF	I/O	DSL loop-filter pin.
48	PLLF	I/O	PLL loop-filter pin.
49	VCOF	I/O	VCO loop-filter pin.
50	AV_{DD2}	I	Power supply for analog circuits (DSL, PLL, D/A converter output, and A/D converter).
51	AV_{SS2}	I	Ground for analog circuits (DSL, PLL, D/A converter output, and A/D converter).
52	EFM or CK384	O	EFM signal output. • EFM output. • Crystal oscillator 16.9344 MHz output. • 384 f_s output from signal processing block. (During variable-pitch operation, this is the VCO clock.) Commands permit switching among the above three outputs.
53	PCK or DSLB	O	Clock for PLL or DSL balance output. f_{PCK}=4.3218MHz
54	TOFS	O	Tracking offset adjustment output.
55	SUBC	O	Subcode serial output.
56	SBCK	I	Clock input for subcode serial output.
57	V_{SS}	I	Ground for oscillator circuit.
58	X1	I	Crystal oscillator circuit input pin. f=16.9344MHz, 33.8688MHz
59	X2	O	Crystal oscillator circuit output pin. f=16.9344MHz, 33.8688MHz
60	V_{DD}	I	Oscillator circuit power supply.
61	BYTCK or TRVSTOP	O	During default operation, byte clock signal output. During command execution, traverse stop signal output. "H" level: stop mode.
62	$\overline{\text{CLDCK}}$	O	Subcode frame clock signal output pin. (f_{CLDCK}=7.35kHz)
63	FCLK	O	Crystal frame clock signal output. (f_{FCLK}=7.35kHz)
64	IPFLAG	O	Interpolation flag signal output. "H" level: interpolation.
65	FLAG	O	Flag signal output.
66	CLVS	O	Spindle servo phase synchronization signal output. "H" level: CLV. "L" level: rough servo.
67	CRC	O	Subcode CRC check result output. "H" level: OK. "L" level: no good.
68	DEMPH	O	De-emphasis detection signal output. "H" level: on.

■ Pin Descriptions (continued)

Pin No.	Symbol	I/O	Function description
69	FLAG6 or RESY	O	During default operation, FLAG6 output, that is the resetting signal for the address of RAM used to de-interleave error correction data. "L" level: address reset. During command execution, RESY output, that is the frame resynchronization signal. "H" level: synchronized. "L" level: out of sync.
70	SDAT48	O	Serial data output for bit rate 48 f_s.
71	$\overline{\text{TEST}}$	I	Test pin. Keep this at "H" level.
72	AV_{DD1}	I	Power supply for digital circuits.
73	LRCK48	O	Left/right channel discrimination signal output for bit rate 48 f_s.
74	AV_{SS1}	I	Ground for digital circuits.
75	BCLK48	O	Bit clock output for bit rate 48 f_s.
76	RSEL	I	RF signal polarity selection pin. "H" level: bright level is "H." "L" level: bright level is "L."
77	CSEL	I	Crystal oscillator frequency specification pin. "H" level: 33.8688 MHz. "L" level: 16.9344 MHz
78	PSEL	I	Test pin. Keep this at "L" level.
79	MSEL	I	SMCK pin output. SMCK frequency selection pin. "H" level: 8.4672 MHz. "L" level: 4.2336 MHz.
80	SSEL	I	SUBQ pin output mode selection pin. "H" level: Buffered Q code mode. "L" level: CLDCK synchronization mode.

■ Package Dimensions (Unit: mm)

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