MN65742

6-Bit, 2-Channel CMOS A/D Converter

■ Overview

The MN65742 is a 6-bit, 2-channel CMOS analog-to-digital converter. It uses a totally parallel structure based on differential comparators to achieve high-speed operation.

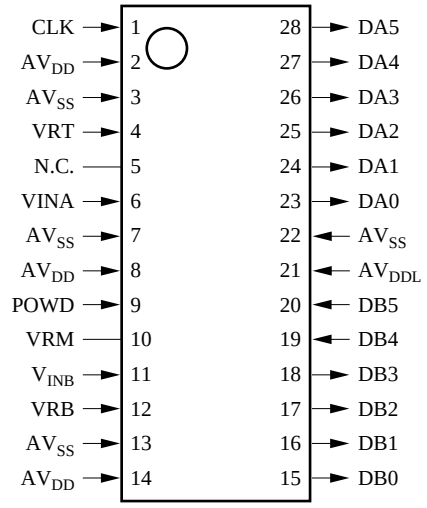
■ Features

- Resolution: 6 bits
- Maximum conversion rate: 60 MSPS (min.)
- Linearity error: ±1.3 LSB (typ.)
- Differential linearity error: ±1.3 LSB (typ.)
- Analog input voltage level:
  1.5 V_{p-p} (typ.) (1.0 to 2.5 V)
- Power supply voltage: 5.0 ±0.25 V
  3.0 to 5.25 V (power supply for output pins)
- Power consumption: 250 mW (typ.) (F_C= 60 MSPS, not including reference current)

■ Applications

- Digital satellite broadcasting receivers
- Digital video equipment
- Multimedia equipment
- Communications equipment

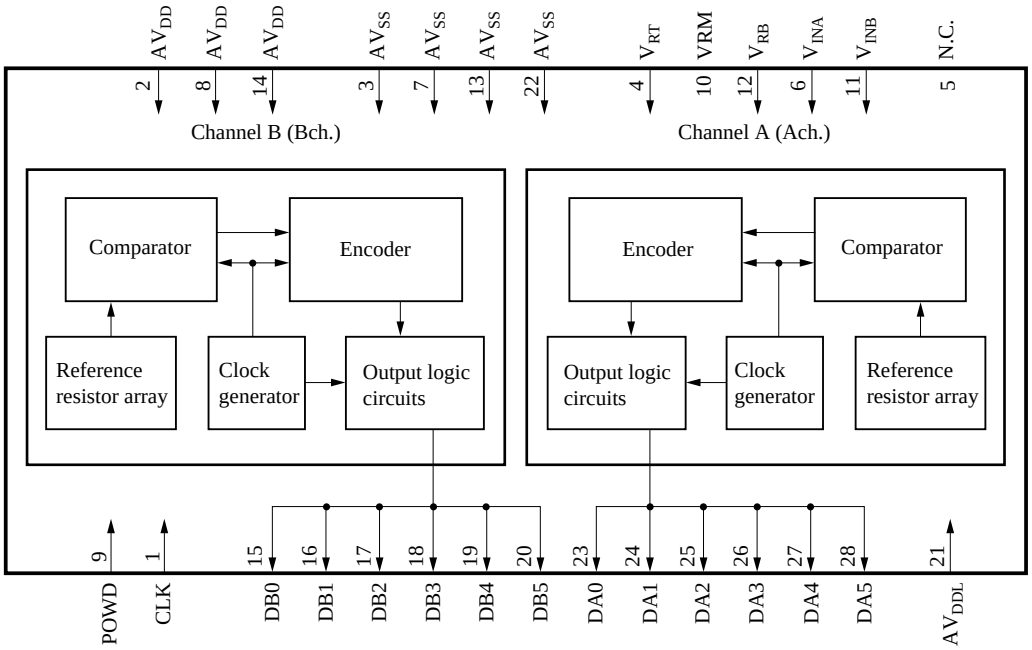
■ Pin Assignment



(TOP VIEW)

SOP028-P-0375

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Function Descriptions
1	CLK	Clock input
2	AV_{DD}	Power supply for analog circuits
3	AV_{SS}	Ground for analog circuits
4	V_{RT}	Reference voltage (top)
5	N.C.	No connection
6	V_{INA}	Analog signal input pin
7	AV_{SS}	Ground for analog circuits
8	AV_{DD}	Power supply for analog circuits
9	POWD	Power-down selection pin
10	VRM	Intermediate reference voltage
11	V_{INB}	Analog signal input pin
12	V_{RB}	Reference voltage (bottom)
13	AV_{SS}	Ground for analog circuits
14	AV_{DD}	Power supply for analog circuits
15	DB0	Digital output pin
16	DB1	Digital output pin
17	DB2	Digital output pin
18	DB3	Digital output pin
19	DB4	Digital output pin
20	DB5	Digital output pin
21	AV_{DDL}	Power supply pin for digital output circuits
22	AV_{SS}	Ground for analog circuits
23	DA0	Digital output pin
24	DA1	Digital output pin
25	DA2	Digital output pin
26	DA3	Digital output pin
27	DA4	Digital output pin
28	DA5	Digital output pin

■ Absolute Maximum Ratings Ta=25˚C

Parameter	Symbol	Rating	Unit
Power supply voltage	AV_{DD}	– 0.3 to +7.0	V
Power supply voltage for output circuits	AV_{DDL}	– 0.3 to AV_{DD} +0.3	V
Input voltage	V_I	– 0.3 to AV_{DD} +0.3	V
Output voltage	V_O	– 0.3 to AV_{DD} +0.3	V
Operating ambient temperature	T_{opr}	–20 to +70	˚C
Storage temperature	T_{stg}	–55 to +125	˚C

■ Recommended Operating Conditions

AV_{DD}=5.0V, AV_{DDL}=3.3V, AV_{SS}=0V, Ta=25˚C

Parameter		Symbol	min	typ	max	Unit
Power supply voltage		V_{DD}	4.75	5.00	5.25	V
Power supply voltage for digital outputs		DV_{DDL}	3.00	3.30	5.25	V
Digital input voltage	"H" level	V_{IH}	2.2		AV_{DD}	V
	"L" level	V_{IL}	AV_{SS}		0.8	V
Reference voltage	"H" level	V_{RT}	2.0	2.5	3.5	V
	"L" level	V_{RB}	0.5	1.0	2.0	V
Clock	"H" level pulse width	t_{WH}	7			ns
	"L" level pulse width	t_{WL}	7			ns
Analog input voltage		V_{AIN}	AV_{SS}		AV_{DD}	V

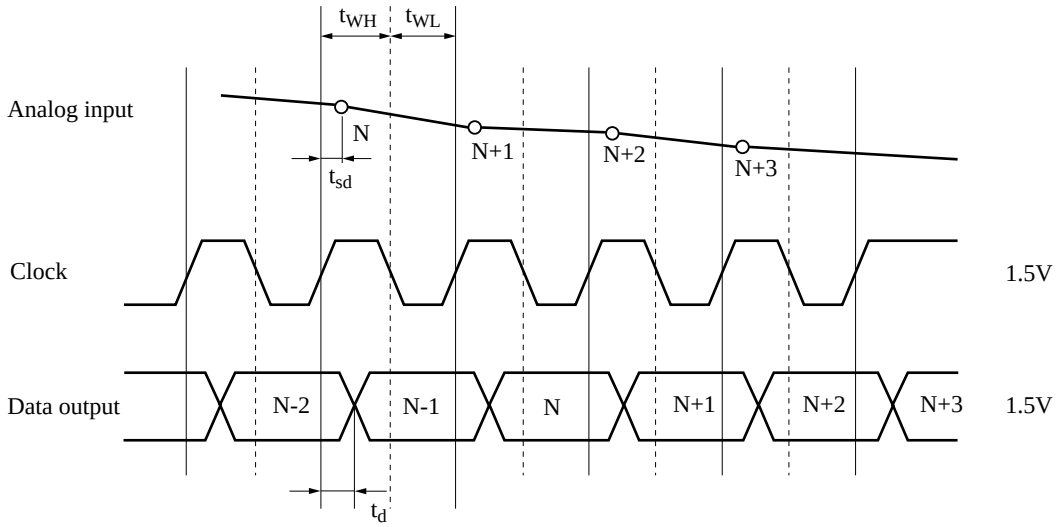
■ Electrical Characteristics

AV_{DD}=5.0V, AV_{DDL}=3.3V, AV_{SS}=0V, V_{RT}=2.5V, V_{RB}=1.0V, Ta=25˚C

Parameter		Symbol	Conditions	min	typ	max	Unit
Current consumption	AV_{DD}	I_{DD}	f_{CLK}= 60 MSPS (not including reference current)		47	80	mA
	AV_{DDL}	I_{DDL}			3	6	mA
Resolution		RES			6		bit
Linearity error		E_L	f_{CLK}=60MSPS		±0.7	±1.3	LSB
Differential linearity error		E_D			±0.7	±1.3	LSB
Maximum conversion rate		$F_{C(max.)}$		60			MSPS
Clock frequency		f_{CLK}		1		60	MHz
Analog input dynamic range		D_R		1.4		V_{RT}–V_{RB}	V
Output current	"H" level	I_{OH}	V_{OH}=DV_{DDL}– 0.8V			–2.0	mA
	"L" level	I_{OL}	V_{OL}=0.4V	2.0			mA
Output delay time		t_d	C_L=20pF	3	7	11	ns
Analog input capacitance		C_I			20		pF

■ Timing Chart

The chip samples the analog input at the rising edge of the clock signal and provides the corresponding digital output one clock cycle later at the rising edge of the clock signal.



Note: The circles indicate analog signal sampling points.

■ Package Dimensions (Unit:mm)

SOP028-P-0375