❑ MN102L62G

Type	**MN102L62G (under development)**
ROM (×8-Bit / ×16-Bit)	128 K
RAM (×8-Bit / ×16-Bit)	5 K
Minimum Instruction Execution Time	**148 ns (at 3.0 V to 3.6 V 13.5 MHz)**
Interrupts	• RESET • Watchdog • Timer Counter 0 to 5 • Timer Counter 6 to 7 • Timer Counter 6 to 7 Compare Capture A • Timer Counter 6 to 7 Compare Capture B • ATC Transfer finish • External 0 to 4 • Serial ch 0, 1 Transmission • Serial ch 0, 1 Reception • NMI Pin • A/D Conversion finish
Timer Counter	**Timer Counter 0 : 8-Bit × 1** (Timer Output, Event Count) Clock Source 1/1, 1/128 of System Clock, 1/4 of Low Speed Clock, External Clock Interrupt Source . . . .Underflow of Timer Counter 0 **Timer Counter 1 : 8-Bit × 1** (Timer Output, Event Count, A/D Conversion Start up) Clock Source System Clock, 1/4 of Low Speed Clock, External Clock, Timer Counter 0 Output Interrupt Source Underflow of Timer Counter 1 **Timer Counter 2 to 3 : 8-Bit × 1** (Timer Output, Event Count, UART Baud Rate Generator) Clock Source System Clock, External Clock, Timer Counter 0 Output, Timer Counter 1, 2 Output Interrupt Source Underflow of Timer Counter 2, 3 **Timer Counter 4, 5 : 8-Bit × 1** (Timer Output, Event Count) Clock Source . . . . 1/4 of Low Speed Clock, External Clock, Timer Counter 0 Output, Timer Counter 3, 4 Output Interrupt Source Underflow of Timer Counter 4, 5 **Timer Counter 6, 7 : 16-Bit × 1** (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-Phase Encoder Input) Clock Source System Clock, External Clock, Timer Counter 4, 5 Output Interrupt Source Coincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture, Underflow of Timer Counter 6, 7 (Connectable) Timer Counter 0 to 5
Serial Interface	**Serial 0 : 7, 8-Bit × 1** (Common use with UART, Transfer direction of MSB/LSB selectable) Clock Source . 1/16 of Timer Counter 2, 1/16 of Timer Counter 3, External Clock, 1/2 of Timer Counter 2 **Serial 1 : 7, 8-Bit × 1** (Common use with UART, Transfer direction of MSB/LSB selectable) Clock Source 1/16 of Timer Counter 2, 1/16 of Timer Counter 3, External Clock, 1/2 of Timer Counter 3 **UART × 2** (Common use with Serial 0, 1) **I^2C × 2** (Single master)
I/O Pins | **I/O** | **80**	• Common use 16 (by 8-Bit), 8 (by 4-Bit), 56 (by-bit)
A/D Inputs	8-Bit × 8ch (with S/H)
PWM	16-Bit × 2ch

Notes

Burst ROM inferface support, ATC (between serial 0ch and internal RAM) support

Package

LQFP100-P-1414

Electrical Characteristics

A/D Characteristics

Parameter	Symbol	Condition		Limit min	Limit typ	Limit max	Unit
A/D Conversion Relative Error		VDD = 3 3 V, VSS = 0 V	ch0 to 3			±3	LSB
			ch4 to 7			+4	LSB
A/D Conversion Time				7 11			µs
Analog Input Voltage	VIA			VSS		VDD	V

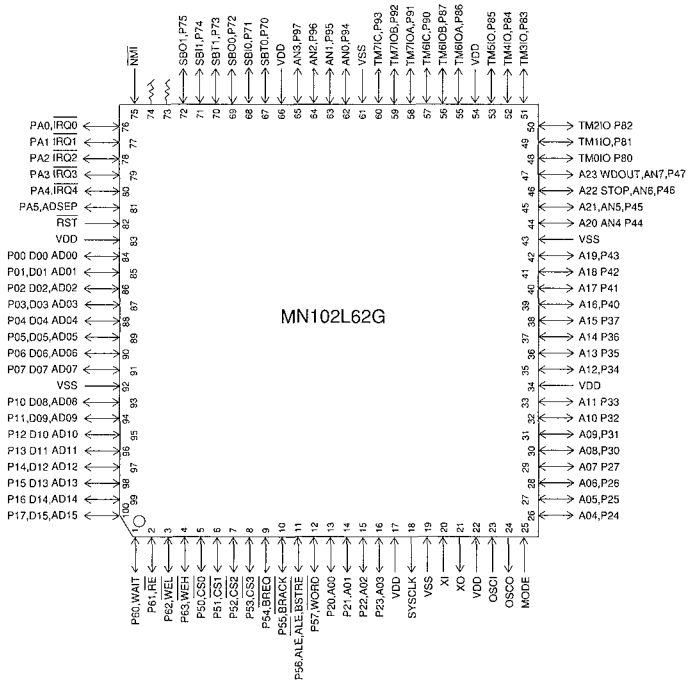
(Ta = 25 °C, VDD = 3.3 V, VSS = 0 V)

Support Tool

In-Circuit Emulator

PX-ICE102L00 + PX-PRB102L25

Pin Assignment



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