

MN102L2403

Type	MN102L2403 [ES (Engineering Sample) available]
ROM (×8-Bit / ×16-Bit) RAM (×8-Bit / ×16-Bit)	Maximum 16 M in total (Special Register 1 K included) External ROM, RAM 3 K
Minimum Instruction Execution Time	100 ns (at 4.5 V to 5.5 V, 20 MHz)
Interrupts	<ul style="list-style-type: none"> • RESET • Watchdog • Timer Counter 0 to 7 • Timer Counter 8 to 10 • Timer Counter 8 to 10 Compare Capture A • Timer Counter 8 to 10 Compare Capture B • DMA 0 to 5 Transfer finish • External 0 to 7 • Serial ch 0 to 2, 1 Transmission • Serial ch 0 to 2 Reception • $\bar{K}I$ Pin (OR) • A/D Conversion finish • NMI Pin • Address coincidence
Timer Counter	<p>Timer Counter 0 : 8-Bit × 1 (Timer Output, Event Count)</p> <p>Clock Source . 1/(1 to 256) of System Clock, External Clock</p> <p>Interrupt Source Underflow of Timer Counter 0</p> <p>Timer Counter 1 : 8-Bit × 1 (Timer Output, Event Count, DMA Start up)</p> <p>Clock Source 1/(1 to 256) of System Clock, External Clock</p> <p>Interrupt Source Underflow of Timer Counter 1</p> <p>Timer Counter 2 : 8-Bit × 1 (Timer Output, Event Count, Synchronous Output (4-Bit × 2ch))</p> <p>Clock Source 1/(1 to 256) of System Clock, External Clock, 1/4 of Low Speed Clock</p> <p>Interrupt Source Underflow of Timer Counter 2 4</p> <p>Timer Counter 3 : 8-Bit × 1 (Timer Output, Event Count, A/D Conversion Start up)</p> <p>Clock Source 1/(1 to 256) of System Clock, External Clock, 1/4 of Low Speed Clock</p> <p>Interrupt Source Underflow of Timer Counter 3</p> <p>Timer Counter 4 : 8-Bit × 1 (Time Output, Event Count, DMA start up)</p> <p>Clock Source . 1/(1 to 256) of System Clock, External Clock</p> <p>Interrupt Source . Underflow of Timer Counter 4</p> <p>Timer Counter 5 to 7 : 8-Bit × 1 (Timer Output, Event Count, UART Baud Rate Generator, Synchronous Serial Clock Generator)</p> <p>Clock Source .. 1/(1 to 256) of System Clock, External Clock</p> <p>Interrupt Source Underflow of Timer Counter 5 to 7</p> <p>Timer Counter 8, 9 : 16-Bit × 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, 2-Phase Encoder Input)</p> <p>Clock Source 1/(1 to 256) of System Clock, External Clock</p> <p>Interrupt Source Coincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture, Underflow of Timer Counter 8, 9</p> <p>Timer Counter 10 : 16-Bit × 1 (Timer Output, Event Count, Input Capture, Output Compare, PWM Output, Synchronous Output (4-Bit × 2ch))</p> <p>Clock Source 1/(1 to 256) of System Clock, External Clock</p> <p>Interrupt Source .Coincidence with Compare Capture A or at Capture, Coincidence with Compare Capture B or at Capture</p> <p style="text-align: center;">(Connectable) Timer Counter 0 to 7</p>
Serial Interface	<p>Serial 0 : 7,8-Bit × 1 (Common use with UART, Transfer direction of MSB/LSB selectable)</p> <p>Clock Source .. 1/2 Timer Counter 5, 1/16 of Timer Counter 5, External Clock, Automatic Baud Rate</p> <p>Serial 1 : 7,8-Bit × 1 (Common use with UART, Transfer direction of MSB/LSB selectable)</p> <p>Clock Source . . . 1/2 Timer Counter 6, 1/16 of Timer Counter 6, 7, External Clock</p> <p>Serial 2 : 7,8-Bit × 1 (Common use with UART, Transfer direction of MSB/LSB selectable)</p> <p>Clock Source 1/2 of Timer Counter 7, 1/16 of Timer Counter 5, 7, External Clock</p> <p>UART × 3 (Common use with Serial 0, 1, 2)</p> <p>I²C × 3 (Single master)</p>

I/O Pins	I/O	39	• Common use 39 (by-bit)
	Input	13	• Common use 13 (by-bit)
	Output	14	• Common use 6 (by-bit), 8 (by 4-Bit)

A/D Inputs	10-Bit × 8ch (with S/H)
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PWM	16-Bit × 3ch
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Notes	Burst ROM Interface, DMA Controller, DRAM Refresh Controller, DRAM High Speed Page Mode, EDO Mode Support
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Package	LQFP128-P-1818B
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Electrical Characteristics

A/D Characteristics

Parameter	Symbol	Condition	Limit			Unit
			min	typ	max	
A/D Conversion Absolute Error		AVDD = 5 V, AVSS = 0 V			±4	LSB
A/D Conversion Time			5	6		μs
Analog Input Voltage	VIA		VSS		VDD	V

(Ta = 25 °C, VDD = 5.0 V, VSS = 0 V)

Support Tool

In-Circuit Emulator	PX-ICE102L00 + PX-PRB102L24
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Pin Assignment

