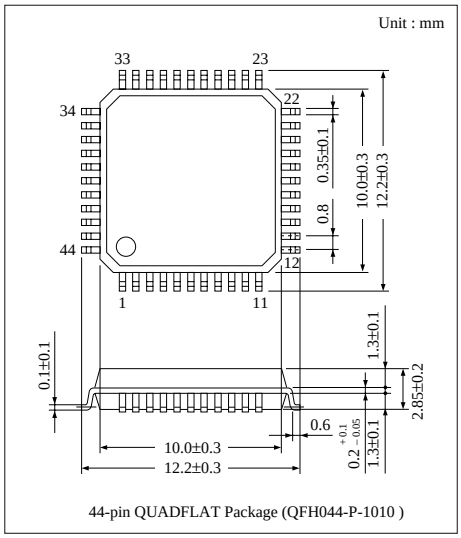
DN8648FBP

32-bit Shift Register Latch Driver IC

■ Overview

The DN8648FBP is an IC which incorporates a 32-bit shift register and a latch driver to meet high-speed operation low power consumption and high-density printout of the thermal printers for the work processors, and so on. It employs the Bi-CMOS process in which the serial-in and serial-out/parallel-out functions are incorporated, the 32-step shift register block and latch block are composed of CMOS, and the 32-step parallel driver block is bipolar.



44-pin QUADFLAT Package (QFH044-P-1010)

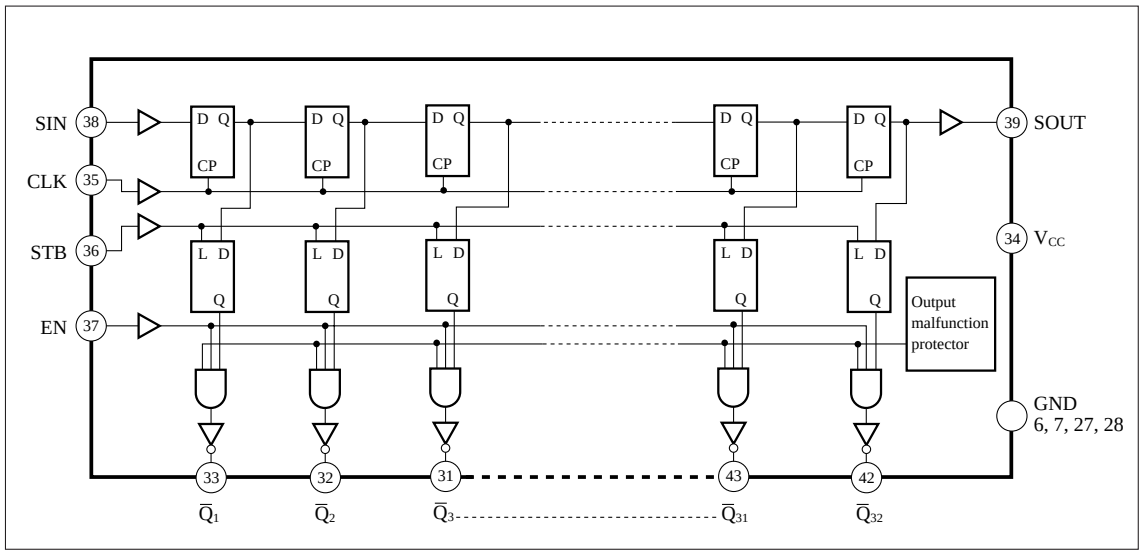
■ Features

- Serial-in and serial-out/parallel-out
- Cascade connection allowed
- Built-in output malfunctioning preventive circuit
- Low current consumption at standby $I_{CC} \leq 100\mu A$
- High-breakdown, large current drive type output steps
  Breakdown voltage : 30V
  Output current : 120mA (per pin)
- Surface mountable 44-pin flat package (pin pitch : 0.8mm)

■ Applications

- Driving of the thermal heads
- Driving of the relays, LEDs, solenoids, etc.

■ Block Diagram



■ Absolute Maximum Ratings (Ta = 25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	0 to 7	V
Output voltage	V_O	0 to 30	V
Output current	I_O	120 (Per one circuit)	mA
Power dissipation	P_D	1.8 *	W
Operating ambient temperature	T_{opr}	– 20 to + 75	˚C
Storage temperature	T_{stg}	– 55 to + 125	˚C

* When mounting onto the PCB, power dissipation is reduced at a rate of 15mW/˚C from Ta= 25˚C.

■ Recommended Operating Range (Ta=25˚C)

Parameter		Symbol	Range
Operating supply voltage		V_{CC}	4 to 6V
Output voltage		V_O	below 30V
Output current		I_O	below 100mA *1
Clock frequency		f_{CLK}	below 10MHz *2
Input pulse width	CLK	t_w	over 40ns
	STB		over 40ns
Setup time	SIN	t_{su}	over 30ns
	STB		over 40ns
Hold time	SIN	t_h	over 20ns
	STB		over 0ns
Clock pulse rise time		t_r	below 500ns
Clock pulse fall time		t_f	below 500ns

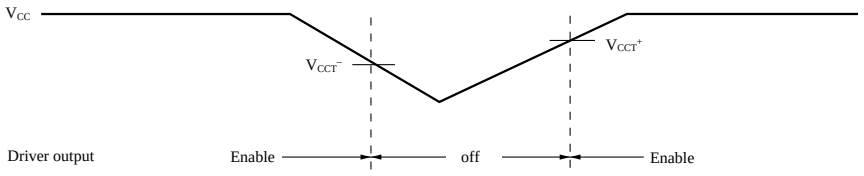
*1 An allowable value changes depends on the number of simultaneously turned-on circuits and the duty. Use with power dissipation taken into full account.
*2 Input duty : 40 to 60%

■ Electrical Characteristics (Ta=25˚C)

Parameter	Symbol	Condition	min	typ	max	Unit
Input voltage	V_{IH}	V_{CC}= 4 to 6V	0.7V_{CC}	—	V_{CC}	V
	V_{IL}		0	—	0.3V_{CC}	V
Input current	I_{IH}	V_{IH}= 5V	—	—	25	µA
	I_{IL}	V_{IL}= 0V	—	—	– 25	µA
Output voltage (SOUT)	V_{OH}	I_O= –1µA	4.9	—	—	V
	V_{OL}	I_O=1µA	—	—	0.1	V
Output current (SOUT)	I_{OH}	V_{OH}= 4.5V	– 4	—	—	mA
	I_{OL}	V_{OL}= 0.4V	4	—	—	mA
Output saturation voltage ($\overline{Qn}$)	$V_{CE\ (sat)\ 1}$	I_{OL}=100mA	—	—	0.4	V
	$V_{CE\ (sat)\ 2}$	I_{OL}= 80mA	—	—	0.35	V
Output leakage current	I_{OLK1}	V_O= 30V (output OFF)	—	—	50	µA
	I_{OLK2}	V_O=15V (output OFF)	—	—	25	µA
Supply current	I_{CC1}	Total driver output OFF	—	—	100	µA
	I_{CC2}	Driver output 1 circuit ON	—	—	5	mA
Output malfunctioning preventive Circuit operating voltage	V_{CCT^+}	*	2.9	—	3.9	V
	V_{CCT^-}	*	2.6	—	3.6	V

* V_{CC}=5V unless otherwise specified

* Output malfunctioning preventive circuit operating voltage timing chart



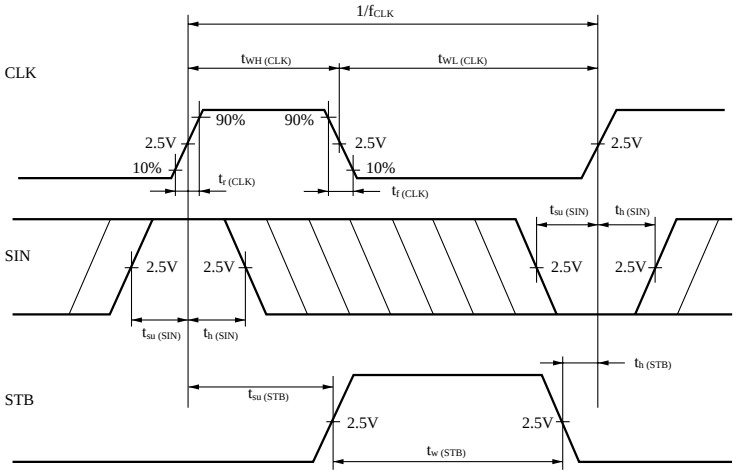
■ Switching Characteristics (Ta =25˚C)

Parameter	Symbol	Input	Output	Condition	min	typ	max	Unit
Maximum clock frequency	$f_{max.}$	CLK			10	—	—	MHz
Propagation delay time	t_{PLH}	CLK	SOUT	V_{CC} = 5V C_L = 15pF	—	—	100	ns
	t_{PHL}				—	—	100	ns
	t_{PLH}	CLK	$\overline{Q}n$	V_{CC} = 5V R_L = 100Ω C_L = 15pF	—	—	2	µs
	t_{PHL}				—	—	0.5	µs
	t_{PLH}	EN	$\overline{Q}n$		—	—	2	µs
	t_{PHL}				—	—	0.5	µs

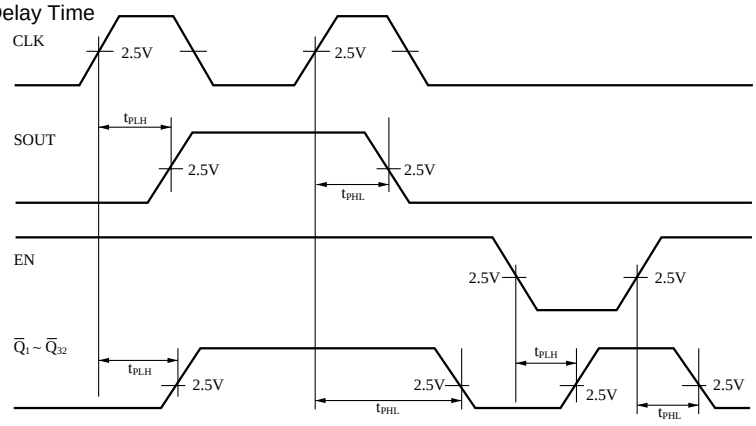
■ Supplementary Descriptions

• Timing Chart

1. Input Timing



2. Propagation Delay Time



■ Supplementary Descriptions (cont.)

• Function Table

Input				Driver output		SOUT
CLK	EN	STB	SIN	$\overline{Q}_1$	$\overline{Q}_n$	
↑	L	×	×	H	H	Q'_{31}
↓	L	×	×	H	H	nc
↑	H	L	×	nc	nc	Q'_{31}
↑	H	H	L	H	$\overline{Q}_{n-1}$	Q'_{31}
↑	H	H	H	L	$\overline{Q}_{n-1}$	Q'_{31}
↓	H	H	×	nc	nc	nc

Note) H = High level, L = Low level, × = Either "H" or "L" will do, ↑ = Transition from "H" to "L",
↓ = Transition from "H" to "L", nc = No change, Q'_{31} = Status of the 31st shift register

• Pin Assignments