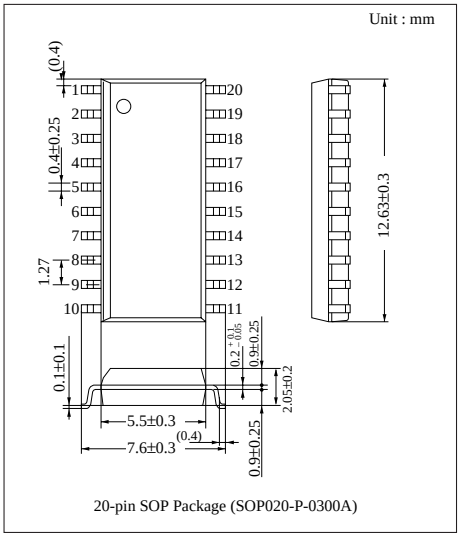
DN8667NS

8-Bit Shift Register Latch Constant Current Driver IC

■ Overview

The DN8667NS is a semiconductor integrated circuit which incorporates a 8-bit shift register, a latch driver and a constant current driver to satisfy the demand for equalization of LED panel brightness. It also incorporates the serial-in and serial-out/parallel-out functions. It employs the Bi-CMOS process : The 8-step shift register block and latch block consist of CMOS while the 8-step parallel driver block is bipolar.



20-pin SOP Package (SOP020-P-0300A)

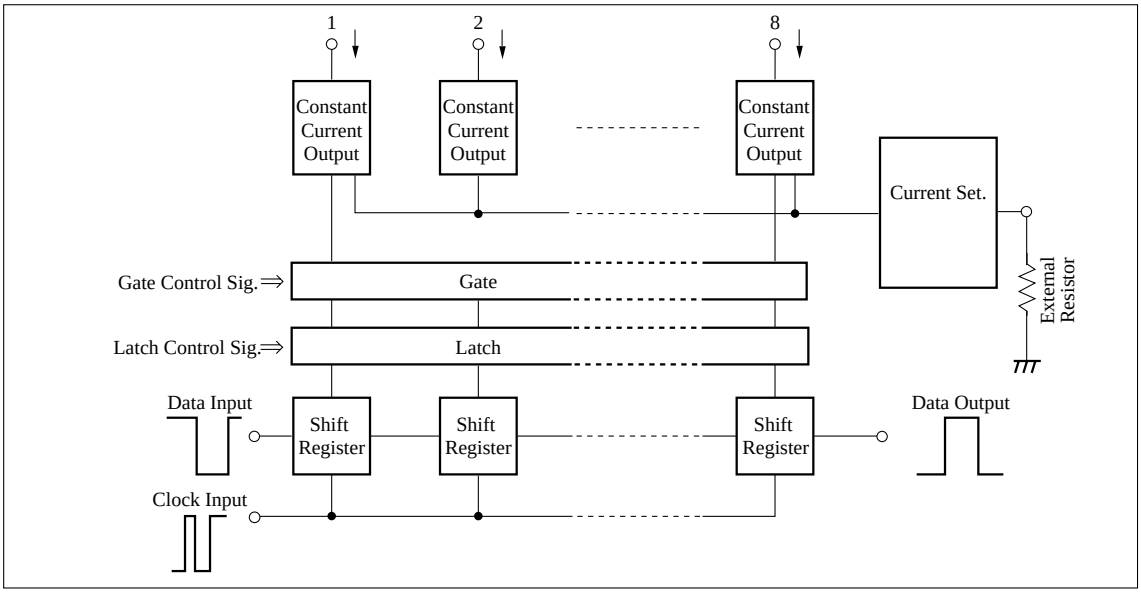
■ Features

- Serial-in, serial-out/parallel-out
- Cascade connection possible
- Constant current output (0 to 100 mA able to be set by one external resistor)
- Output-forced ON/OFF terminal attached (EN)
- Input/Output CMOS compatible

■ Application

- LED panel drive

■ Block Diagram



■ Absolute Maximum Rating (Ta = 25˚C)

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	0 to + 7.0	V
Output voltage	V_O	0 to + 14	V
Output current	I_O	150	mA
Power dissipation*	P_D	1.28	W
Operating ambient temperature	T_{opr}	–20 to + 85	˚C
Storage temperature	T_{stg}	–55 to + 150	˚C

* For printed board SM, it decreases with rate of 10.24 mW/˚C from Ta = 25 ˚C.

■ Recommended Operation Range (Ta=25 ˚C)

Parameter	Symbol	Range
Operating supply voltage	V_{CC}	4.5V to 5.5V

■ Electrical Characteristics (V_{CC}=5V,Ta=25 ± 2˚C)

Parameter		Symbol	Condition	min	typ	max	Unit
Input voltage	Positive direction	V_{T+}	V_{SOUT} = 0.1, V_{CC} – 0.1V $\lvert I_{SOUT}\rvert$ = 20µA	0.35V_{CC}	—	0.7V_{CC}	V
	Negative direction	V_{T-}	I_O ($\overline{Qn}$) = –10µA, 90mA V_O ($\overline{Qn}$) = 0.6V I_{ref} = –2.5mA	0.2V_{CC}	—	0.55V_{CC}	V
Input current		I_{IH}	V_{1H} = 5.0V	—	—	25	µA
		I_{IL}	V_{1L} = 0V	– 25	—	—	µA
Output voltage (SOUT)		V_{OH}	I_{OH} = – 0.4mA	4.0	—	—	V
		V_{OL}	I_{OL} = 1.6mA	—	—	0.5	V
Output current 1 ($\overline{Qn}$)		I_{OI}	V_O ($\overline{Qn}$) = 0.5V	—	—	100	mA
Output current 2 ($\overline{Qn}$)		I_{OI}	V_{CC} = 5.0V, I_{ref} = –12mA V_O ($\overline{Qn}$) = 1.0V	83	—	117	mA
Output current error between bits		DI_O		—	—	±6	%
Output leak current		I_{OLK}	V_O= 14V (Output OFF)	—	—	25	µA
Supply current		I_{CC1}	Total Driver Output OFF, V_{CC}=5.5V, I_{ref} = 0mA	—	—	2	mA
		I_{CC2}	Total Driver Output OFF, V_{CC}=5.5V, I_{ref} = –2.5mA	—	—	20	mA
		I_{CC3}	Total Driver Output ON, V_{CC}=5.5V, I_{ref} = –2.5mA	—	—	30	mA
Clock frequency		f_{CLK}	CLK, Input Duty 40 to 60%	—	—	20	MH_Z
Input pulse width		t_w	CLK, V_{CC}=5.0V, R_L=50Ω, C_L=15pF	20	—	—	ns
			STB	20	—	—	ns
Setting-up time		t_{su}	SIN	20	—	—	ns
			STB	15	—	—	ns
Holding time		t_h	SIN	20	—	—	ns
			STB	10	—	—	ns
Clock pulse rise time		t_r		—	—	500	ns
Clock pulse fall time		t_f		—	—	500	ns

Note) V_{CC}= 5V unless otherwise specified.

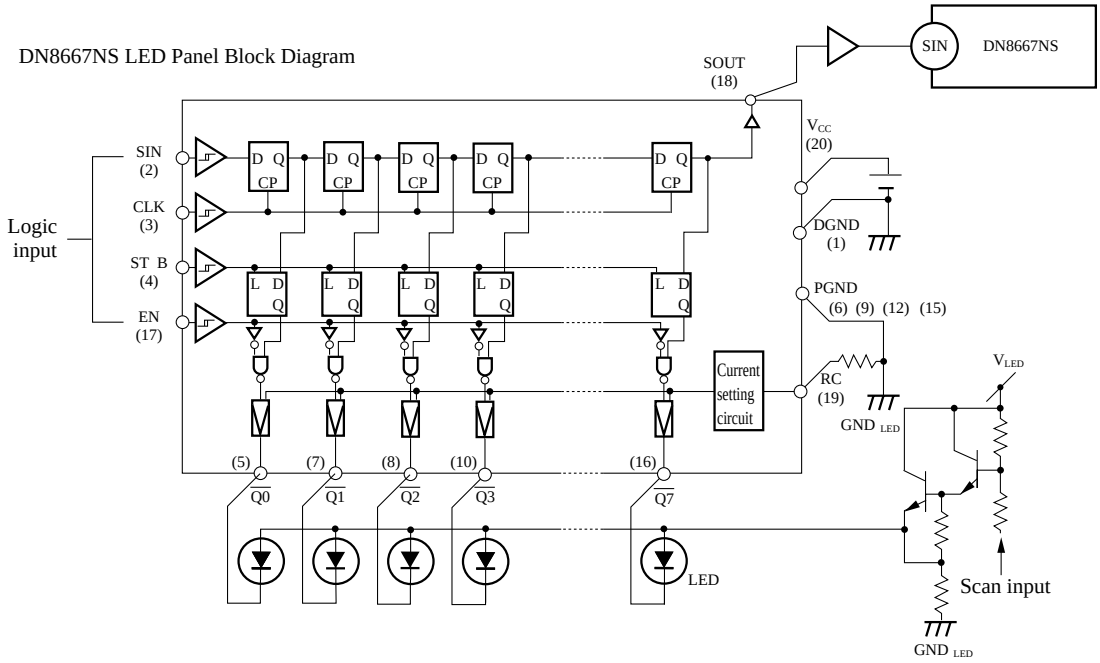
■ Pin Descriptions

Pin No.	Symbol	Pin name	Description
1	DGND	Digital ground	Digital ground
2	SIN	Serial data input	It is the serial data input terminal for shift register.
3	CLK	Clock input	The value of shift register shifts at the rising edge of clock input.
4	STB	Strobe input	Setting the STB input to "H" forwards the data of shift register to the latch. When the STB input is set to "L" , even if the value of shift register changes, the value of latch is not changed.
5 7,8 10,11 13,14 16	$\overline{Qn}$	Driver output	It outputs signals by using the polarity opposite to that of data taken into the latch. For example, when the value of serial input is "H" , the output becomes "L" level and the output is turned on. The output takes open collector form of NPN transistor.
6 9,12 15	PGND	Output ground	Output ground
17	EN	Enabling input	When the EN input is set to "H" , all the outputs are turned off, independent of condition of shift register or latch driver.
18	SOUT	Serial data output	It is the terminal which performs the serial-output of data inputted from the SIN.
19	RC	Constant current setting input	It connects the external resistor between RC and GND and sets the current of output block. * Output current calculation : $I_{O}(\overline{Qn})_{(A)} \approx \frac{20 \times V_{CC}\,(V)}{R_{RC}\,(\Omega) + 90}$ or $R_{RC}{}_{(\Omega)} \approx \frac{1}{2}\left(\frac{V_{CC}\,(V)}{I_{RC}\,(A)} - 180\right)$ ** RC terminal setting calculation : $I_{RC}{}_{(A)} \approx \frac{V_{CC}\,(V)}{2 \times R_{RC}\,(\Omega) + 180}$
20	V_{CC}	V_{CC}	Supply terminal

* Calculation example
$V_{CC} = 5V$
$R_{RC} = 910\Omega$
$I_{O}(\overline{Qn}) \approx \frac{20 \times 5}{910 + 90}$
$I_{O}(\overline{Qn}) \approx 100mA$

** Calculation example
$V_{CC} = 5V$
$I_{RC} = 0.0025A$
$R_{RC} \approx \frac{1}{2}\left(\frac{5}{0.0025} - 180\right)$
$R_{RC} \approx 910\ (\Omega)$

■ Application Circuit

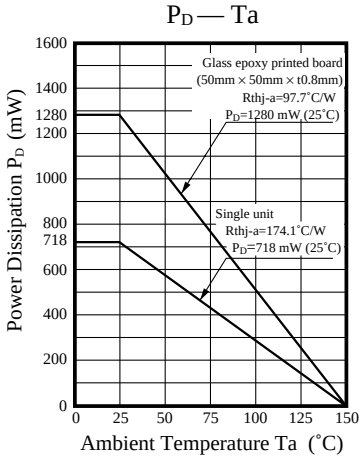


■ Function Table (Note)

Input				Output			
CLK	STB	EN	SIN	$\overline{Q_O}$	$\overline{Q_m}$	$\overline{Q_7}$	SOUT
↑	H	L	Q_n	$\overline{Q_n}$	$\overline{Q_{m-1}}$	$\overline{Q_6}$	Q_6
↑	L	L	Q_n	nc	nc	nc	Q_6
↑	×	H	Q_n	H	H	H	Q_6
↓	×	×	Q_n	nc	nc	nc	nc

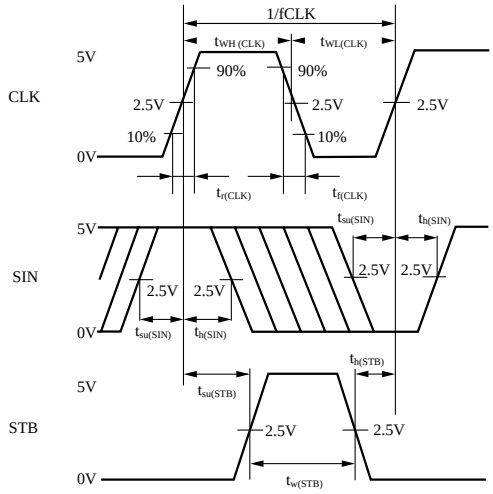
(Note)
H : High level,
L : Low level,
× : H or L
Q_m, Q_n : H or L.
However, for $\overline{Q_n}$, "H"= OFF, "L"= ON.
↑ : Shift from L to H,
↓ : Shift from H to L
nc : No change

■ Characteristics Curve



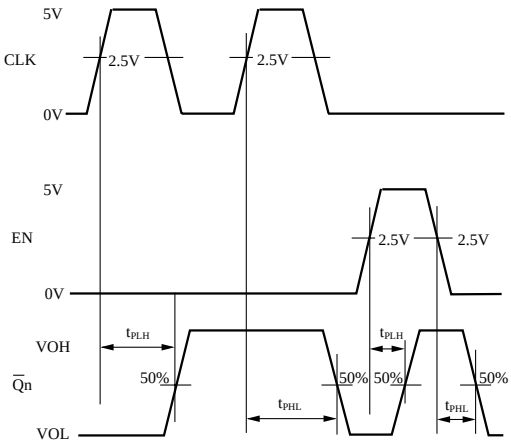
■ Timing Chart

1.Input timing



(V_{IL}= 0V,V_{IH}= 5.0V)

2.Transmission delay time



(V_{IL}= 0V,V_{IH}= 5.0V)