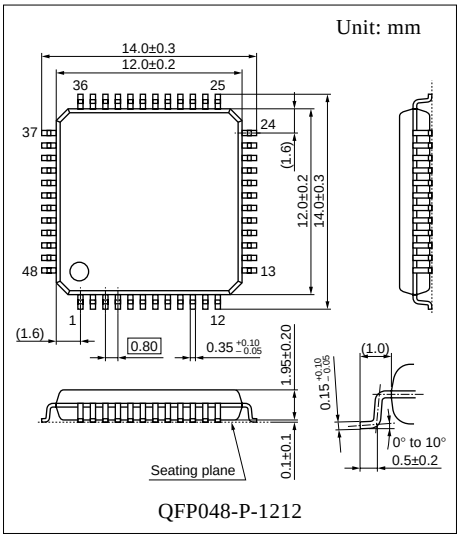
AN5367FB

NTSC video, chroma, and deflection signal processing circuit

■ Overview

The AN5367FB is an IC to demodulate the NTSC composite signal. It is possible to control the all functions by the I²C bus. The use of flat package allows a space saving in sets design.



QFP048-P-1212

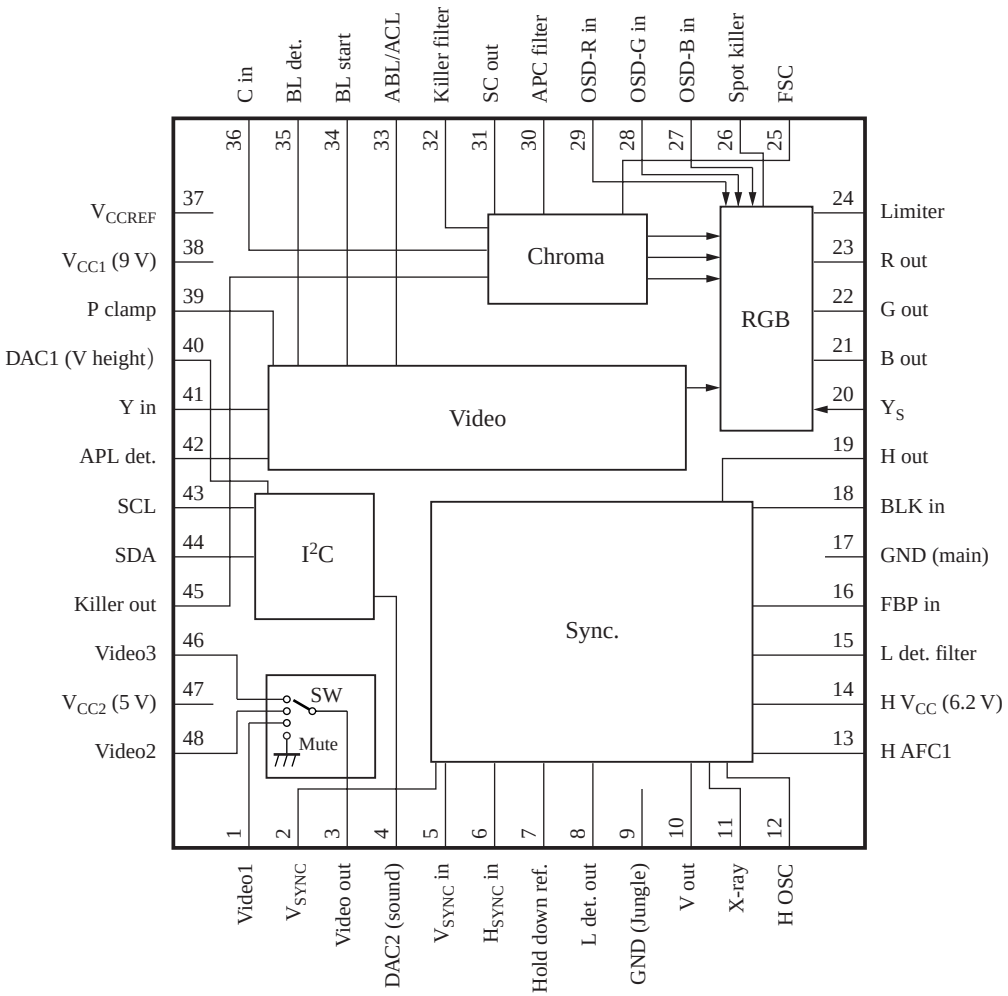
■ Features

- Luminance signal processing
  - Incorporating 3.58 MHz trap
  - Black side gradation control is possible by black expansion circuit
  - Adopting delay line aperture control
- Color signal processing
  - Incorporating band-pass filter
  - Incorporating ACC filter
- Deflection signal processing
  - Stable sync. signal generation by the use of double AFC circuit and countdown circuit
  - Vertical directional screen position is adjustable
- Others
  - Incorporating 3-input composite signal changeover SW
  - DAC output for adjusting sound volume and screen height

■ Applications

- Color televisions and combined CTV/VCR set

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	Video signal input pin 1	11	Hold down input pin
2	Vertical signal clamp pin	12	Horizontal oscillation pin
3	Video signal output pin	13	Horizontal AFC1 filter pin
4	DAC output pin 1	14	Horizontal stabilized power supply pin (6.2 V)
5	Vertical sync. separation input pin	15	Lock detection filter pin
6	Horizontal sync. separation input pin	16	FBP input pin
7	Hold down reference voltage pin	17	GND pin
8	Lock detection output pin	18	Blanking pulse input pin
9	GND pin (sync. system)	19	Horizontal pulse output pin
10	Vertical pulse output pin	20	Y_S input pin

■ Pin Descriptions (continued)

Pin No.	Description	Pin No.	Description
21	B output pin	35	Black level detection filter pin
22	G output pin	36	Chroma signal input pin
23	R output pin	37	V_{CC1} reference voltage pin (9.6 V)
24	Output limiter pin	38	Power supply pin (V_{CC1}: 9 V)
25	Chroma oscillator pin	39	Capacitor pin for Y clamp
26	Spot killer pin	40	DAC output pin 2
27	External B input pin	41	Y signal input pin
28	External G input pin	42	APL detection filter pin
29	External R input pin	43	SCL pin (for I^2C bus)
30	Chroma APC filter pin	44	SDA pin (for I^2C bus)
31	Subcarrier output pin	45	Killer output pin
32	Killer filter pin	46	Video signal input pin 3
33	ABL/ACL input pin	47	Power supply pin (V_{CC2}: 5 V)
34	Black extension start adjusting pin	48	Video signal input pin 2

■ Absolute Maximum Ratings

Parameter	Symbol		Rating	Unit
Supply voltage	V_{CC}	$V_{CC1\ (38)}$	9.9	V
		$V_{CC3\ (47)}$	5.5	
Supply current	I_{CC}	I_{38}	47	mA
		I_{47}	31	
		I_{14}	13	
		I_{37}	5	
Power dissipation *2	P_D		775	mW
Operating ambient temperature *1	T_{opr}		–20 to +70	°C
Storage temperature *1	T_{stg}		–55 to +150	°C

Note) ∗1 : Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
∗2 : The power dissipation shown is the value for T_a = 70°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	8.55 to 9.45	V
	V_{CC2}	4.75 to 5.25	
Supply current	I_{14}	6.0 to 12	mA
	I_{37}	1.0 to 4.5	

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SW and power supply						
Circuit current 1 (I_{CC1}) (9 V system)	I_{38}	No signal input, I_{14} = 8 mA, V_{CC1} = 9 V, V_{CC2} = 5 V	28	36	43	mA
Circuit current 2 (I_{CC2}) (5 V system)	I_{47}	No signal input, I_{14} = 8 mA, V_{CC1} = 9 V, V_{CC2} = 5 V	18	23	28	mA
9.6 V reference voltage	V_{37}	I_{37} = 2.4 mA	9.0	9.6	10.2	V
Operating resistance	R_{37}	I_{37} = 1.0 mA to 5.0 mA	0	11	30	Ω
Zener maximum current	I_{VD}	Largest possible sink current	5	—	—	mA
SW circuit gain	G_{SW}	f = 1 MHz, 0.7 V[p-p]	4.9	5.9	6.9	dB
Frequency characteristics	f_{SW}	Attenuation amount at 7 MHz with f = 1 MHz as reference	–3	–1.3	—	dB
Crosstalk	CT	f = 1 MHz, input signal 0.7 V[p-p], sine wave	–50	—	—	dB
Clamp current	I_1 , I_{46} , I_{48}	Sink current of each input pin, when applying 3 V to pin 1, pin 46 and pin 48	6	10	14	μA
Total gain	G_{TOTAL}	Gain dispersion from each input to output	–19	0	+19	%
Y signal processing						
Video input pin voltage	V_{41}	V_{CC}: Typ., input pin voltage measurement	1.1	1.5	1.9	V
Y typical output	E_{OSTD}	Input 2 V[p-p] stair steps	2.6	3.2	3.8	V[0-p]
Video voltage gain relative ratio	ΔG_Y	As same as the above, G/R, B/R	–1.0	0	+1.0	dB
Video voltage gain	G_Y	Input 2 V[p-p] stair steps, contrast: typ.	1.7	2.1	2.5	V[0-p]
Video frequency characteristics	f_Y	Attenuation amount at 6 MHz with f = 1 MHz as reference	–5.0	–2.0	—	dB
Picture quality variable range 1	G_{S1}	Input 0.2 V[p-p], sine wave f = 2.5 MHz, sharpness: typ./min.	5.9	9.0	11.4	dB
Contrast ratio	G_C	Input 2 V[p-p] stair steps, contrast: max./min.	6	9	12	dB
Brightness variable range	BR	Input: Without input, cut-off: max. , brightness: min. to max. , pedestal level measurement	2.15	2.40	2.80	V
Typical pedestal voltage	PL_{STD}	Input: Without input	1.95	2.60	3.10	V
DC restoration ratio 1	T_{DC1}	Input 2.0 V[p-p] total white, APL 10% to 90%, DC restoration ratio correction: Off (pin 42: 0 V)	94	100	106	%
RGB output BLK level	Y_{BLK}	V_{CC}: typ.	1.0	1.5	2.0	V
Black level correction amplitude 1	V_{BL1}	Input signal: Total black, black level detection pin: external RC → 9 V, BL start = 20 kΩ	–100	0	+100	mV

Note) Unless otherwise specified, refer to "• Typical conditions for testing" for the conditions of I^2C bus and each pin.

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y signal processing (continued)						
Black level correction amplitude 2	V_{BL2}	Input signal: Total black, black level detection pin: 3 V, BL start = 20 kΩ	0.46	0.80	1.14	V
Black level correction amplitude 3	V_{BL3}	Adjust output amplitude to 0.8 V[p-p], black level detection pin: 9 V → external RC, BL start = 20 kΩ	0.10	0.25	0.40	V
Black level correction amplitude 4	V_{BL4}	Adjust output amplitude to 2.0 V[p-p], black level detection pin: 9 V → external RC, BL start = 20 kΩ	– 0.1	0	+0.1	V
Y signal delay time	t_{D1}	Input 2.0 V[p-p] stair step, B.P.F. SW: On, trap SW: On, measurement of time delay between input and output	330	410	490	ns
Sub-contrast adjustment range 1	E_{OADJ1}	Sub-contrast typ. → min., input: 2 V[p-p] stair step	–40	–30	–22	%
Sub-contrast adjustment range 2	E_{OADJ2}	Sub-contrast typ. → max., input: 2 V[p-p] stair step	35	46	55	%
Trap attenuation amount	G_{TRAP}	f = 3.579545 MHz, trap on/off	23	—	—	dB
Delay line	Δt_D	Difference of amount of delay between B.P.F. on/off	90	120	150	ns
ACL variable range	ΔACL	Pin 33 7.5 V → 2.5 V, stair step 2 V[p-p]	12	20	28	%
ABL variable range	ΔABL	Without input, pin 33: 4.5 V → 2.5 V, pedestal voltage of RGB output	0.4	0.6	0.8	V
Color signal processing						
ACC characteristics 1	ACC1	Color bar input: 6 dB up, (R–Y) output measurement, burst typical input = 150 mV[p-p]	0.9	1.0	1.1	Times
ACC characteristics 2	ACC2	Color bar input: 20 dB down, (R–Y) output measurement, burst typical input = 150 mV[p-p]	0.7	0.9	1.1	Times
Color killer tolerance 1	e_{K1}	Level at which demodulation output does not appear when color bar input level is being attenuated. Typical input level: 0 dB	–53	–43	–34	dB
Color difference output (B–Y) 1	e_{O1}	Color bar input, color: typ., tint: Center	1.55	2.00	2.45	V[0-p]
Color difference output (B–Y) 2	e_{O2}	Color bar input, color: max., tint: Center	2.85	3.7	4.5	V[0-p]
Color residue	e_{LC}	Color bar input, color: min.	—	15	60	mV
Chroma contrast	C_{CONT}	Color bar input, contrast: min. → max.	5.2	8.2	11.2	dB
Free-running frequency	f_{C0}	For f_0 of typical sample, f_0 = 3.579545 MHz	–300	0	+300	Hz
APC pull-in range 1	f_{APC}	Color bar: Typical input, B.P.F.: On	±450	±600	—	Hz
Tint center data	TC	Rainbow signal, tint data at which B–Y output becomes typical.	15	1D	25	H

Note) Unless otherwise specified, refer to "• Typical conditions for testing" for the conditions of I^2C bus and each pin.

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing (continued)						
Tint variable range	$\Delta\theta$	Tint = min. to max.	±30	±45	—	deg
Demodulation output ratio R/B	R/B	Rainbow input	0.76	0.96	1.15	Times
Demodulation output ratio G/B	G/B	Rainbow input	0.27	0.36	0.45	Times
Demodulation angle ∠R	∠R	Reference is ∠B	96	104	112	deg
Demodulation angle ∠G	∠G	Reference is ∠B	225	235	245	deg
Demodulation output residual carrier	A_{FSC}	f_{SC} component of demodulation output	—	20	50	mV[p-p]
CW output DC level 1	$V_{31(1)}$	Subcarrier output: Off	1.4	1.9	2.4	V
CW output DC level 2	$V_{31(2)}$	Subcarrier output: On	5.6	6.1	6.6	V
CW Out output level	A_{CW}	Output level of f_{SC}	250	350	500	mV[p-p]
High-level killer output	KIL_H	Pin 45 voltage measurement, V_{32} = 5.5 V	4.0	4.6	—	V
Low-level killer output	KIL_L	Pin 45 voltage measurement, V_{32} = 4 V	—	0.4	1.0	V
Killer output open	KIL_{OP}	At VV mode, I_{45} measurement, V_{32} = 4 V or 5.5 V	–1	0	+1	µA
RGB processing						
RGB output DC difference voltage	ΔPL_1	$\Delta V = V_R - V_G$, $V_G - V_B$, $V_B - V_R$, burst input only, cut off: min.	–300	0	+300	mV
RGB output limit level	V_{LIM}	Input: 2.0 V[p-p], total white, contrast: max., cut off: max., bright: max.	6.6	6.9	7.2	V
External RGB input clip level 1	E_{G1}	Y_S: H, contrast: max., difference from internal pedestal voltage, cut off: min., drive: typ.	2.2	2.6	3.0	V
External RGB input clip level 2	E_{G2}	Y_S: H, contrast: min., difference from internal pedestal voltage, cut off: min., drive: typ.	1.1	1.6	2.1	V
External RGB input clip level difference	ΔE_{G1}	Y_S: H, contrast: max., external input clip level difference among R, G and B channel	–300	0	+300	mV
External RGB gain	G_{EXT}	Y_S: H, contrast: max., input voltage: 0.3 V[p-p], sine wave, 1 MHz	1.6	2.3	3.0	Times
External RGB frequency characteristics	f_{EXT}	Y_S: H, contrast: max., input voltage: 0.3 V[p-p], sine wave, reference: 1 MHz, attenuation amount at 7 MHz	–4.8	–1.8	—	dB
Internal/external pedestal difference voltage	ΔPL_2	Burst input only, Y_S: high/low	50	250	600	mV
Y_S threshold level	Y_S	Pin 20 voltage at which inside and outside change over	1.1	1.6	2.1	V
Cut-off variable range	ΔCO	Without input, cut off: min. to max.	1.2	1.5	1.8	V
Drive variable range	ΔDR	Input: staircase, 2.0 V[p-p], drive: min. to max.	5	7	9	dB

Note) Unless otherwise specified, refer to "• Typical conditions for testing" for the conditions of I^2C bus and each pin.

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal signal processing						
Horizontal stabilized power supply voltage	V_{14}	Pin voltage, when power supply pin input current I_{14} = 8 mA	5.7	6.1	6.8	V
Horizontal stabilized power supply maximum current	I_{14}	Maximum input current for which power supply is stabilized	13	—	—	mA
Horizontal stabilized power supply on-state resistance	R_{14}	On-state resistance, when input current I_{14} = 6 mA to 13 mA	0	14	30	Ω
Horizontal output start voltage	V_{FHS}	Horizontal stabilized power supply voltage, when horizontal output pulse becomes 1 V[p-p] or more. Do not apply other power supply voltage.	—	4.5	5.2	V
Horizontal output pulse duty	τ_{HO}	Horizontal output pulse high level duty	46.9	50.0	53.1	%
High-level horizontal output	V_{19H}	Horizontal output pulse high level	4.0	4.3	4.6	V
Low-level horizontal output	V_{19L}	Horizontal output pulse low level	—	0.2	0.5	V
Horizontal output free-running frequency	f_{HO}	Horizontal output frequency, when there is no horizontal sync. separation input	15.45	15.73	16.05	kHz
Hor. pull-in range	f_{HP}	Frequency at which horizontal sync. separation input frequency pulls in. Sync. signal 0.57 V[p-p].	±500	±600	—	Hz
Screen position fluctuation 1	H_{POS1}	Phase change of horizontal sync. signal and FBP, H-center (0A): 67 → 60	–1.70	–2.12	–2.55	µs
Screen position fluctuation 2	H_{POS2}	Phase change of horizontal sync. signal and FBP, H-center (0A): 67 → 6F	1.97	2.46	3.14	µs
Hold Down operation level	V_{HD}	Voltage at which X-ray input pin voltage holds down. Hold down pin reference voltage: 6.2 V	5.9	6.2	6.5	V
High-level lock det. output	LD_H	At horizontal AFC unlocked, RL = 56 kΩ	4.5	—	—	V
Low-level lock det. output	LD_L	At horizontal AFC locked, RL = 56 kΩ	—	—	0.7	V
BLK-in input threshold voltage	BLK_{ST}	Pin 18 threshold voltage (BLK is applied to RGB output stage only)	1.7	2.2	2.7	V
Vertical signal processing						
Ver. out pulse width	τ_{VO}	Pulse width at horizontally/vertically synchronized state	610	640	670	µs
High-level ver. out 1	V_{10H1}	Vertical output pulse high level pin 10: open	4.0	4.3	4.6	V
High-level ver. out 2	V_{10H2}	Vertical output pulse high level pin 10: – 0.2 mA	3.75	4.10	4.60	V
High-level ver. out 3	V_{10H3}	Vertical output pulse high level pin 10: – 0.5 mA	3.3	3.9	4.6	V

Note) Unless otherwise specified, refer to "• Typical conditions for testing" for the conditions of I^2C bus and each pin.

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Vertical signal processing (continued)						
Low-level ver. out	V_{10L}	Vertical output pulse low level	—	0	0.3	V
V_{OUT} free-running frequency	f_{VO}	Ver. out frequency, when there are no hor. and ver. sync. signals input.	58	60	62	Hz
Vertical pull-in range	f_{VP}	Sync. input: 2 V[p-p], measurement should be conducted from not pulled in state.	56	—	64	Hz
V_{OUT} position shift	V_{POS}	V position: min. → max.	—	31	—	H
I^2C processing						
SCL, SDA input threshold voltage	V_{SCL}, V_{SDA}		1.5	—	3.0	V
Sink capability at ACK	ACK	I = 3 mA when pull-up resistor is 1.6 kΩ	—	—	0.4	V
High level DAC output 1	V_{4H}	Pin 4 output DC voltage, 0D = 7F	8.25	8.75	9.25	V
High level DAC output 2	V_{40H}	Pin 40 output DC voltage, 0C = 7F	4.5	5.0	5.5	V
Low level DAC output 1	V_{4L}	Pin 4 output DC voltage, 0D = 00	0.60	0.90	1.20	V
Low level DAC output 2	V_{40L}	Pin 40 output DC voltage, 0C = 00	0	0.1	0.2	V

Note) Unless otherwise specified, refer to "• Typical conditions for testing" for the conditions of I^2C bus and each pin.

• Design reference data

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SW power supply						
Reference voltage-temperature characteristics	$\Delta V_{37}/T_a$	I_{37} = 2.4 mA, T = –20°C to +70°C	–1.4	–1.8	–2.2	mV/°C
SW input dynamic range	SW_D	1 V[p-p] is reference (0 dB), V_{CC1} = 9 V, V_{CC2} = 5 V	6	—	—	dB
Input clamp voltage	V_1, V_{46}, V_{48}	Without input, pin 1, pin 46 and pin 48 voltage	1.8	2.2	2.6	V
SW output voltage	V_3	Without input, pin 3 voltage	2.6	3.0	3.4	V
SW output–Y input DC difference voltage	$V_3 - V_{41}$	Without input, difference voltage between pin 3 and pin 41	1.0	1.2	—	V
SW output–H. Sync. DC difference voltage	$V_3 - V_6$	Without input, difference voltage between pin 3 and pin 6	1.0	1.2	—	V
SW output–V. Sync. DC difference voltage	$V_3 - V_5$	Without input, difference voltage between pin 3 and pin 5	1.0	1.2	—	V
Y signal processing						
Video maximum output voltage	E_{Omax}	Brightness: max.	—	7.5	—	V
Y signal input dynamic range	Y_{IN}	Input D range measurement, contrast: typ., sub-contrast: typ.	—	4.0	—	V[p-p]
Picture quality variable range 2	G_{S2}	Input: 0.2 V[p-p], sine wave, f = 2.5 MHz, sharpness: max./min.	—	13	—	dB

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y signal processing (continued)						
Contrast fluctuation with picture quality control	ΔA_{SC}	Input: 2.0 V[p-p], stair step, sharpness: max./min.	−300	—	+300	mV[p-p]
Brightness relative control sensitivity	ΔBR	Same as the above G/R, B/R, brightness: min. → max.	0.9	1	1.1	Times
Black level correction starting point voltage	V_{BLSTA}	BL start external resistor: 20 kΩ	—	53	—	IRE
Video signal output supply voltage dependency	$\Delta E_O / V_{CC}$	Input: 2.0 V[p-p], stair step, output amplitude change of V_{CC} = ±5%	—	0	0.25	V[p-p]/V
Output DC voltage ambient temperature dependency	$\Delta E_{ODC} / T_a$	Pedestal level change ratio, when T_a changes from 50°C to 75°C, contrast: max.,brightness: typ.	—	−1.8	—	mV/°C
Y S/N	$Y_{S/N}$	Input: 2.0 V[p-p], stair step, noise meter measurement, contrast: max., sharpness: min.	53	55	—	dB
Service SW operation 1	$SRSW_1$	Input: 2.0 V[p-p], stair step, service SW: Measurement of output amplitude, when SW is on.	—	10	150	mV[p-p]
Service SW operation 2	$SRSW_2$	Service SW: On, DC voltage measurement at no-appearance of V_{OUT} .	3.8	4.3	4.8	V
DC restoration ratio 2	T_{DC2}	2.0 V[p-p], stair step, APL det. = 20 kΩ	—	120	—	%
Trap center frequency	f_{0TRAP}	Difference from f = 3.579545 MHz	−70	—	+70	kHz
Delay amount of trap	τ_{TRAP}	f = 0.5 MHz, comparison of delay amount between trap on/off	—	40	—	ns
Temperature characteristics of trap attenuation amount	$\Delta G_{TRAP} / T_a$	f = 3.579545 MHz, −20°C to +70°C	23	—	—	dB
Temperature characteristics of trap frequency	$\Delta f_{TRAP} / T_a$	−20°C to +70°C	−50	—	+50	kHz
ACL start voltage	ACL_{STA}	Pin 33 voltage at which ACL starts to become effective	—	7.1	—	V
ACL stop voltage	ACL_{STO}	Pin 33 voltage at which ACL stops	—	2.9	—	V
ABL start voltage	ABL_{STA}	Pin 33 voltage at which ABL starts to become effective	—	4.0	—	V
ABL stop voltage	ABL_{STO}	Pin 33 voltage at which ABL stops	—	3.0	—	V
Color signal processing						
Maximum color difference output	e_{Omax}	Color bar input, brightness: min., color: max., pedestal to peak voltage	—	4.5	—	V[0-p]
Free-running frequency supply voltage dependency	$\Delta f_{CO} / V_{CC}$	V_{CC} = ±5%	−250	—	+250	Hz
VCO control sensitivity	β	Check change in oscillation frequency, when V_{APC} = 5.6 V to 5.8 V	—	2.8	—	Hz/mV

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Color signal processing (continued)						
Free-running frequency ambient temperature dependency	Δf_{CO} /T_a	Ambient temperature: −20°C to +70°C	—	−2.9	—	Hz/°C
Phase detection sensitivity	μ	{1/ ($\Delta\phi \times \beta$)} × 100	—	22.3	—	mV/deg
Phase hold characteristic	$\Delta\phi$	Change amount of tint, when f_{SC} is shifted by ±300 Hz	—	1.6	—	deg/ 100 Hz
Demodulation output frequency characteristic	Δf_{-3}	Frequency at which color output pin becomes −3 dB	—	1.1	—	MHz
Demodulation output supply voltage dependency	Δe_O /V_{CC}	Tint: typ., contrast: typ., V_{CC} ±5%, color: typ.	—	0	—	%
Demodulation output ambient temperature dependency	Δe_O /T_a	T_a = −20°C to +70°C, +25°C is typ.	—	±7	—	%
Tint Center shift	ΔT_C	Change amount of tint center, when B.P.F. is used and not.	—	±4	—	H
H.P.F. frequency characteristic	f_{HPF}	Gain at f = f_{SC}	—	−12	—	dB
H.P.F. group delay amount	τ_{HPF}	Group delay amount at f = f_{SC}	—	140	—	ns
Color killer tolerance 2	e_{K2}	B.P.F. on state	—	−43	—	dB
Chroma delay amount	τ_{CHO}	Delay from pin 36 input to pin 21 output	—	375	—	ns
C−Y/Y ratio	C−Y/Y	Color data, when C−Y/Y ratio becomes 1.0	—	40	—	H
RGB processing						
Y output amplitude fluctuation (trap on/off)	ΔE_{OTRAP}	2 V[p-p] staircase input, amplitude fluctuation at trap on/off	—	±10	—	%
Y output amplitude fluctuation (B.P.F. on/off)	ΔE_{OBPF}	2 V[p-p] staircase input, amplitude fluctuation at B.P.F. on/off	—	±10	—	%
Y output amplitude fluctuation (sharpness)	ΔE_{OSHARP}	2 V[p-p] staircase input, sharpness: min. → max.	—	±5	—	%
Spot killer operation	V_{SPK}	V_{CC1} voltage at which RB_{RGB} output becomes high, when pin 26 voltage = 8.25 V	—	7.6	—	V
Horizontal signal processing						
Sync. separation clamp voltage	V_5 , V_6	Clamp voltage of sync. separation input pin (pin 5 and pin 6)	—	1.4	—	V
Black out operation level	V_{BLOUT}	Voltage at which Y output blacks out when X-ray input pin voltage is raised from 0 V	—	6.3	—	V
Operating frequency at hold down	f_{HD}	Frequency of H_{OUT} at the time of hold down when X-ray input pin voltage is raised from 0 V	16.3	16.4	16.8	kHz
BGP start position	BGP_{STA}	Phase difference from rear edge of hor. sync. to BPG at horizontal AFC loop on	0.3	0.5	0.7	μs

■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

Note) The characteristics listed below are theoretical values based on the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Horizontal signal processing (continued)						
BGP pulse width	BGP_W	BGP width at horizontal AFC loop on	2.5	3.0	3.5	µs
FBP level 1	V_{FBP1}	AFC operation DC level at FBP input pin	1.4	2.0	2.2	V
FBP level 2	V_{FBP2}	HBLK operation DC level at FBP input pin	0.3	0.7	1.1	V
FBP delay operating range	τ_{FBP}	Range of normal operation, when delay amounts are being changed from raise of H_{OUT} to FBP center.	10.0	to	22.0	µs
Horizontal oscillation frequency temperature characteristics	$\Delta f_{HO}/T_a$	Change in ambient temperature from –20°C to +70°C	—	±100	—	Hz
Vertical signal processing						
V. BLK pulse width	$VBLK_W$	VBLK width at R,G,B out in horizontall/verticall synchronization	—	17.0	—	H
I^2C processing						
Each DAC precision for 4-bit, 5-bit, 6-bit	DAC1	1LSB = {data (max.) – data (min.)}/(2N–1)	0.1	1	1.9	LSB/step
Each DAC precision for 7-bit, 7+1-bit, (40) excluded	DAC2	1LSB = {data (max.) – data (min.)}/(2N–1)	0.1	1	1.9	LSB/step
Each DAC precision for 7-bit, 7+1-bit, (40) only	DAC3	1LSB = {data (max.) – data (min.)}/(2N–1)	–1	1	2	LSB/step
Each DAC precision for 7+1-bit (7F → 80)	DAC4	1LSB = {data (max.) – data (min.)}/(2N–1), sub address; 06, 07 (Change amount/total change amount) × 100	–9.25	–6.25	0	%

• Typical conditions for testing

1. Input signal
   1) Video: 10-step staircase, 2.0 V[p-p]
   2) Chroma: Color bar signal: Burst level 150 mV[p-p]
      Rainbow signal: Burst level 150 mV[p-p]
   3) Sync. signal: Video signal 1.5 V[p-p] to 2.5 V[p-p] for both horizontal and vertical sync. signal input
2. I^2C bus conditions

Sub address	Control	Data (H)	Sub address	Control	Data (H)
00	Color	40	08	Drive G	40
01	Tint	20	09	Drive B	40
02	Brightness	40	0A	Y-adjust, H-center	67
03	Contrast	3F	0B	Test, V-position	00
04	Sharpness	00	0C	DAC1	40
05	Cut off R	00	0D	DAC2	40
06	Cut off G	00	0E	SW	50
07	Cut off B	00			

■ Electrical Characteristics at T_a = 25°C (continued)

- Typical conditions for testing (continued)

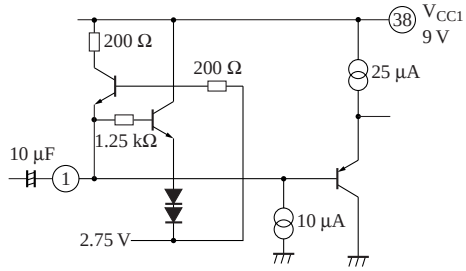
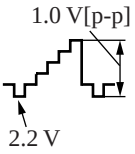
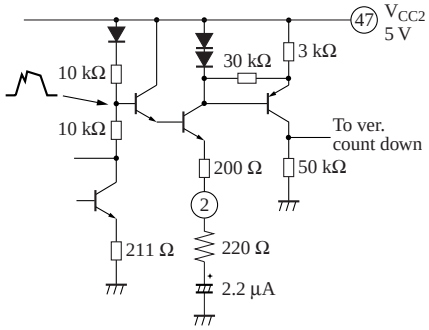
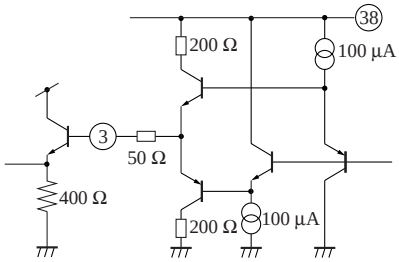
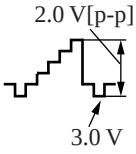
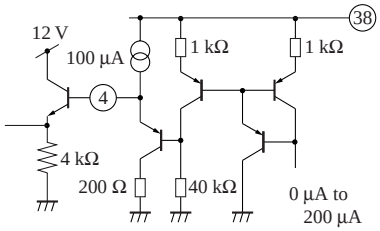
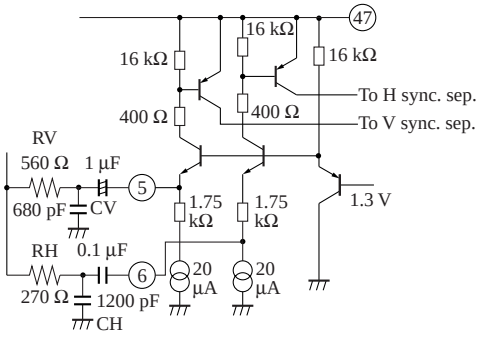
3. State of each pin

Pin No.	Symbol	State
18	BLK in	0 V
20	Y_S	1.1 V
24	Limiter	V_{CC1}
33	ABL/ACL	7.5 V
34	BL start	20 kΩ
35	BL det.	V_{CC1}
38	V_{CC1}	Applied from outside (9 V)
42	APL det.	0 V
47	V_{CC2}	5 V

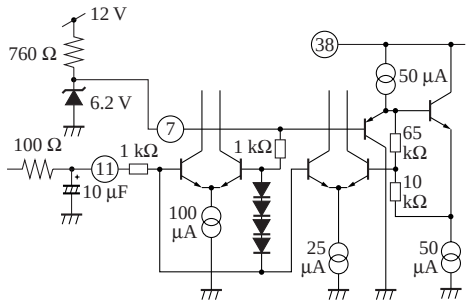
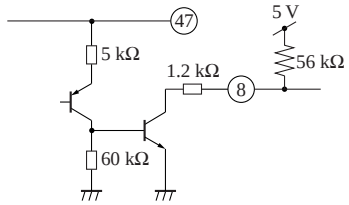
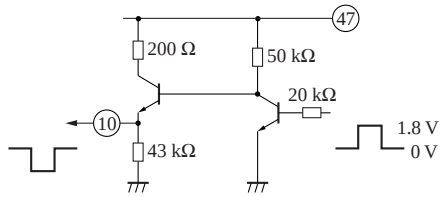
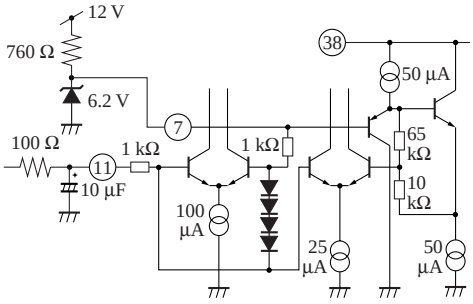
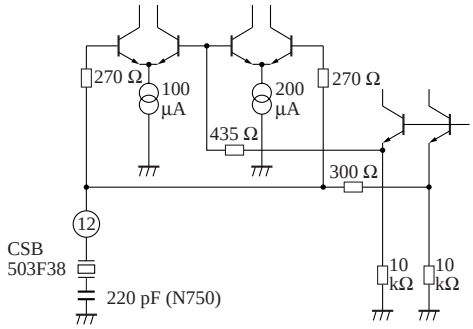
- Functions of SW controlled by I^2C bus

<table>
<tr><th>Data-bit</th><th>Functions of SW</th><th>Contents</th></tr>
<tr><td>0E-D0
0E-D1</td><td>AV SW changeover
<table><tr><th>D1</th><th>D0</th><th>Output</th></tr><tr><td>0</td><td>0</td><td>Video1</td></tr><tr><td>0</td><td>1</td><td>Video2</td></tr><tr><td>1</td><td>0</td><td>Video3</td></tr><tr><td>1</td><td>1</td><td>Mute</td></tr></table></td><td>1. Composite signal changeover
Input Video1: Pin 1
Video2: Pin 48
Video3: Pin 46
Output : Pin 3
2. No output at mute</td></tr>
<tr><td>0E-D2</td><td>Chroma trap SW
(0 → without trap)
(1 → with trap)</td><td>1. Video circuit chroma trap changeover
(Y signal phase leads by about 40 ns at trap off (through))</td></tr>
<tr><td>0E-D3</td><td>Chroma B.P.F. SW
(0 → without B.P.F.)
(1 → with B.P.F.)</td><td>1. Chroma circuit band-pass filter changeover
(Video signal delay amount varies according to B.P.F. on/off)</td></tr>
<tr><td>0E-D4
0E-D7</td><td>EE/VV SW
<table><tr><th>D7</th><th>D4</th><th>Killer out</th><th>f_{SC} out</th></tr><tr><td>0</td><td>0</td><td>Killer result</td><td>Yes</td></tr><tr><td>0</td><td>1</td><td>Open</td><td>No</td></tr><tr><td>1</td><td>0</td><td>Killer result</td><td>Yes</td></tr><tr><td>1</td><td>1</td><td>Open</td><td>Yes</td></tr></table></td><td>1. Tuner (EE) and VTR (VV) changeover
In principle change over by D4
Tuner (EE): Killer result is output
f_{SC} is output
VTR (VV): Killer result is not output
f_{SC} is not output
However, f_{SC} is output if D7 = 1 even at VV.
Killer out: Pin 45, f_{SC} out: Pin 31</td></tr>
<tr><td>0E-D5</td><td>SSW (service SW)
(0 → normal)
(1 → service mode)</td><td>1. At service mode (no vertical scanning, white balance adjustment)
Vertical output pulse stops (DC about 4.3 V)
Y output off, chroma output small</td></tr>
<tr><td>0E-D6</td><td>BLK off SW
(0 → normal)
(1 → output without BLK)</td><td>1. RGB output blanking (BLK) off changeover
To be used when RGB output signal without BLK is required.</td></tr>
</table>

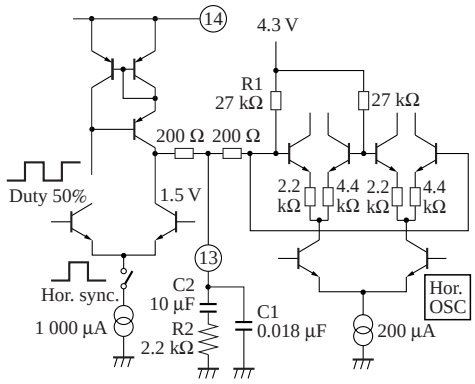
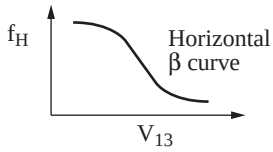
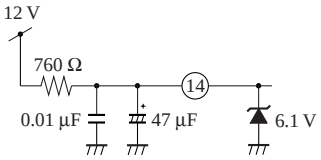
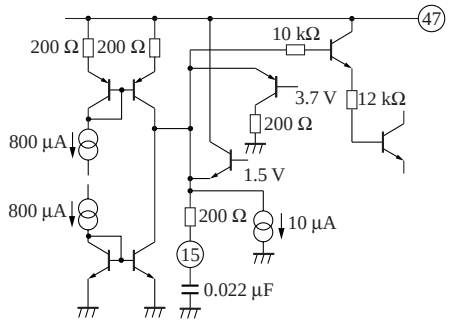
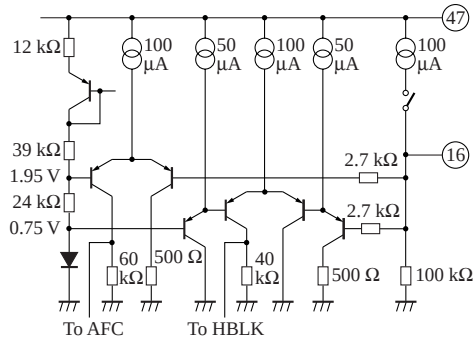
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Voltage
1		Video signal input pin 1: • Video signal input pin • Typical input 1.0 V[p-p] • Input through capacitor, and sync. top is clamped at 2.2 V • Input video signal with low impedance	AC 
2		Vertical signal clamp pin: • Peak clamp pin for separating vertical sync. signal	AC $f = f_V$ 
3		Video signal output pin: • Outputs signals inputted from pin 1, pin 46 and pin 48 • Control of output signal is carried out by I^2C bus • Recommended range of use is from –2 mA to +2 mA	AC 
4		DAC output pin 1: • Output voltage is adjustable in 128 stages (7-bit organization) by sub-address of I^2C bus (0D). • Recommended range of use is from –70 μA to +70 μA	DC 0.95 V to 8.75 V
5 6		Pin 5: Vertical sync. separation input pin: Pin 6: Horizontal sync. separation input pin: • $R_V > R_H$ so that slice level is made deep for vertical sync. and shallow for horizontal sync. • Cutoff frequency determined by R_H and CH shall be about 500 kHz. • R → large, slice level becomes deeper. (Weak in sync. compression) • R → small, slice level is shallow. (Weak in fluctuation such as V sag)	AC 2 V[p-p] 

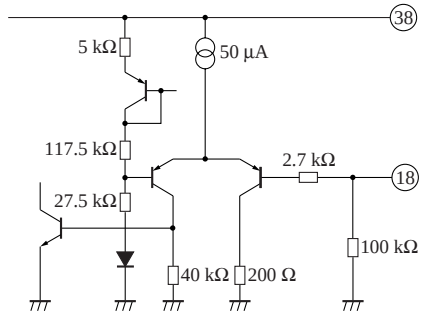
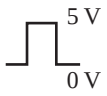
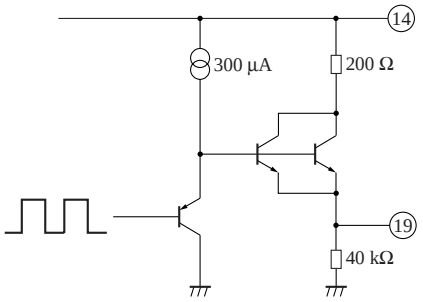
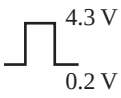
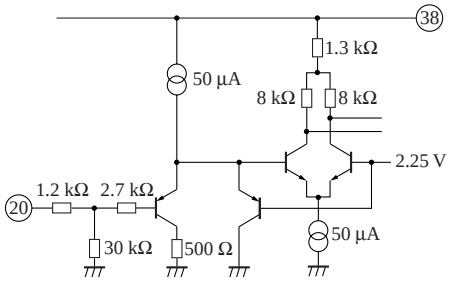
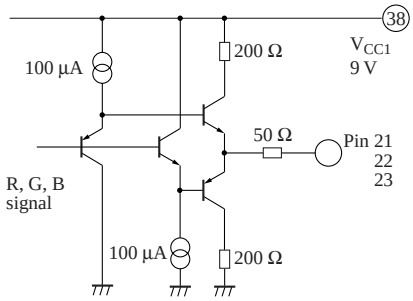
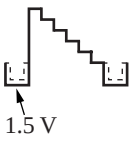
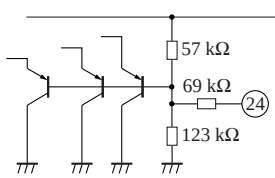
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
7		Hold down reference voltage pin: • Operates hold down by comparing voltage inputted to pin 11 $V_7 > V_{11}$: Normal operation $V_7 < V_{11}$: Out of horizontal sync. $V_7 + 0.1\ V < V_{11}$: Output with all BLK. • Recommended range of use is from 3 V to 7 V	DC 6.2 V
8		Lock detection output pin: • Pin which outputs whether vertical sync. signal of input and H_{OUT} are synchronizing. • Recommended range of use is from 0 mA to 0.2 mA	DC 0.7 V or less at lock, 4.5 V or more at unlock
9	—	GND pin: • Sync. system GND	—
10		Vertical pulse output pin: • Negative polarity, pulse width 10H • Recommended range of use is from – 0.7 mA to 0 mA	AC 4.3 V 0 V
11		Hold down reference voltage pin: • Voltage in proportion to a high-tension of CRT is applied.	DC
12		Horizontal oscillation pin: • Oscillates at $32f_H \cong 503$ kHz by means of ceramic oscillator element • Makes horizontal and vertical pulse by internal countdown circuit of IC.	AC $f = 32f_H$ (approx. 503 kHz)

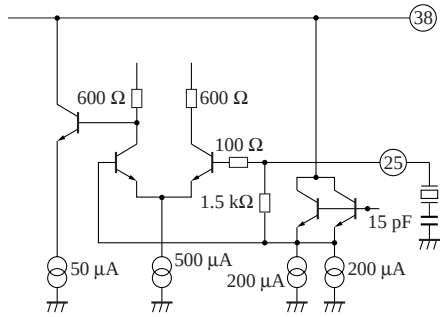
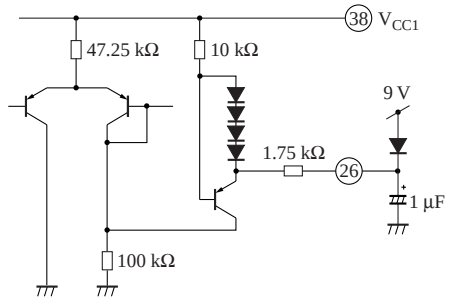
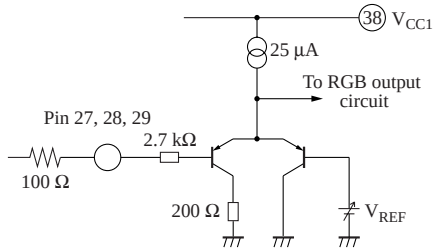
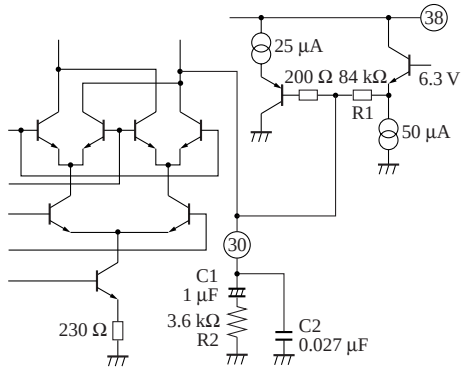
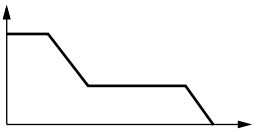
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
13		Horizontal AFC1 filter pin: • Charges and discharges the capacitor connected to pin 13 after comparing the phase of horizontal sync. signal and pulse inside IC. • R1, R2, C1 and C2 are lag-lead filter for AFC1. 	DC typ. 4.3 V
14		Horizontal stabilized power supply pin: • Stabilized power supply for horizontal circuit. A constant voltage circuit is inside. • Recommended range of use is from 6 mA to 12 mA	DC 6.1 V
15		Lock detection pin: • Detects phase of horizontal sync. signal and horizontal output pulse, and outputs the results. • Color control becomes minimum and chroma output becomes zero in asynchronous. • Pin 15 becomes low in out of sync.	DC In synchronization approx. 4.5 V In asynchronization approx. 0.7 V
16		FBP input pin: • FBP input pin for horizontal blanking and AFC circuit. • Threshold level HBLK: 0.75 V AFC: 1.9 V • Burst gate pulse monitor pin Current is flowing out at BGP timing • Voltage input of 0 V or less is inhibited • Recommended range of use is from 0 V to 5 V	AC FBP 
17	—	GND pin: • Main GND	—

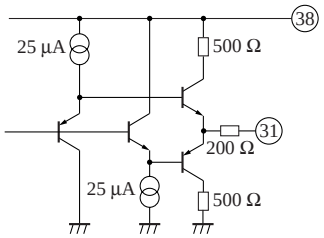
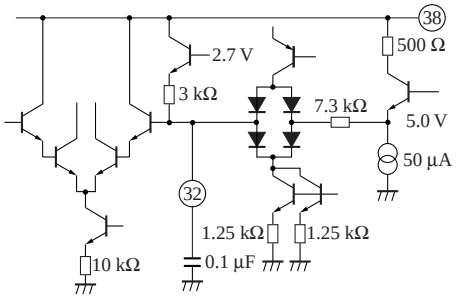
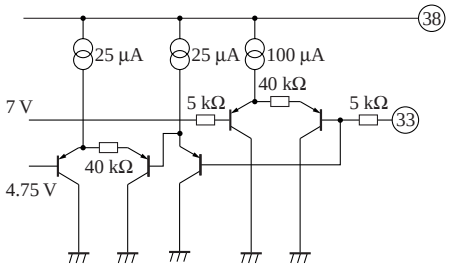
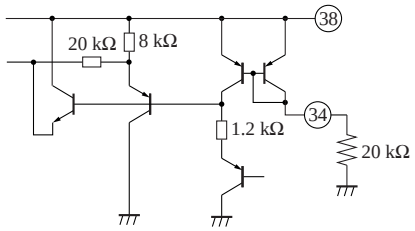
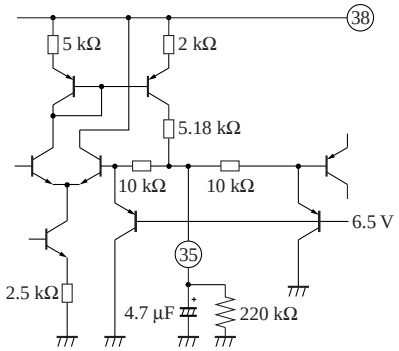
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
18		Blanking pulse input pin: • Input threshold voltage: 2.1 V • Operation V_{18} <1.6 V: Normal operation V_{18} >2.6 V: RGB outputs are blanked • Recommended range of use is from 0 V to 5 V	AC 
19		Horizontal pulse output pin: • Output pulse duty is 50% • Recommended range of use is from –7 mA to 0 mA	AC Pulse 
20		Y_S input pin: • Fast blanking input pulse input pin for OSD • Input threshold voltage 1.6 V Low: Normal output High: OSD output • Recommended range of use is from 0 V to 5 V	AC Pulse 
21 22 23		Pin 21: B output pin: Pin 22: G output pin: Pin 23: R output pin: • Those are R,G,B output pin • Recommended range of use is from –2 mA to +2mA	AC 
24		Output limiter pin: • This pin determines the voltage to clip high side of R,G,B output. • R,G,B output is clipped at 6.8 V at open. • Recommended range of use is from 0 V to V_{CC1}	DC

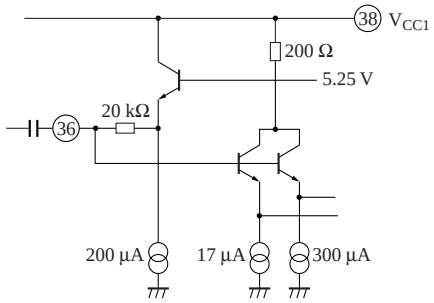
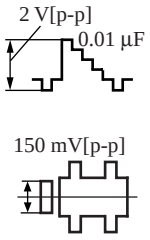
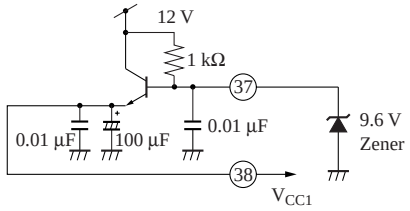
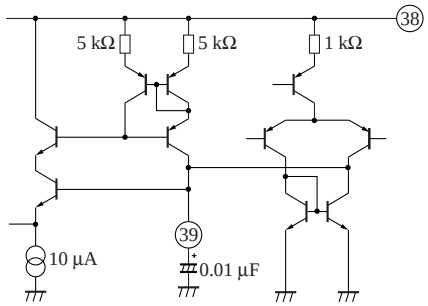
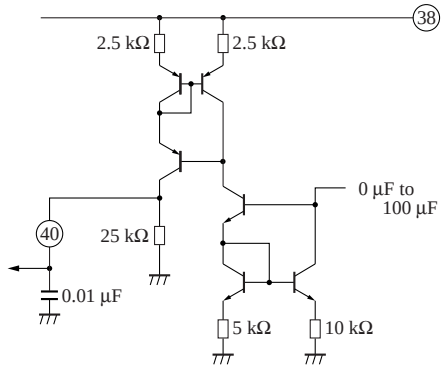
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
25		Chroma oscillation pin: • Pattern of pin and oscillator element should be as short as possible. f = 3.58 MHz	AC $f = f_{C0}$ approx. 0.3 V[p-p]
26		Spot killer pin: • This is used for quick discharging CRT electric charge, when set power is turned off. • Operating speed varies by changing external capacitance • Recommended range of use is from 0 V to 9 V	DC
27 28 29		Pin 27: External B input pin: Pin 28: External G input pin: Pin 29: External R input pin: • External input pin for OSD • Input limit voltage varies according to contrast control level • Recommended range of use is from 0 V to 5.5 V	AC 
30		Chroma APC filter pin: • Filter pin for APC detection circuit (operates for BGP period). • External R2 → larger, detection sensitivity becomes larger. (It is tends to be pulled in easily but tends to be affected by noise) • Lag-lead filter is organized by R1, R2, C1 and C2 	DC 5.5 V

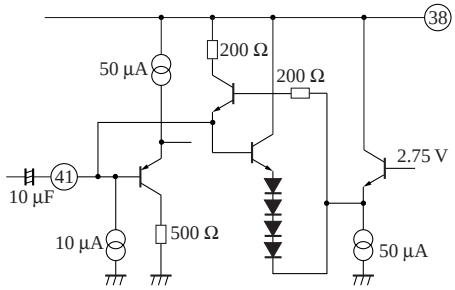
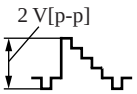
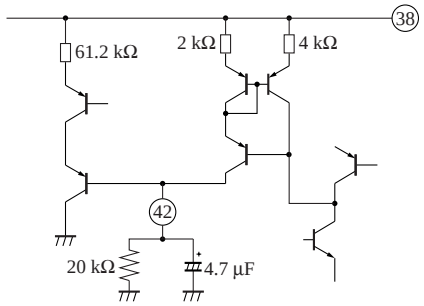
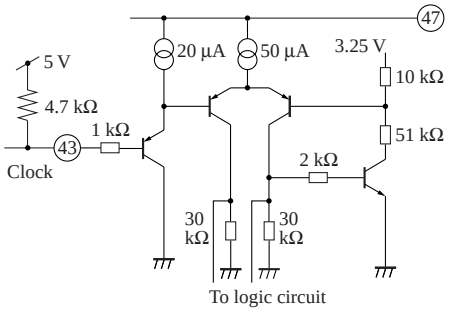
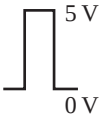
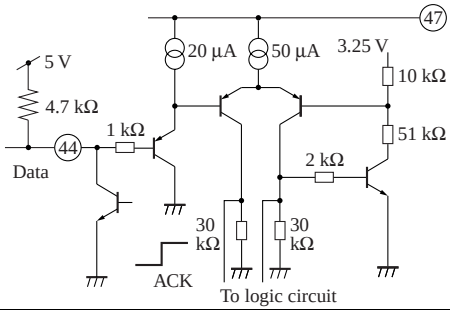
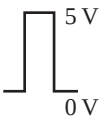
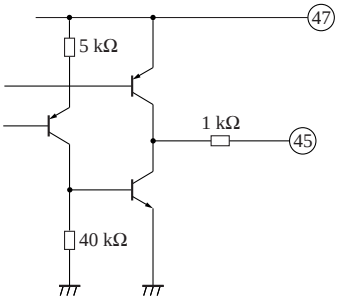
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
31		Subcarrier output pin: • Controls output by 0E-D4, D7 of I^2C bus. • There is f_{SC} output. DC: 6.1 V, AC: 350 mV[p-p] • There is no f_{SC} output. DC: 1.9 V, AC: 0 mV[p-p] • Recommended range of use is from – 0.4 mA to +0.4 mA	f_{SC} 300 mV[p-p]  DC
32		Killer filter pin: • Filter pin for killer detection circuit (operates for BGP period) High: Killer on (B&W) Low: Killer on (color)	DC
33		ABL/ACL pin: • Apply voltage inversely proportional to brightness of CRT screen. • Operating range is 7 V to 2 V • Controls contrast and brightness in inverse proportion to applied voltage • Recommended range of use is from 0 V to V_{CC1}	DC
34		Black extension start adjusting pin: • When current flowing out of this pin becomes larger, black extension start point comes closer to white side. • Recommended range of use is from – 0.4 mA to +0.1 mA	DC
35		Black level detection filter pin: • Adjusts black level detection area • Recommended range of use is from 0 V to 8 V	DC

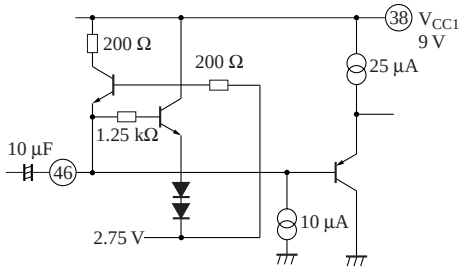
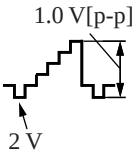
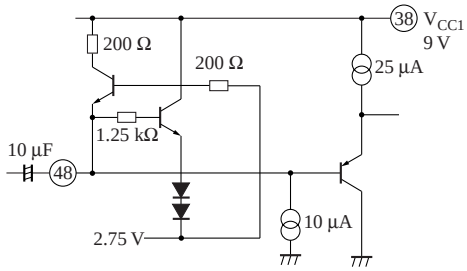
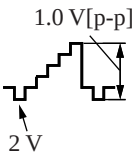
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
36		Chroma signal input pin: • 2 V[p-p] composite signal in using H.P.F. of IC inside. • Chroma signal of burst = 150 mV[p-p] at externally separating Y/C.	AC 
37		V_{CC1} reference voltage pin: • Reference voltage circuit for generating 9 V power supply. • Recommended range of use is from 1.5 mA to 4.5 mA	DC 9.6 V
38	—	Power supply pin V_{CC1}: • Power supply for chroma, video, RGB and AVSW. • Recommended range of use (typ.: 9 V)	DC
39		Capacitor pin for Y clamp: • Clamps the pedestal level of Y signal. • Place clamp capacitor close to pin.	DC
40		DAC output pin 2: • Output voltage is adjustable in 128 stages (7-bit organization) by I^2C sub-address (0C). • External circuit should be high impedance	DC 0 V to 5 V

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
41		Y signal input pin: • Video signal input pin. • Input 2 V[p-p] signal.	AC 
42		Y signal APL detection filter pin: • Current flows out according to APL and is smoothed by external CR to generate DC voltage.	DC
43		SCL pin (for I²C bus): • Low-level input: 1.5 V or less • High-level input: 3.0 V or more • Recommended range of use is from 0 V to V_{CC2}	AC (Pulse) 
44		SDA pin (for I²C bus): • Low-level input: 1.5 V or less • High-level input: 3.5 V or more • ACK sink capability: 3 mA • Recommended range of use is from 0 V to V_{CC}	AC (Pulse) 
45		Killer output pin: • Output pin of killer detection circuit • Output logic At color: Low At B&W: High However, if 0E-D4 is set at "1" by I²C bus, output becomes open. • Recommended range of use is from –300 µA to +300 µA	DC

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage
46		Video signal input pin 3: • Video signal input pin • Typical input 1.0 V[p-p] • Input should be done through capacitor, and sync. top is clamped at 2.0 V. • Video signal should be inputted in low impedance	AC 
47	—	Power supply pin (V_{CC2}: 5 V): • I^2C • To be used for sync. block • Using range from 4.75 V to 5.25 V (typ.: 5 V)	DC
48		Video signal input pin 2: • Video signal input pin • Typical input 1.0 V[p-p] • Input should be done through capacitor, and sync. top is clamped at 2.0 V. • Video signal should be inputted in low impedance	AC 

Note) 1. Do not apply external currents or voltages to any pins not specifically mentioned.
For circuit currents, '+' denotes current flowing into the IC, and '–' denotes current flowing out of the IC.

2. The following pins are not resistant to surge so that the precautions should be observed when using this IC.
The + side surge withstanding voltage for pin 15, pin 16 and pin 18 is approximately 200 V when a surge source capacitance is 200 pF. Do not apply a surge voltage higher than that.

■ Application Circuit Example