256K x 16 CMOS 3.3V Static RAM

Features

- ☐ High-speed access times
  - Com'l: 8, 10, 12, 15, and 20 ns
  - Ind: 12, 15, and 20 ns
- ☐ Low power operation (typical)
  - PDM31564SA
    Active: 300 mW
    Standby: 25mW
- ☐ High-density 256K x 16 architecture
- ☐ 3.3V (±0.3V) power supply
- ☐ Fully static operation
- ☐ TTL-compatible inputs and outputs
- ☐ Output buffer controls: $\overline{OE}$
- ☐ Data byte controls: $\overline{LB}$, $\overline{UB}$
- ☐ Packages:
  Plastic SOJ (400 mil) - SO
  Plastic TSOP (II) - T

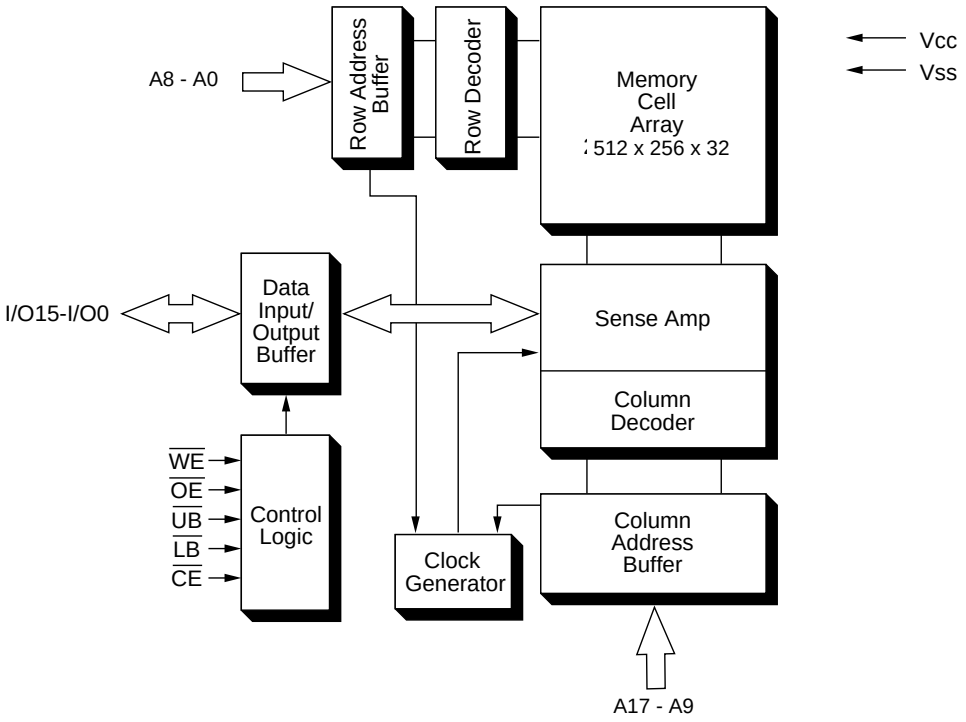
Description

The PDM31564 is a high-performance CMOS static RAM organized as 262,144 x 16 bits. The PDM31564 features low power dissipation using chip enable ($\overline{CE}$) and has an output enable input ($\overline{OE}$) for fast memory access. Byte access is supported by upper and lower byte controls.

The PDM31564 operates from a single 3.3V power supply and all inputs and outputs are fully TTL-compatible.

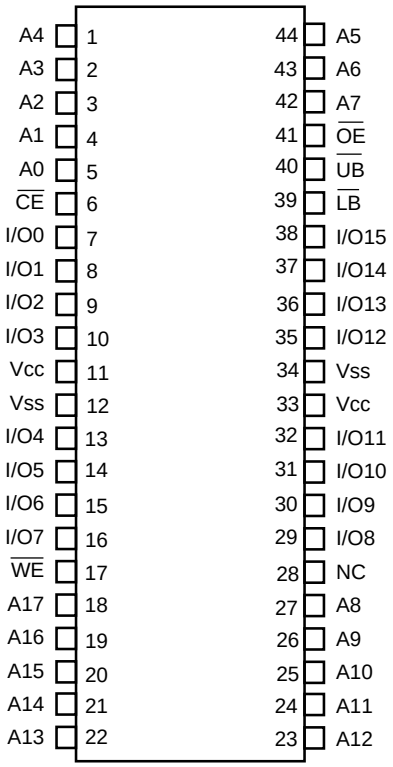
The PDM31564 is available in a 44-pin 400-mil plastic SOJ and a plastic TSOP package for high-density surface assembly and is suitable for use in high-speed applications requiring high-speed storage.

Functional Block Diagram

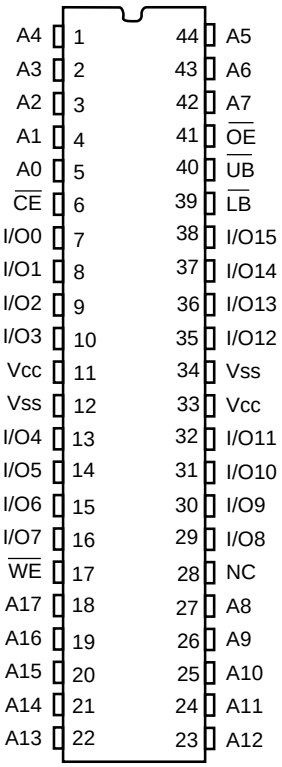


Pin Configuration

TSOP (II)



SOJ



Pin Description

Name	Description
A17-A0	Address Inputs
I/O15-I/O0	Data Inputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
$\overline{LB}$, $\overline{UB}$	Data Byte Control Inputs
NC	No Connect
V_{ss}	Ground
V_{CC}	Power (+3.3V)

Capacitance (T_A = +25°C, f = 1.0 MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = V_{SS}$	6	pF
$C_{I/O}$	Output Capacitance	$V_{I/O} = V_{SS}$	8	pF

NOTE: This parameter is determined by device characterization, but is not production tested.

Operating Mode

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O7-I/O0	I/O15-I/O8	Power
Read	L	L	H	L	L	Output	Output	I_{CC}
				H	L	High Impedance	Output	I_{CC}
				L	H	Output	High Impedance	I_{CC}
Write	L	X	L	L	L	Input	Input	I_{CC}
				H	L	High Impedance	Input	I_{CC}
				L	H	Input	High Impedance	I_{CC}
Output Disable	L	H	H	X	x	High Impedance	High Impedance	I_{CC}
	L	X	X	H	H	High Impedance	High Impedance	I_{CC}
Standby	H	X	X	X	X	High Impedance	High Impedance	I_{SB}

NOTE: H = V_{IH}, L = V_{IL}, X = DON'T CARE

Absolute Maximum Ratings (1)

Symbol	Rating	Com'l.	Ind.	Unit
V_{TERM}	Terminal Voltage with Respect to V_{SS}	–0.5 to +4.6	–0.5 to +4.6	V
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
P_T	Power Dissipation	1.5	1.5	W
I_{OUT}	DC Output Current	50	50	mA
T_j	Maximum Junction Temperature (2)	125	145	°C

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form: $T_j = T_a + P * \theta_{ja}$ where T_a is the ambient temperature, P is average operating power and θ_{ja} the thermal resistance of the package. For this product, use the following θ_{ja} values:

   SOJ: 59° C/W
   TSOP: 87° C/W

Recommended DC Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
V_{SS}	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	–40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

DC Electrical Characteristics (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions		Min.	Max.	Unit
I_{LI}	Input Leakage Current	V_{CC} = Max., V_{IN} = Vss to V_{CC}	Com'l/ Ind.	–5	5	µA
I_{LO}	Output Leakage Current	V_{CC}= Max., $\overline{CE}$ = V_{IH}, V_{OUT} = Vss to V_{CC}	Com'l/ Ind.	–5	5	µA
V_{IL}	Input Low Voltage			–0.3(1)	0.8	V
V_{IH}	Input High Voltage			2.2	Vcc + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 8 mA, V_{CC} = Min.		—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4 mA, V_{CC} = Min.		2.4	—	V

NOTE: 1. V_{IL}(min) = –3.0V for pulse width less than 20 ns.

Power Supply Characteristics

		-8	-10	-12		-15		-20		
Symbol	Parameter	Com'l	Com'l	Com'l	Ind.	Com'l	Ind.	Com'l	Ind.	Unit
I_{CC}	Operating Current $\overline{CE}$ = V_{IL} f = f_{MAX} = 1/t_{RC} V_{CC} = Max. I_{OUT} = 0 mA	220	210	200	210	190	200	185	195	mA
I_{SB}	Standby Current $\overline{CE}$ = V_{IH} f = f_{MAX} = 1/t_{RC} V_{CC} = Max.	50	45	40	45	35	40	30	35	mA
I_{SB1}	Full Standby Current $\overline{CE}$ ≥ V_{CC} – 0.2V f = 0 V_{CC} = Max., V_{IN} ≥ V_{CC} – 0.2V or ≤ 0.2V	10	10	10	15	10	15	10	15	mA

NOTES: All values are maximum guaranteed values.

AC Test Conditions

Input pulse levels	V_{SS} to 3.0V
Input rise and fall times	2.5 NS
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

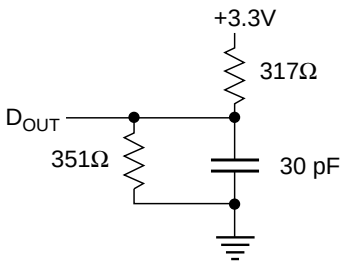


Figure 1. Output Load

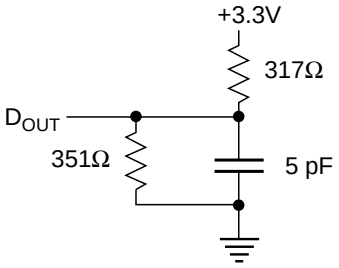
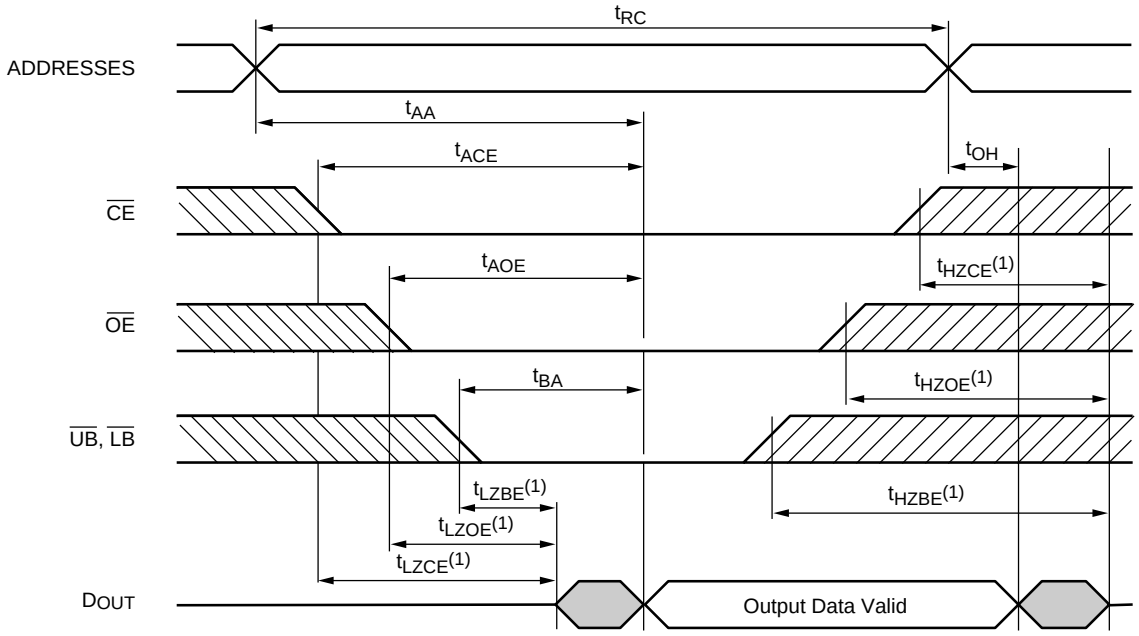


Figure 2. Output Load Equivalent (for t_{LZCE}, t_{HZCE}, t_{LZWE}, t_{HZWE}, t_{LZBE}, t_{HZBE}, t_{LZOE}, t_{HZOE})

Read Timing Diagram

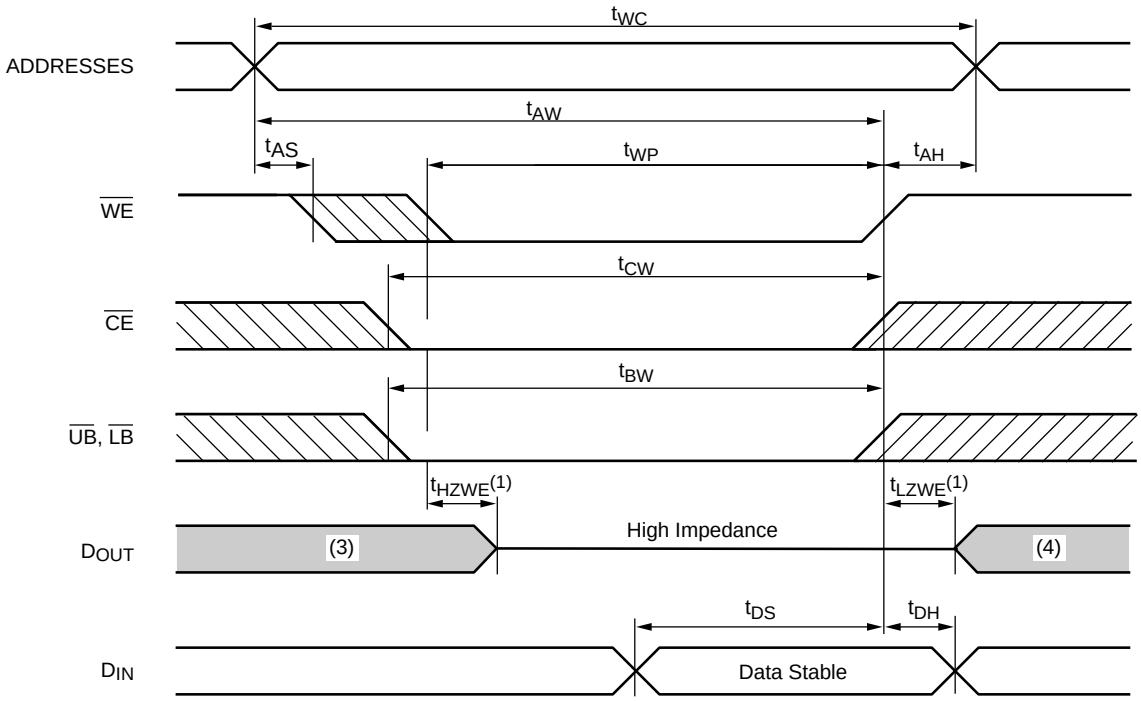


AC Electrical Characteristics

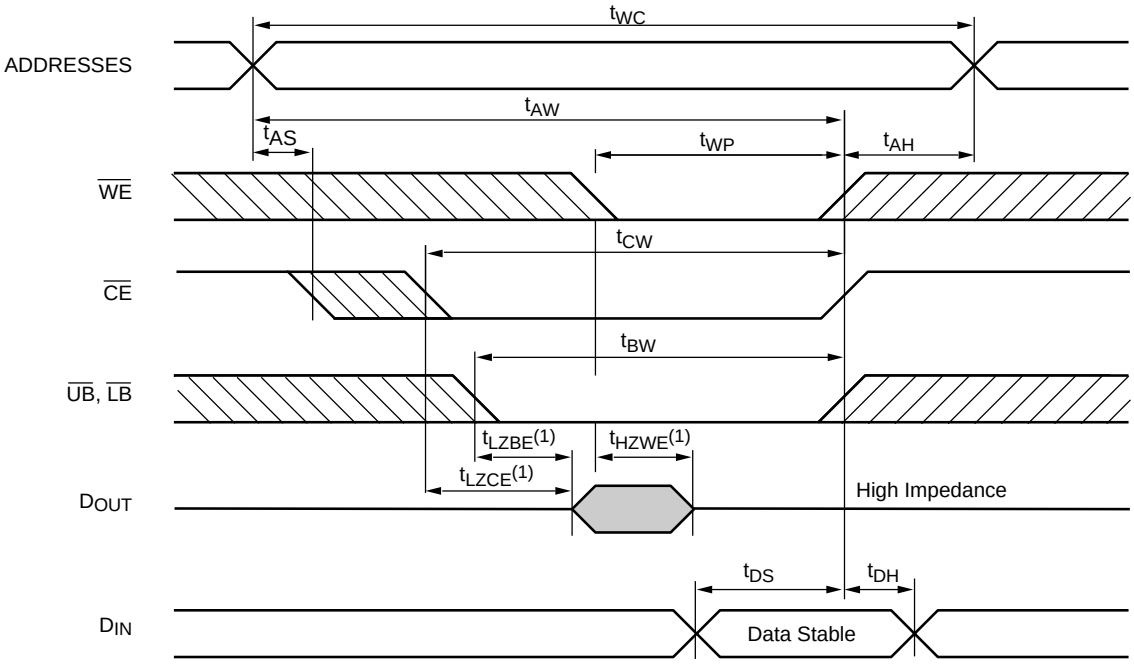
Description		-8*		-10*		–12		–15		–20		
READ Cycle	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
READ cycle time	t_{RC}	8	–	10	–	12	—	15	—	20	—	ns
Address access time	t_{AA}	–	8	–	10	—	12	—	15	—	20	ns
Chip enable access time	t_{ACE}	–	8	–	10	—	12	—	15	—	20	ns
Byte access time	t_{BA}	–	5	–	6	—	7	—	8	—	9	ns
Output hold from address change	t_{OH}	4	–	4	–	4	—	4	—	4	—	ns
Byte disable to output in low-Z[1]	t_{LZBE}	0	–	0	–	0	—	0	—	0	—	ns
Byte enable to output in high-Z[1]	t_{HZBE}	–	4	–	5	—	8	—	9	—	9	ns
Chip enable to output in low-Z[1]	t_{LZCE}	3	–	3	–	4	—	4	—	5	—	ns
Chip disable to output high-Z[1, 2]	t_{HZCE}	–	4	–	5	—	6	—	7	—	8	ns
Output enable access time	t_{AOE}	–	4	–	5	—	6	—	7	—	10	ns
Output enable to output in low-Z[1]	t_{LZOE}	0	–	0	–	0	—	0	—	0	—	ns
Output disable to output in high-Z[1, 2]	t_{HZOE}	–	4	–	5	—	5	—	6	—	6	ns

* V_{CC} = 3.3V ±5%

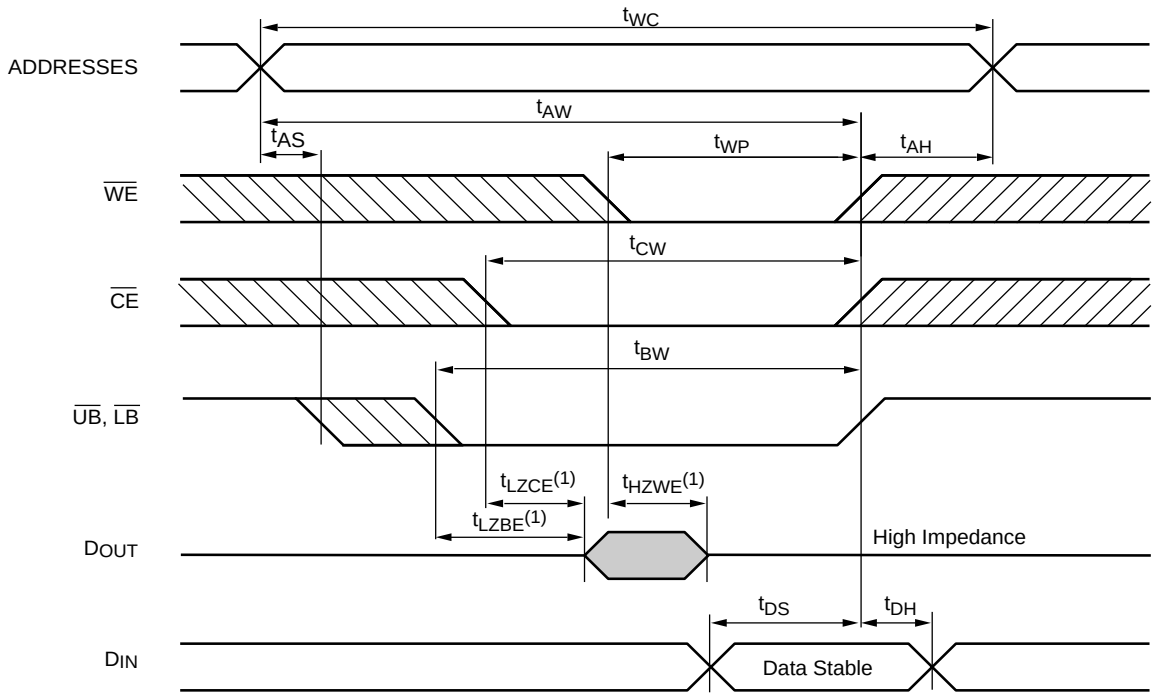
Write Cycle 1 Timing Diagram ($\overline{WE}$ Controlled)



Write Cycle 2 Timing Diagram ($\overline{CE}$ Controlled)



Write Cycle 3 Timing Diagram ($\overline{UB}$, $\overline{LB}$ Controlled)



AC Electrical Characteristics

Description		-8*		-10*		-12		-15		-20		
WRITE Cycle	**Sym**	**Min.**	**Max**	**Min.**	**Max**	**Min.**	**Max.**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
WRITE cycle time	t_{WC}	8	—	10	—	12	—	15	—	20	—	ns
Chip enable to end of write	t_{CW}	7	—	8	—	10	—	11	—	13	—	ns
Address valid to end of write	t_{AW}	7	—	8	—	10	—	11	—	13	—	ns
Byte pulse width	t_{BW}	7	—	8	—	10	—	12	—	13	—	ns
Address setup time	t_{AS}	0	—	0	—	0	—	0	—	0	—	ns
Address hold from end of write	t_{AH}	0	—	0	—	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	7	—	8	—	8	—	9	—	10	—	ns
Data setup time	t_{DS}	5	—	6	—	7	—	8	—	9	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	0	—	0	—	ns
Byte disable to output in low Z(1, 3, 4)	t_{LZBE}	0	—	0	—	0	—	0	—	0	—	ns
Byte enable to output in high Z(1, 3, 4)	t_{HZBE}	—	6	—	6	—	7	—	8	—	9	ns
Output disable to output in low Z(1, 3, 4)	t_{LZOE}	0	—	0	—	0	—	0	—	0	—	ns
Output enable to output in high Z(1, 3, 4)	t_{HZOE}	—	6	—	6	—	7	—	7	—	8	ns
Write disable to output in low Z(1,3, 4)	t_{LZWE}	0	—	0	—	0	—	0	—	0	—	ns
Write enable to output in high Z(1, 3, 4)	t_{HZWE}	—	6	6	—	—	7	—	7	—	9	ns

* V_{CC} = 3.3v ±5%

NOTES:

1. Parameter is determined by device characterization and is not production tested. See Figure 2 for load conditions.
2. If the $\overline{CE}$ LOW transition occurs coincident with or after the $\overline{WE}$ LOW transition, outputs remain in a high impedance state.
3. If the $\overline{CE}$ HIGH transition occurs coincident with or after the $\overline{WE}$ HIGH transition, outputs remain in a high impedance state.
4. If $\overline{OE}$ is HIGH during a write cycle, the outputs are in a high-impedance state during this period.

Ordering Information