

PE3293

Product Description

The PE3293 is a dual fractional-N phase-lock loop (PLL) IC designed for frequency synthesis and fabricated on Peregrine's patented UTSi® CMOS process. Each PLL includes a prescaler, phase detector, charge pump and on-board fractional spur compensation.

The patented spur compensation circuitry designed into the device ensures superior spur performance over the full temperature and VCO tuning range.

The PE3293 provides fractional-N division with power-of-two denominator values up to 32. This allows comparison frequencies up to 32 times the channel spacing, providing a lower phase noise floor than integer PLLs. The 32/33 RF prescaler (PLL1) operates up to 1.8 GHz and the 16/17 IF prescaler (PLL2) operates up to 550 MHz.

Applications

- Triple mode, dual-band PCS / Cellular handset
- PCS/CDMA/Cellular handsets
- PCS/CDMA/Cellular base stations

1.8 GHz / 550 MHz Dual Fractional-N Ultra-Low Spurious PLL for Frequency Synthesis

Features

- Industry leading fractional spur compensation: no adjusting required, stable over temp.
- Ultra-Low Power consumption: 4.0 mA typical, both loops operating
- Modulo-32 fractional-N main counters
- Supply voltage range 2.7 to 3.3 VDC

Figure 1. Block Diagram

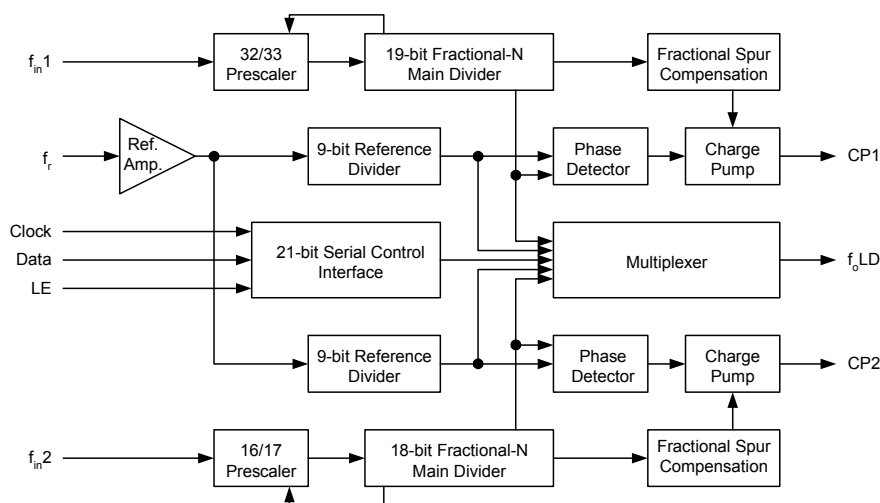
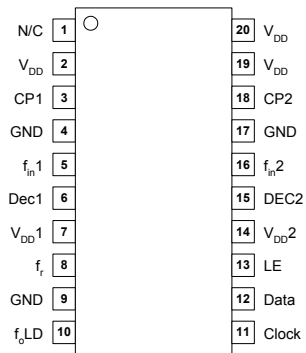


Figure 2. Pin Configuration: TSSOP (JEDEC MO-153-AC)

Table 1. Pin Descriptions

| Pin No. | Pin Name | Type | Description |
|---------|------------------|----------|---|
| 1 | N / C | | No connect. |
| 2 | V _{DD} | (Note 1) | Power supply voltage input. Input may range from 2.7 V to 3.6 V. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. |
| 3 | CP1 | Output | Internal charge-pump output from PLL1 for connection to a loop filter for driving the input of an external VCO. |
| 4 | GND | | Ground. |
| 5 | f _{in1} | Input | Prescaler input from the PLL1 (RF) VCO. Maximum frequency is 1.8 GHz. |
| 6 | Dec1 | | Power supply decoupling pin for PLL1. A capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. |
| 7 | V _{DD1} | | PLL1 prescaler power supply. 330 ohm resistor to V _{DD} . |
| 8 | f _r | Input | Reference frequency input. |
| 9 | GND | | Ground. |
| 10 | f _{0LD} | Output | Multiplexed output of the PLL1 and PLL2 main counters or reference counters, Lock Detect signals, and data out of the shift register. CMOS output (see Table 11, f _{0LD} Programming Truth Table). |
| 11 | Clock | Input | CMOS clock input. Serial data for the various counters is clocked in on the rising edge into the 21-bit shift register. |
| 12 | Data | Input | Binary serial data input. CMOS input data entered MSB first. The two LSBs are the control bits. |
| 13 | LE | Input | Load Enable CMOS input. When LE is high, data word stored in the 21-bit serial shift register is loaded into one of the four appropriate latches (as assigned by the control bits). |
| 14 | V _{DD2} | Output | PLL2 prescaler power supply. 330 ohm resistor to V _{DD} . |
| 15 | Dec2 | Output | Power supply decoupling pin for PLL2. A capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. |
| 16 | f _{in2} | Input | Prescaler input from the PLL2 (IF) VCO. Maximum frequency is 550 MHz. |
| 17 | GND | | Ground. |
| 18 | CP2 | Output | Internal charge-pump output for PLL2. For connection to a loop filter for driving the input of an external VCO. |
| 19 | V _{DD} | (Note 1) | Same as pin 2. |
| 20 | V _{DD} | (Note 1) | Same as pin 2. |

Note 1: V_{DD} pins 2, 19, and 20 are connected by diodes and must be supplied with the same voltage level.

Figure 3. Pin Configuration: 24-Pin BCC (Top View)

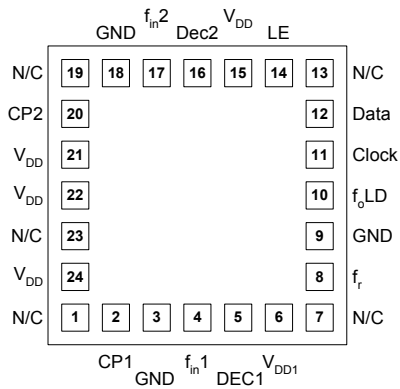


Table 2. Pin Descriptions

| Pin No. | Pin Name | Type | Description |
|---------|------------------|----------|---|
| 1 | N / C | | No connect. |
| 2 | CP1 | Output | Internal charge-pump output from PLL1 for connection to a loop filter for driving the input of an external VCO. |
| 3 | GND | | Ground |
| 4 | f _{in1} | Input | Prescaler input from the PLL1 (RF) VCO. Maximum frequency is 1.8 GHz. |
| 5 | Dec1 | | Power supply decoupling pin for PLL1. A capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. |
| 6 | V _{DD1} | | PLL1 prescaler power supply (FlexiPower 1). |
| 7 | N / C | | No connect. |
| 8 | f _r | Input | Reference frequency input. |
| 9 | GND | | Ground. |
| 10 | f _{oLD} | Output | Multiplexed output of the PLL1 and PLL2 main counters or reference counters, Lock Detect signals, and data out of the shift register. CMOS output (see Table 11, f _{oLD} Programming Truth Table). |
| 11 | Clock | Input | CMOS clock input. Serial data for the various counters is clocked in on the rising edge into the 21-bit shift register. |
| 12 | Data | Input | Binary serial data input. CMOS input data entered MSB first. The two LSBs are the control bits. |
| 13 | N / C | | No connect. |
| 14 | LE | Input | Load Enable CMOS input. When LE is high, data word stored in the 21-bit serial shift register is loaded into one of the four appropriate latches (as assigned by the control bits). |
| 15 | V _{DD2} | | PLL2 prescaler power supply. 330 ohm resistor to V _{DD} . |
| 16 | Dec2 | | Power supply decoupling pin for PLL2. A capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. |
| 17 | f _{in2} | Input | Prescaler input from the PLL2 (IF) VCO. Maximum frequency is 550MHz. |
| 18 | GND | | Ground. |
| 19 | N / C | | No connect. |
| 20 | CP2 | Output | Internal charge-pump output for PLL2. For connection to a loop filter for driving the input of an external VCO. |
| 21 | V _{DD} | (Note 1) | Power supply voltage input. Input may range from 2.7 V to 3.6 V. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. |

| Pin No. | Pin Name | Type | Description |
|---------|-----------------|----------|-----------------|
| 22 | V _{DD} | (Note 1) | Same as pin 21. |
| 23 | N / C | | No connect. |
| 24 | V _{DD} | (Note 1) | Same as pin 21. |

Note 1: V_{DD} pins 21, 22, and 24 are connected by diodes and must be supplied with the same voltage level.

PE3293 Description

The PE3293 is intended for such applications as the local oscillator for the RF and first IF of dual-conversion transceivers. The RF PLL (PLL1) includes a 32/33 prescaler with a 1.8 GHz maximum frequency of operation, where the IF PLL (PLL2) incorporates a 16/17 prescaler with a 550 MHz maximum frequency of operation. Using an advanced fractional-N phase-locked loop technique, the PE3293 can generate a stable, very low phase- noise signal. The dual fractional architecture allows fine resolution in both PLLs, with no degradation in phase noise performance.

Data is transferred into the PE3293 via a three-wire interface (Data, Clock, LE). Supply voltage can range from 2.7 to 3.6 volts for V_{DD}. PE3293 features very low power consumption and is available in a JEDEC MO-153-AC (TSSOP), 20-pin package and 24-lead BCC package.

Spurious Response

A critical parameter for synthesizer designs is spurious output. Spurs occur at the integer multiples of the step size away from center tone. An important feature of fractional synthesizers is their ability to reduce these spurious sidebands. The PE3293 has a built-in method for reducing these spurs, with no external components or tuning required. In addition, this circuitry works over the full commercial temperature and VCO tuning range.

Table 3. Absolute Maximum Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|--------------------|---------------------------|------|----------------|-------|
| V_{DD} | Supply voltage | -0.3 | 4.0 | V |
| V_{DD1}, V_{DD2} | Prescaler supply voltage | -0.3 | V_{DD} | V |
| V_I | Voltage on any input | -0.3 | $V_{DD} + 0.3$ | V |
| I_I | DC into any input | -10 | +10 | mA |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

Table 4. Operating Ratings

| Symbol | Parameter/Conditions | Min | Max | Units |
|--------------------|-------------------------------------|-----|----------|-------|
| V_{DD} | Supply voltage | 2.7 | 3.3 | V |
| V_{DD1}, V_{DD2} | Prescaler supply voltage | 0.8 | V_{DD} | °C |
| T_A | Operating ambient temperature range | -40 | 85 | °C |

Table 5. ESD Ratings

| Symbol | Parameter/Conditions | Level | Units |
|-----------|---------------------------------------|-------|-------|
| V_{ESD} | ESD voltage human body model (Note 1) | 2000 | V |

Note 1: Periodically sampled, not 100% tested. Tested per MIL-STD-883, M3015 C2

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 5.

Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Table 6. DC Characteristics
 $V_{DD} = 3.0\text{ V}$, $-40^\circ\text{ C} < T_A < 85^\circ\text{ C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|--|---|---------------------|-----|---------------------|---------------|
| I_{DD} | 3 V supply current | $C_{10}, C_{20} = 00$ (both PLLs on) | | 4.0 | | mA |
| I_{stby} | Total standby current | | | 5.0 | 50 | μA |
| Digital inputs: Clock, Data, LE | | | | | | |
| V_{IH} | High level input voltage | $V_{DD} = 2.7$ to 3.6 volts | $0.7 \times V_{DD}$ | | | V |
| V_{IL} | Low level input voltage | $V_{DD} = 2.7$ to 3.6 volts | | | $0.3 \times V_{DD}$ | V |
| I_{IH} | High level input current | $V_{IH} = V_{DD} = 3.6$ volts | -1 | | +1 | μA |
| I_{IL} | Low level input current | $V_{IL} = 0, V_{DD} = 3.6$ volts | -1 | | +1 | μA |
| Reference Divider input: f_r | | | | | | |
| I_{IHR} | Input current | $V_{IH} = V_{DD} = 3.6$ volts | | | +25 | μA |
| I_{ILR} | Input current | $V_{IL} = 0, V_{DD} = 3.6$ volts | -25 | | | μA |
| Digital output: f_oLD | | | | | | |
| V_{OLD} | Output voltage LOW | $I_{out} = 1\text{ mA}$ | | | 0.4 | V |
| V_{OHD} | Output voltage HIGH | $I_{out} = -1\text{ mA}$ | $V_{DD} - 0.4$ | | | V |
| Charge Pump outputs: CP1, CP2 | | | | | | |
| $I_{CP - Source}$ | Drive current | $V_{CP} = V_{DD} / 2$ | | -70 | | μA |
| $I_{CP - Sink}$ | | | | -70 | | μA |
| I_{CPL} | Leakage current | $0.5\text{ V} < V_{CP} < V_{DD} - 0.5\text{ volt}$ | -5 | | 5 | nA |
| $I_{CP - Source}$ vs. $I_{CP - Sink}$ | Sink vs. source mismatch | $V_{CP} = V_{DD} / 2, T_A = 25^\circ\text{ C}$ | | | 10 | % |
| I_{CP} vs T_A | Output current vs. temperature | $V_{CP} = V_{DD} / 2$ | | 10 | | % |
| I_{CP} vs. V_{CP} | Output current magnitude variation vs. voltage | $0.5\text{ V} < V_{CP} < V_{DD} - 0.5\text{ volt}, T_A = 25^\circ\text{ C}$ | | 10 | | % |

Table 7. AC Characteristics

$V_{DD} = 3.0\text{ V}$, $-40^\circ\text{ C} < T_A < 85^\circ\text{ C}$, unless otherwise specified

| Symbol | Parameter | Conditions | Min | Max | Units |
|--|---|-------------------------------|-----|------|------------------|
| Control Interface and Latches (see figure 6) | | | | | |
| f_{Clock} | Serial data clock frequency | | | 10 | MHz |
| t_{ClockH} | Serial clock HIGH time | | 50 | | ns |
| t_{ClockL} | Serial clock LOW time | | 50 | | ns |
| t_{DSU} | Data set-up time to Clock rising edge | | 50 | | ns |
| $t_{\text{DHL D}}$ | Data hold time after Clock rising edge | | 10 | | ns |
| t_{LEW} | LE pulse width | | 50 | | ns |
| t_{CLE} | Clock falling edge to LE rising edge | | 50 | | ns |
| t_{LEC} | LE falling edge to Clock rising edge | | 50 | | ns |
| $t_{\text{Data Out}}$ | Data Out delay after Clock falling edge (f_{oLD} pin) | $C_L = 50\text{ pf}$ | | 90 | ns |
| Main Divider (Including Prescaler) | | | | | |
| $f_{\text{in}1}$ | Operating frequency | | 300 | 1800 | MHz |
| $f_{\text{in}2}$ | Operating frequency | | 45 | 550 | MHz |
| $Pf_{\text{in}1}$ | Input level range | External AC coupling | -7 | 5 | dBm |
| $Pf_{\text{in}2}$ | Input level range | External AC coupling | -10 | 5 | dBm |
| f_c | Comparison frequency | | | 10 | MHz |
| Reference Divider | | | | | |
| f_r | Operating frequency | | | 50 | MHz |
| V_{fr} | Input sensitivity | External AC coupling (note 1) | 0.5 | | $V_{\text{P-P}}$ |

Note 1: CMOS logic levels may be used if DC coupled.

Functional Description

The Functional Block Diagram in Figure 5 shows a 21-bit serial control register, a multiplexed output, and PLL sections PLL1 and PLL2. Each PLL contains a fractional-N main counter chain, a reference counter, a phase detector, and an internal charge pump with on-chip fractional spur compensation. Each fractional-N main counter chain includes an internal dual modulus prescaler, supporting counters, and a fractional accumulator.

Serial input data is clocked on the rising edge of Clock, MSB first. The last two bits are the address bits that determine the register address. Data is transferred into the counters as shown in Table 8, PE3293 Register Set. If the f₀LD pin is configured as data out, then the contents of shift register bit S₂₀ are clocked on the falling edge of Clock onto the f₀LD pin. This feature allows the PE3293 and compatible devices to be connected in a daisy-chain configuration.

The PLL1 (RF) VCO frequency f_{in1} is related to the reference frequency f_r by the following equation:

$$f_{in1} = [(32 \times M_1) + A_1 + (F_1/32)] \times (f_r/R_1)$$

(1) Note that A₁ must be less than or equal to M₁. Also, f_{in1} must be greater than or equal to 1024 x (f_r/R₁) to obtain contiguous channels.

The PLL2 (IF) VCO frequency f_{in2} is related to the reference frequency f_r by the following equation:

$$f_{in2} = [(16 \times M_2) + A_2 + (F_2/32)] \times (f_r/R_2)$$

(2) Note that A₂ must be less than or equal to M₂. Also, f_{in2} must be greater than or equal to 256 x (f_r/R₂) to obtain contiguous channels.

F₁ sets PLL1 fractionality. If F₁ is an even number, the PE3293 automatically reduces the fraction. For example, if F₁ = 12, then the fraction 12/32 is automatically reduced to 3/8. In this way, fractional denominators of 2, 4, 8, 16 and 32 are available. F₂ sets the fractionality for PLL2 in the same manner.

Figure 4. Functional Block Diagram

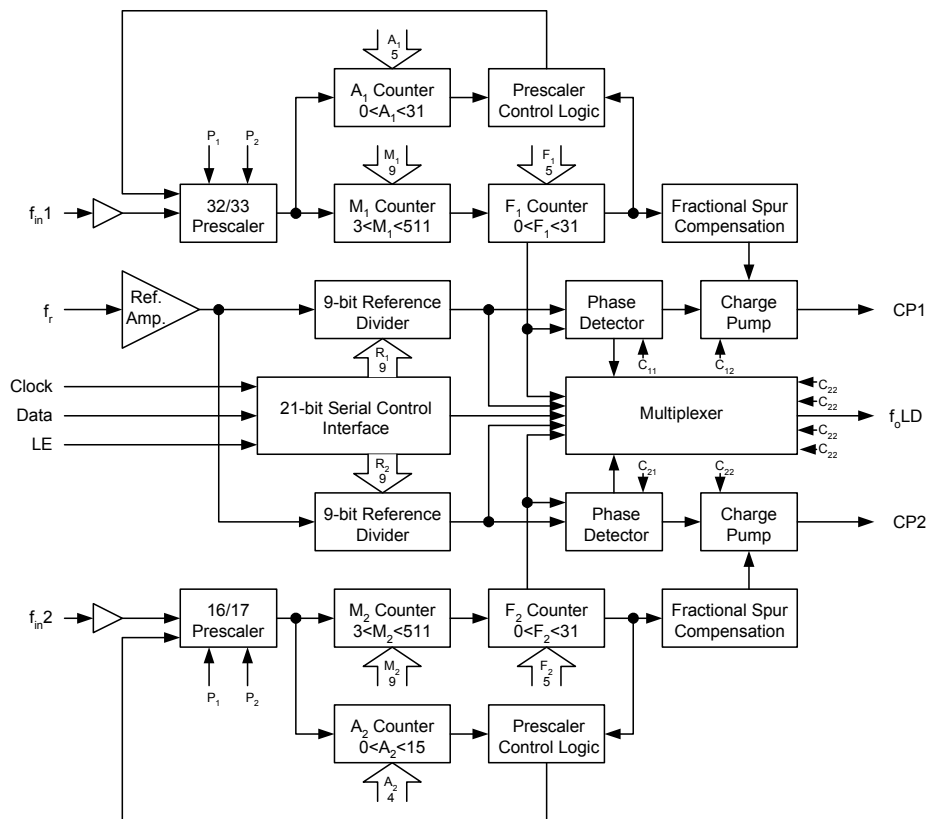


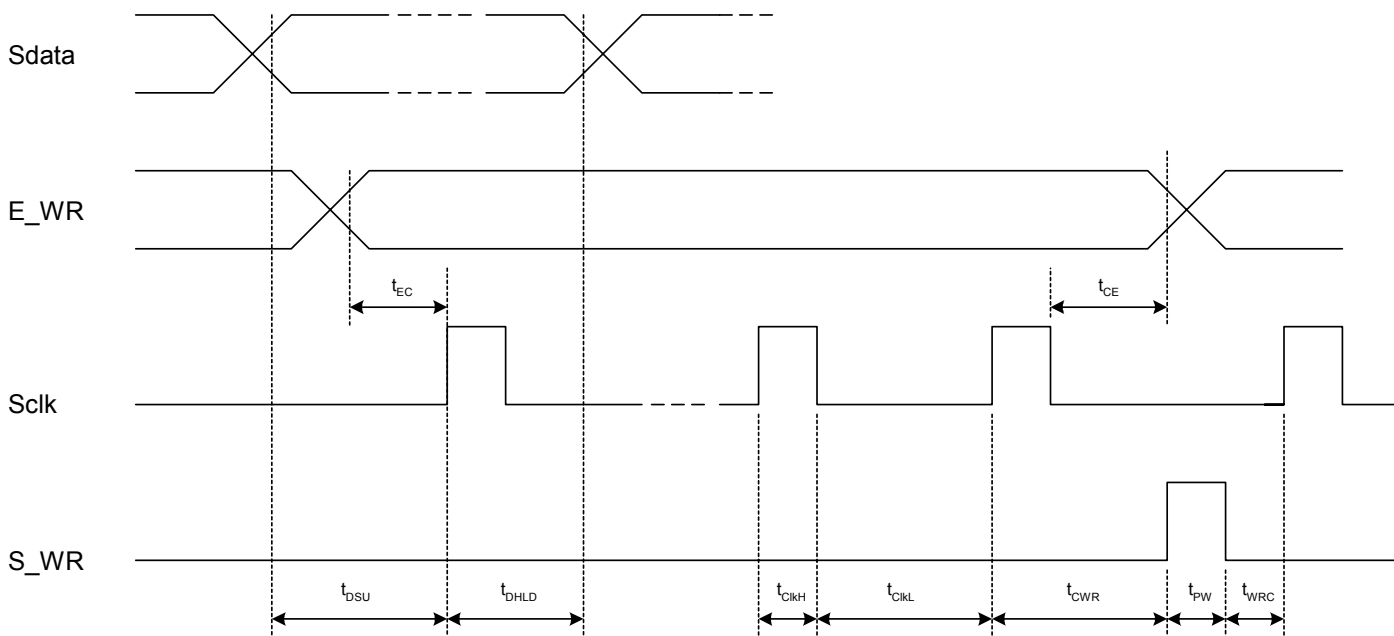
Table 8. Register Set

| | | | | | | | | | | | | | | | | | | | | |
|---|---|-----------------|-----------------|--------------------------|--------------------------|-----------------|-----------------|-----------------|--|--|-----------------|-----------------|-----------------|--|-----------------|-----------------|-----------------|-----------------|----------------|----------------|
| S ₂₀ | S ₁₉ | S ₁₈ | S ₁₇ | S ₁₆ | S ₁₅ | S ₁₄ | S ₁₃ | S ₁₂ | S ₁₁ | S ₁₀ | S ₉ | S ₈ | S ₇ | S ₆ | S ₅ | S ₄ | S ₃ | S ₂ | S ₁ | S ₀ |
| Reserved | | | | Test | PLL2 Synthesizer control | | | | | PLL2 Reference counter R ₂ divide ratio | | | | | | | | Address | | |
| | | | | 0 | C ₂₄ | C ₂₃ | C ₂₂ | C ₂₁ | C ₂₀ | R ₂₈ | R ₂₇ | R ₂₆ | R ₂₅ | R ₂₄ | R ₂₃ | R ₂₂ | R ₂₁ | R ₂₀ | 0 | 0 |
| Res. | PLL2 Main counter M ₂ divide ratio | | | | | | | | | PLL2 Swallow counter A ₂ divide ratio | | | | PLL2 Fractional counter F ₂ numerator value | | | | | Address | |
| | M ₂₈ | M ₂₇ | M ₂₆ | M ₂₅ | M ₂₄ | M ₂₃ | M ₂₂ | M ₂₁ | M ₂₀ | A ₂₃ | A ₂₂ | A ₂₁ | A ₂₀ | F ₂₄ | F ₂₃ | F ₂₂ | F ₂₁ | F ₂₀ | 0 | 1 |
| Res. | FlexiPower voltage regulation | | | PLL1 Synthesizer control | | | | | PLL1 Reference counter R ₁ divide ratio | | | | | | | | Address | | | |
| | P ₂ | Res. | P ₁ | C ₁₄ | C ₁₃ | C ₁₂ | C ₁₁ | C ₁₀ | R ₁₈ | R ₁₇ | R ₁₆ | R ₁₅ | R ₁₄ | R ₁₃ | R ₁₂ | R ₁₁ | R ₁₀ | 1 | 0 | |
| PLL1 Main counter M ₁ divide ratio | | | | | | | | | PLL1 Swallow counter A ₁ divide ratio | | | | | PLL1 Fractional counter F ₁ numerator value | | | | | Address | |
| M ₁₈ | M ₁₇ | M ₁₆ | M ₁₅ | M ₁₄ | M ₁₃ | M ₁₂ | M ₁₁ | M ₁₀ | A ₁₄ | A ₁₃ | A ₁₂ | A ₁₁ | A ₁₀ | F ₁₄ | F ₁₃ | F ₁₂ | F ₁₁ | F ₁₀ | 1 | 1 |

↑
MSB (first in)

↑
(last in) LSB

Figure 5. Serial Interface Mode Timing Diagram



Programmable Divide Values (R1, R2, F1, F2, A1, A2, M1, M2)

Data is clocked into the 21-bit shift register, MSB first. When LE is asserted HIGH, data is latched into the registers addressed by the last two bits shifted into the 21-bit register, according to Table 8. For example, to program the PLL1 (RF) swallow counter, A₁, the last two bits shifted into the register (S₀, S₁) would be (1,1). The 5-bit A₁ counter would then be programmed according to Table 9. For normal operation, S₁₆ of address (0,0) (the Test bit) must be programmed to 0 even if PLL2 (IF) is not used.

Table 9. PE3293 Counter Programming Example

| Divide Value | MSB | | | | LSB | Address | |
|--------------|-----------------|-----------------|-----------------|-----------------|-----------------|----------------|----------------|
| | S ₁₁ | S ₁₀ | S ₉ | S ₈ | S ₇ | S ₁ | S ₀ |
| | A ₁₄ | A ₁₃ | A ₁₂ | A ₁₁ | A ₁₀ | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 2 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| - | - | - | - | - | - | 1 | 1 |
| 31 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Program Modes

Several modes of operation can be programmed with bits C₁₀ - C₁₄ and C₂₀ - C₂₄, including the phase detector polarity, charge pump high impedance, output of the f_{oLD} pin and power-down modes. The PE3293 modes of operation are shown on Table 10. The truth table for the f_{oLD} output is shown in Table 11.

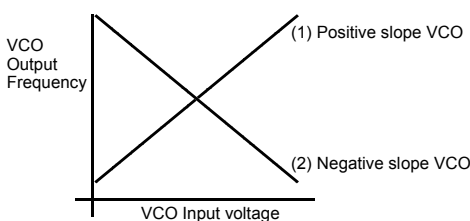
Table 10. PE3293 Program Modes

| S ₁₅ | S ₁₄ | S ₁₃ | S ₁₂ | S ₁₁ | S ₁ | S ₀ |
|---------------------------------|---------------------------------|---|--|---|----------------|----------------|
| C ₂₄ See Table 10 | C ₂₃ See Table 10 | C ₂₂ 0 = PLL1 CP normal 1 = PLL1 CP High Z | C ₂₁ (Note 2) 0 = PLL2 Phase Detector inverted 1 = PLL2 Phase Detector normal | C ₂₀ (Note 1) 0 = PLL2 on 1 = PLL2 off | 0 | 0 |
| C ₁₄ See Table 10 | C ₁₃ See Table 10 | C ₁₂ 0 = PLL1 CP normal 1 = PLL1 CP High Z | C ₁₁ (Note 2) 0 = PLL1 Phase Detector inverted 1 = PLL1 Phase Detector normal | C ₁₀ (Note 1) 0 = PLL1 on 1 = PLL1 off | 1 | 0 |

Note 1: The PLL1 power-down mode disables all of PLL1's components except the R₁ counter and the reference frequency input buffer, with CP1 (pin 3) and f_{in1} (pin 5) becoming high impedance. The power down of PLL2 has similar results with CP2 (pin 18) and f_{in2} (pin 16) becoming high impedance. Power down of both PLL1 and PLL2 further disables counters R₁ and R₂, the reference frequency input, and the f_{oLD} output, causing f_r (pin 8) and f_{oLD} (pin 10) to become high impedance. The Serial Control Interface remains active at all times.

Note 2: The C₁₁ and C₂₁ bits should be set according to the voltage versus frequency slope of the VCO as shown in Figure 7. This relationship presumes the use of a passive loop filter. If an inverting active loop filter is used the relationship is also inverted.

Figure 6. VCO Characteristics



- When VCO1 (RF) slope is positive like (1), C₁₁ should be set HIGH.
- When VCO1 (RF) slope is negative like (2), C₁₁ should be set LOW.
- When VCO2 (IF) slope is positive like (1), C₂₁ should be set HIGH.
- When VCO2 (IF) slope is negative like (2), C₂₁ should be set LOW.

Table 11. f_oLD Programming Truth Table

X = don't care condition

| f _o LD Output State | C ₁₄ (PLL1F ₀) | C ₁₃ (PLL1LD) | C ₂₄ (PLL2F ₀) | C ₂₃ (PLL2LD) |
|---|--|-----------------------------|--|-----------------------------|
| Disabled (Note 1) | 0 | 0 | 0 | 0 |
| PLL 1 Lock detect (Note 2) (LD1) | 0 | 1 | 0 | 0 |
| PLL2 Lock detect (Note 2) (LD2) | 0 | 0 | 0 | 1 |
| PLL1 / PLL2 Lock detect (Note 2) | 0 | 1 | 0 | 1 |
| PLL1 Reference divider output (f _c 1) | 1 | X | 0 | 0 |
| PLL2 Reference divider output (f _c 2) | 0 | X | 1 | 0 |
| PLL1 Programmable divider output (f _p 1) | 1 | X | 0 | 1 |
| PLL2 Programmable divider output (f _p 2) | 0 | X | 1 | 1 |
| Serial data out | 1 | 0 | 1 | 0 |
| Reserved | 1 | 0 | 1 | 1 |
| Reserved | 1 | 1 | 1 | 0 |
| Counter reset (Note 3) | 1 | 1 | 1 | 1 |

Note 1: When the f_oLD is disabled the output is a CMOS LOW.

Note 2: Lock detect indicates when the VCO frequency is in "lock". When PLL1 is in lock and PLL1 lock detect is selected, the f_oLD pin will be HIGH with narrow pulses LOW. When PLL2 is in lock and PLL2 lock detect is selected, the f_oLD pin will be HIGH with narrow pulses LOW. When PLL1 / PLL2 lock detect is selected the f_oLD pin will be HIGH with narrow pulses LOW only when both PLL1 and PLL2 are in lock.

Note 3: The counter reset state when activated resets all counters. Upon removal of the reset, counters M, A, and F resume counting in close alignment with the R counter (the maximum error is one prescaler cycle). The reset bits can be activated to allow smooth acquisition upon powering up.

Programming the Pre-scaler

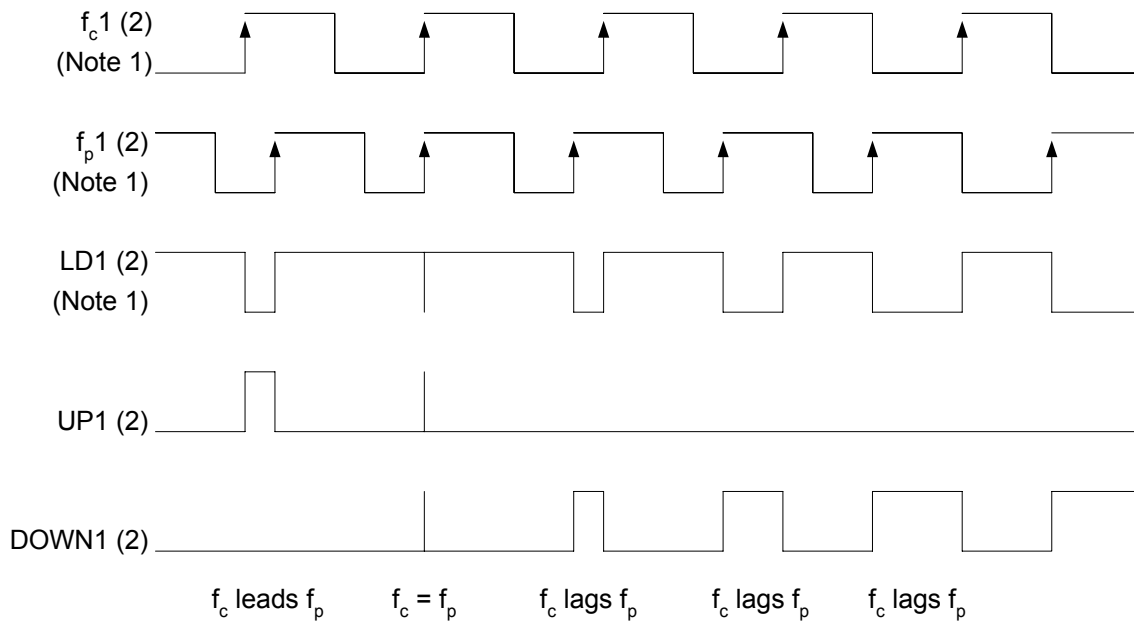
P₂ and P₁ are used for internal testing of the prescaler and must be programmed with 0,0 for normal PLL operation.

Phase Comparator Characteristics

PLL1 has the timing relationships shown below for f_c1 , f_p1 , LD1, UP1, and DOWN1. When $C_{11} = \text{HIGH}$, UP1 directs the internal PLL1 charge pump to source current and DOWN1 directs the PLL1 internal charge pump to sink current. If $C_{11} = \text{LOW}$, UP1 and DOWN1 are interchanged.

PLL2 has the timing relationships shown below for f_c2 , f_p2 , LD2, UP2, and DOWN2. When $C_{21} = \text{HIGH}$, UP2 directs the internal PLL2 charge pump to source current and DOWN2 directs the PLL2 internal charge pump to sink current. If $C_{21} = \text{LOW}$, UP2 and DOWN2 are interchanged.

Figure 7. Phase Comparator Timing Diagram



Note 1: $f_c1(2)$, $f_p1(2)$, and LD1(2) are accessible via the f_0 LD pin per programming in Table 11.

Loop Filter

Second/Third Order Loops

Choosing the optimum loop filter for a design encompasses many trade offs. The rule of thumb for choosing the loop filter bandwidth is 10 percent of the step size. A second order loop (C_1 C_2 R_2 and C_4 C_5 R_5 in Figure 9 omitting C_3 R_3 C_6 and R_6) will provide the least amount of components and the fastest lock times. If lock time is an issue, one might try opening up the loop filter, although if it is too wide, instability will dominate and worsen lock time. If lock time is not an issue, a narrower second order filter will minimize residual FM without requiring additional components.

Third Order loop filters (C_1 C_2 R_2 C_3 R_3 and C_4 C_5 R_5 C_6 R_6 in Figure 9) provide a good compromise between lock time and residual FM. We have found using a third order loop with 20 dB of rejection at the step size will halve the Residual FM as measured with a similar second order loop, with minimum effect on lock time.

Loop Filter Bandwidth Design Considerations

As part of the spur compensation circuitry, the PE329x series PLLs contain capacitors to ground internal to the charge pump. PLL1 contains a 50 pF capacitor and PLL2 contains a 100 pF capacitor. To ensure accurate loop filter calculations, it is critical that the calculated value of the first shunt capacitor (C_3 & C_4 in Figure 11) be at least 100 pF for PLL1 and 200 pF for PLL2. With this requirement satisfied, the remaining loop components can be calculated.

For a stable loop, it is also important that the loop bandwidth be less than or equal to one tenth of the step size.

Digital Control Lines

Control Line Noise

We have noticed frequency jitter during programming when a low impedance, such as a capacitor to ground, is placed next to any control line pin (clock, data, and load enable). The use of a 51 k ohm resistor in series with the control line will eliminate the problem with no effect to programming time.

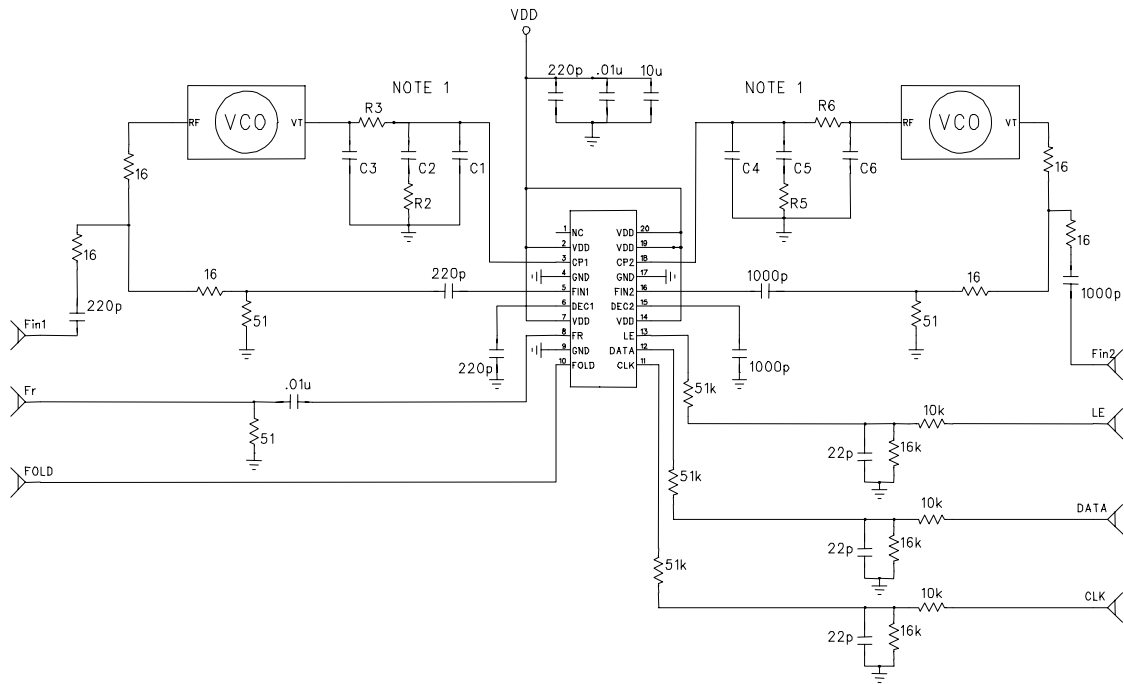
Enable Line Voltage

The PE329x series PLLs use a level sensitive load enable. Therefore the digital controller must provide an active low to the part at all times except when the data is to be loaded into the shift register. If the PLL controller does not hold the voltage low, a high impedance resistor to ground should be added to the enable line to ensure stable operation.

5 Volt Operation:

The PE329x series PLLs are not capable of accepting control voltages greater than 3.6 volts. Interface to 5 volt controllers requires the addition of resistor dividers to comply with the 3.6 volt maximum operation voltage.

Figure 8. Application Example



Note 1: For optimum fractional spur and lock-time performance C_2 and C_5 should be polyester (or poly propylene). In addition, the loop filter components must be free from contamination. Contamination will result in poor spur performance. For accurate loop bandwidth, C_3 must be greater than or equal to 100 pF, and C_4 must be greater than or equal to 200 pF.

Figure 9. Package Drawing

20-lead TSSOP (JEDEC MO-153-AC)

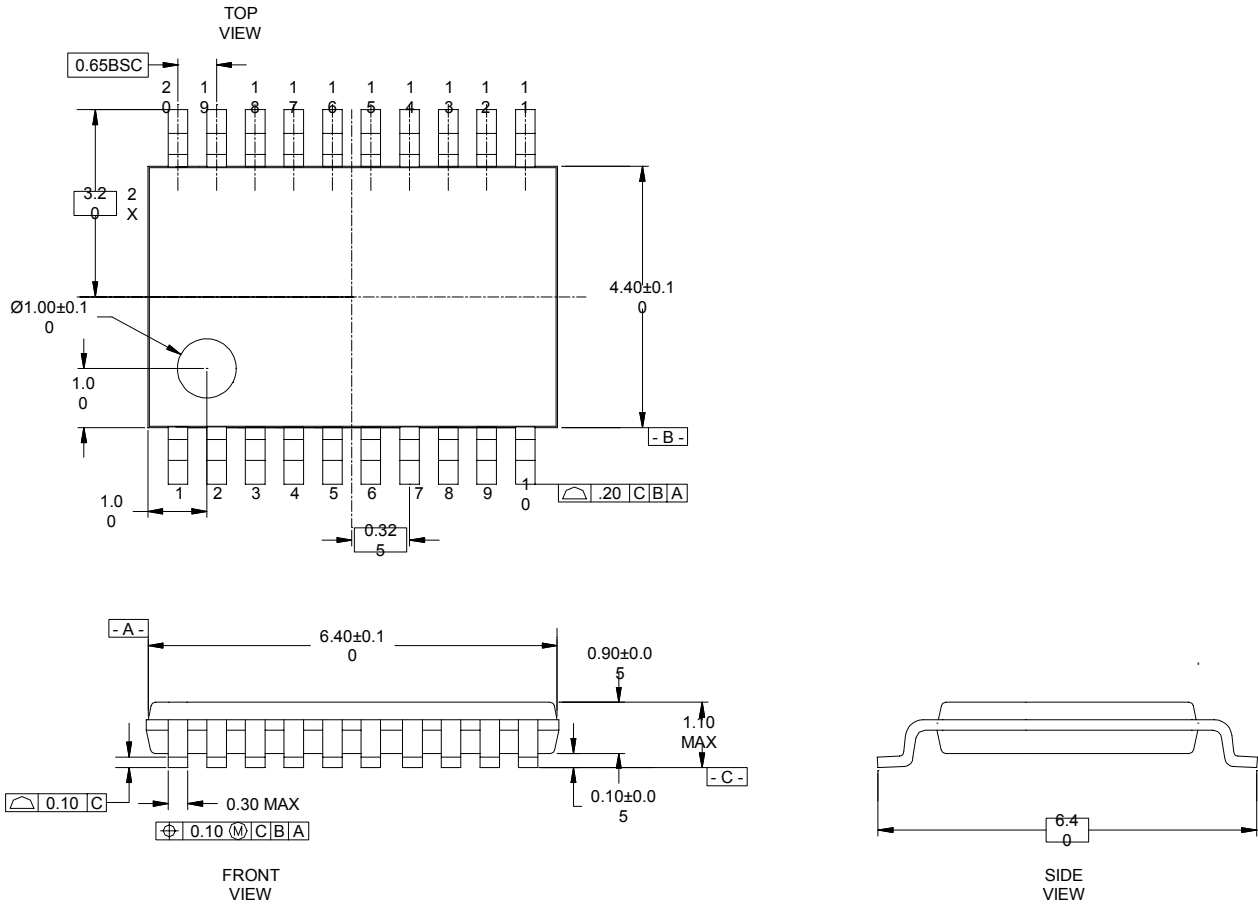


Figure 10. Package Drawing

24-lead BCC

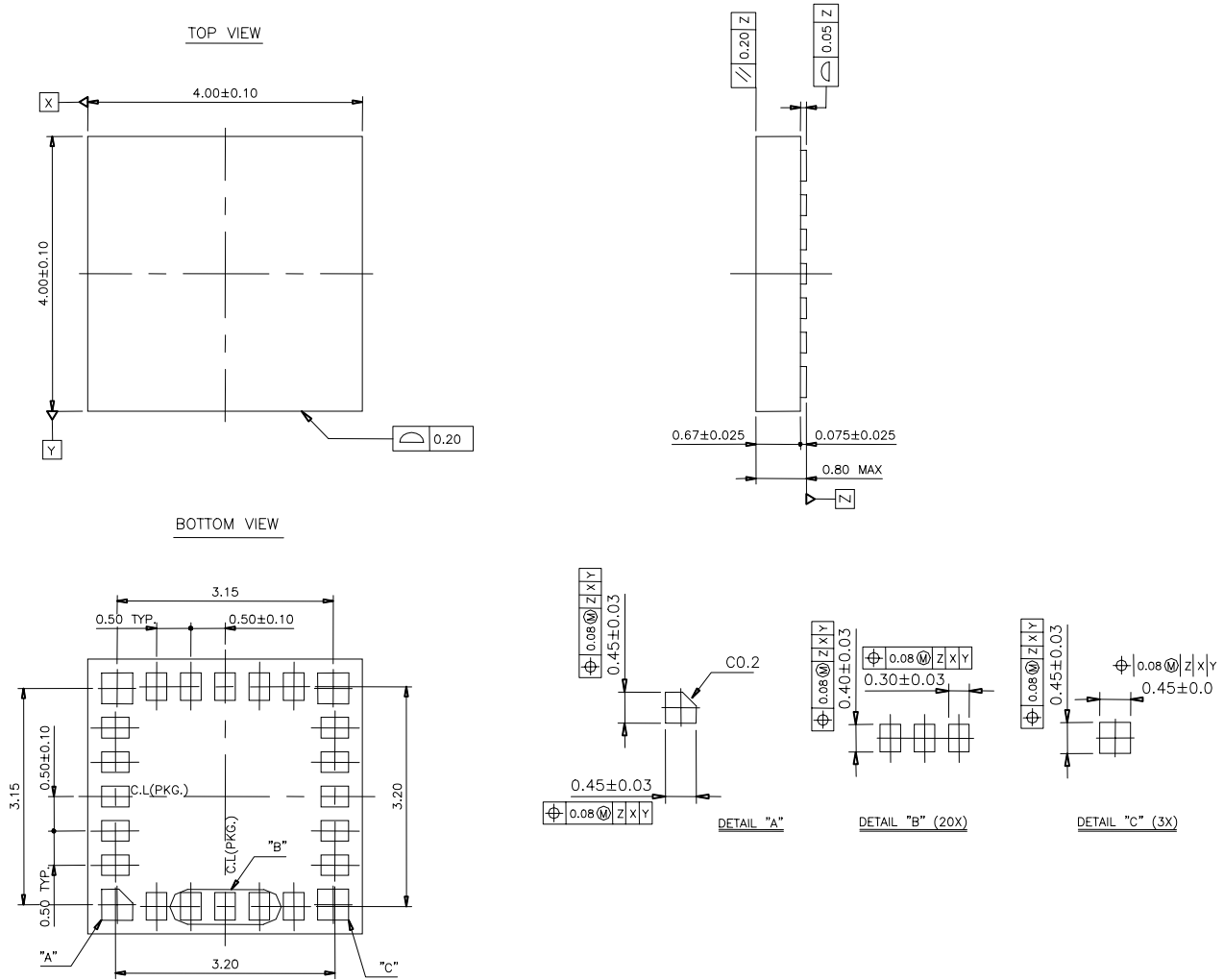


Table 12. Ordering Information

| Order Code | Part Marking | Description | Package | Shipping Method |
|-------------------|---------------------|---|----------------|------------------------|
| 3293-11 | PE3293 | Screened to datasheet specs., fully qualified | 20-lead TSSOP | 74 units / Tube |
| 3293-12 | PE3293 | Screened to datasheet specs., fully qualified | 20-lead TSSOP | 2000 unit / T&R |
| 3293-14 | 3293 | Screened to datasheet specs., fully qualified | 24-lead BCC | 640 Unit Trays |
| 3293-15 | 3293 | Screened to datasheet specs., fully qualified | 24-lead BCC | 2000 Unit T&R |
| 3293-00 | PE3293EK | Evaluation Board | 20-lead TSSOP | 1 / Box |
| 3293-04 | PE3293EK | Evaluation Board | 24-lead BCC | 1 / Box |

Sales Offices

United States

Peregrine Semiconductor Corp.

6175 Nancy Ridge Drive
San Diego, CA 92121
Tel 1-858-455-0660
Fax 1-858-455-0770

Europe

Peregrine Semiconductor Europe

Aix-En-Provence Office
Parc Club du Golf, bat 9
13856 Aix-En-Provence Cedex 3
France
Tel 33-0-4-4239-3360
Fax 33-0-4-4239-7227

Japan

Peregrine Semiconductor K.K.

The Imperial Tower, 15th floor
1-1-1 Uchisaiwaicho, Chiyoda-ku
Tokyo 100-0011 Japan
Tel: 03-3507-5755
Fax: 03-3507-5601

Australia

Peregrine Semiconductor Australia

8 Herb Elliot Ave.
Homebush, NSW 2140
Australia
Tel: 011-61-2-9763-4111
Fax: 011-61-2-9746-1501

For a list of representatives in your area, please refer to our Web site at: <http://www.peregrine-semi.com>

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