PEREGRINE SEMICONDUCTOR

PRELIMINARY SPECIFICATION

PE4122-260

High Linearity MOSFET Quad Mixer For PCS & 3G BTS

Features

- Integrated, Single Ended RF & LO Interfaces
- High linearity: IIP3 >+ 30 dBm, 1.8 – 2.0 GHz (+17 dBm LO)
- Low-conversion loss: 7.6 dB (+17 dBm LO)
- High Isolation: Typical LO-IF at 38 dB / LO-RF at 34 dB
- Designed for Low-Side LO Injection

Product Description

The PE4122 is a high linearity, passive MOSFET Quad Mixer for PCS & 3G Base Station Receivers, exhibiting high dynamic range performance over an LO drive range of +14 dBm to +20 dBm. This mixer integrates passive matching networks to provide single-ended interfaces for the RF and LO ports, eliminating the need for external RF baluns or matching networks. The PE4122 is optimized for frequency down conversion using low-side LO injection for PCS & 3G Base Station applications.

The PE4122 is manufactured in Peregrine's patented Ultra-Thin Silicon (UTSi®) CMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Schematic Diagram

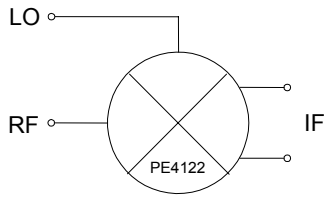


Figure 2. Package Drawings

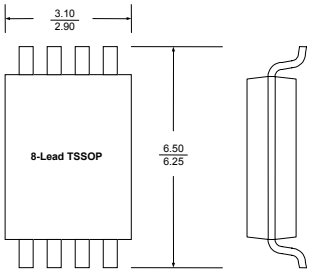


Table 1. Electrical Specifications @ +25 °C (Z_S = Z_L = 50 Ω)

Parameter	Minimum	Typical	Maximum	Units
Frequency Range:				
LO	1540	--	1740	MHz
RF	1800	--	2000	MHz
IF	--	260*	--	MHz
Conversion Loss		7.6	8.3	dB
Isolation:				
LO-RF	24	34		dB
LO-IF	26	38		dB
Input IP3				
1.8 GHz	27	30		dBm
1.9 GHz	30	33		dBm
2.0 GHZ	27	30		dBm
Input 1 dB Compression		20		dBm

**An IF frequency of 260 MHz is a nominal frequency. The IF frequency can be specified by the user as long as the RF and LO frequencies are within the specified maximum and minimum.*

Test conditions unless otherwise noted: LO input drive = 17 dBm, RF input drive = 0 dBm

Figure 3. Pin Configuration

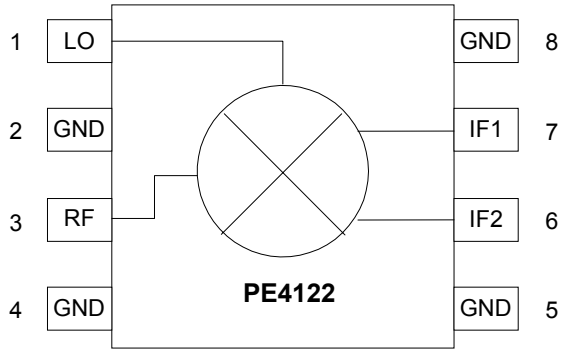


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	LO	LO Input
2	GND	Ground connection for Mixer. Traces should be physically short and connect immediately to ground plane for best performance.
3	RF	RF Input
4	GND	Ground.
5	GND	Ground.
6	IF1	IF differential output
7	IF2	IF differential output
8	GND	Ground.

Table 3. Absolute Maximum Ratings

Symbol	Parameter/Conditions	Min	Max	Units
T_{ST}	Storage temperature range	-65	150	°C
T_{OP}	Operating temperature range	-40	85	°C
P_{LO}	LO input power		20	dBm
P_{RF}	RF input power		20	dBm
VESD	ESD Sensitive Device		100	V

Electrostatic Discharge (ESD) Precautions

When handling this UTSi device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the rating specified in Table 3.

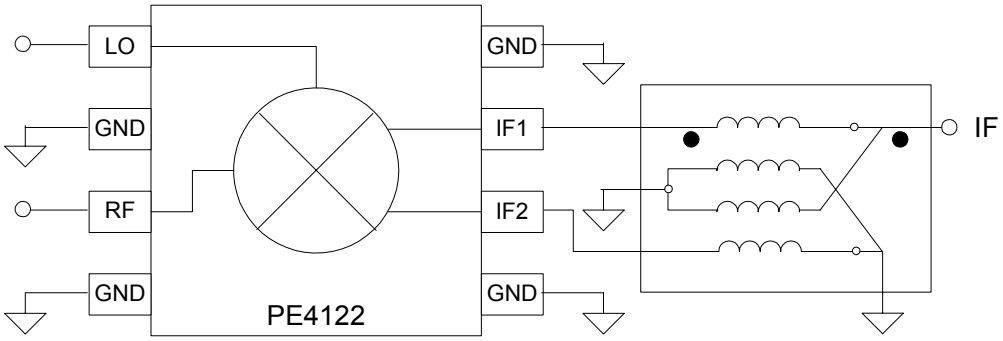
Latch-Up Avoidance

Unlike conventional CMOS devices, UTSi CMOS devices are immune to latch-up.

Evaluation Board

Figure 4 is the Schematic for the evaluation test board while Figure 5 shows the board layout. The PE4122 has on-chip passive matching networks for the RF and LO inputs, eliminating the need for additional passive components or RF baluns on the RF and LO inputs. The RF input is tuned for an input of 1.8 GHz to 2.0 GHz. The LO input is designed for low-side injection over a frequency range of 1.54 GHz to 1.74 GHz. Figure 6 shows the test circuit used for a 2-tone, third order intercept measurement.

Figure 4. Evaluation Board Schematic Diagram



T3 M/A-Com E-Series RF 4:1 Transformer 2.0 – 1000 MHz ETK4-2T

Figure 5. Evaluation Board Layout

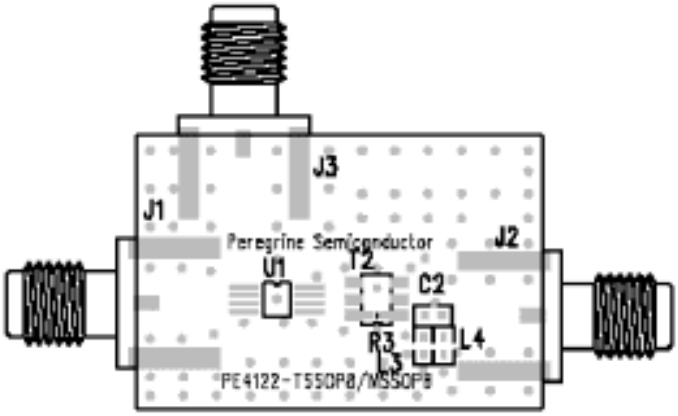
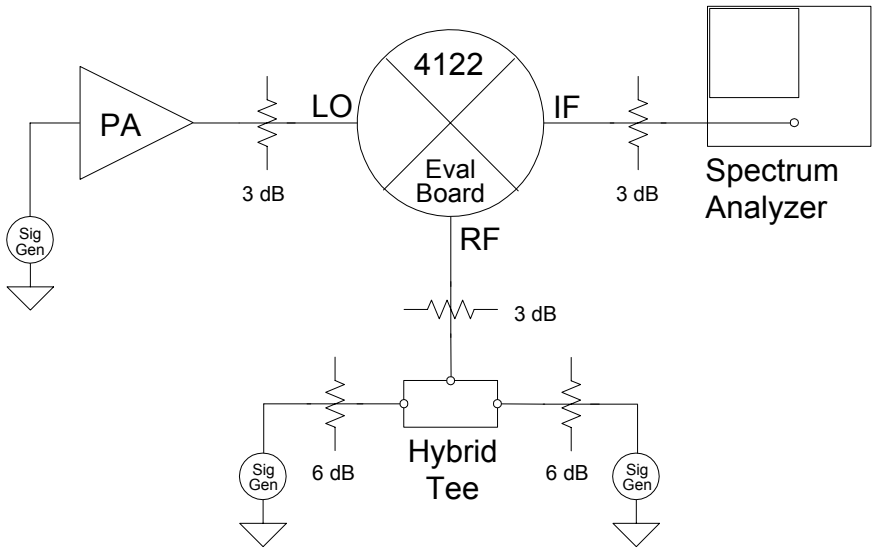


Table 4. Bill of Materials

Reference	Value / Description
T2	M/A Com ETK4-2T
C2	OΩ
R3	DNI
L3, L4	DNI
U1	PE4122 Mixer
J1, J2, J3	SMA Connector

Figure 6. Evaluation Board Testing Block Diagram, 2-Tone Setup



Typical Performance Data

Figure 7. 1dB Compression

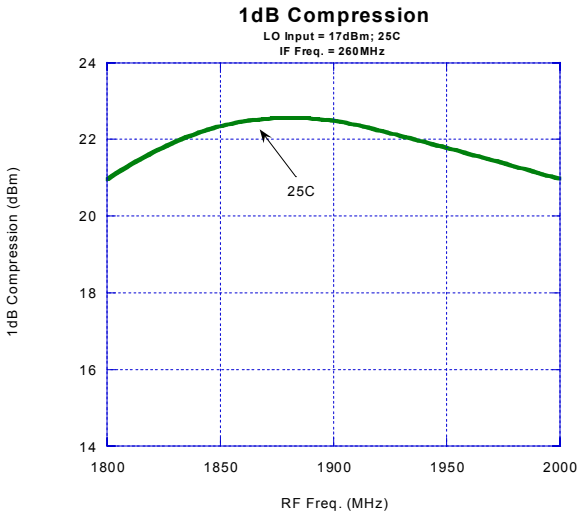


Figure 8. Conversion Loss vs. Temperature

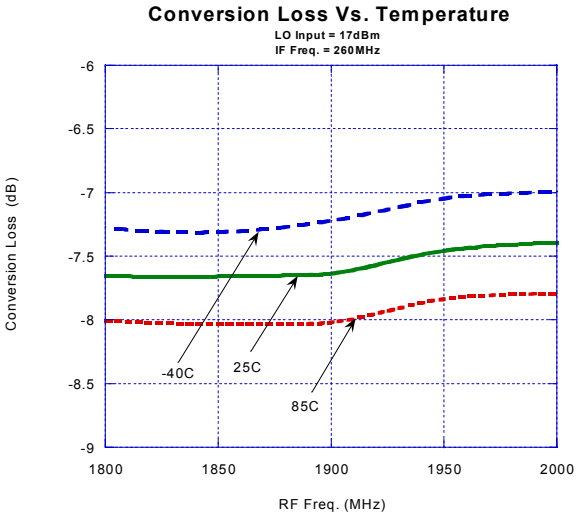


Figure 9. Input IP3 vs. Temperature

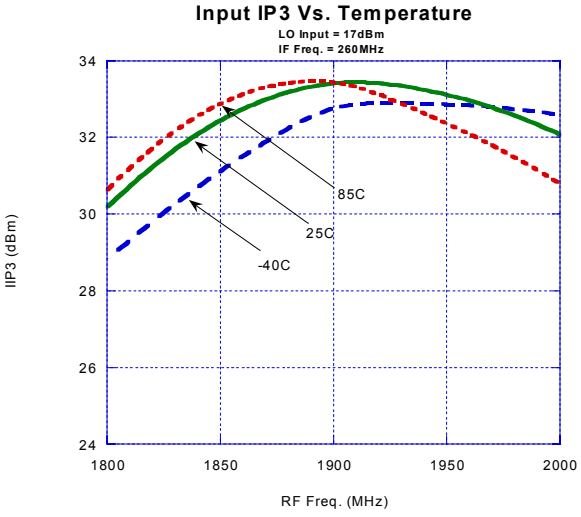
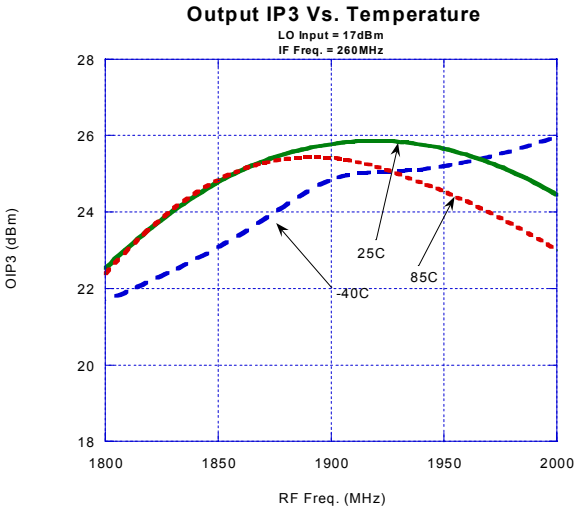


Figure 10. Output IP3 vs. Temperature



Typical Performance Data

Figure 11. LO-IF Isolation vs. Temperature

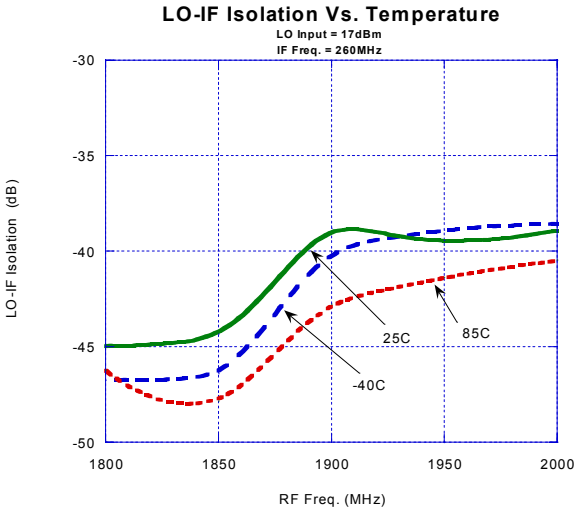


Figure 12. LO-RF Isolation vs. Temperature

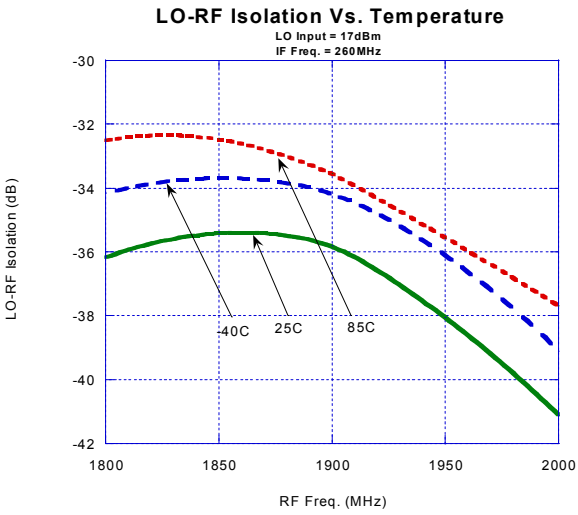


Figure 13. LO Port Return Loss

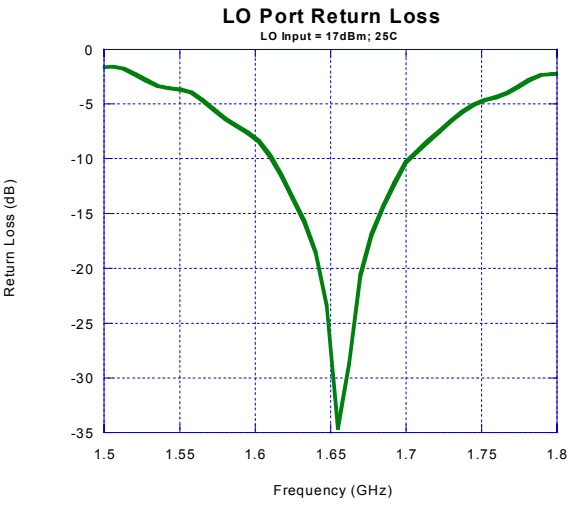
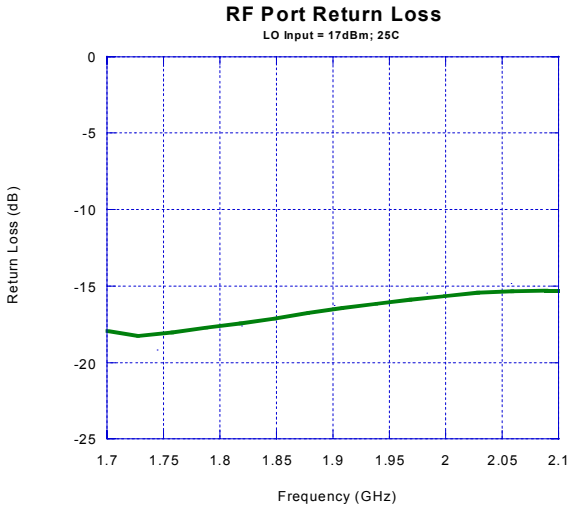


Figure 14. RF Port Return Loss



Typical Performance Data

Figure 15. Input IP3 Vs. LO Power

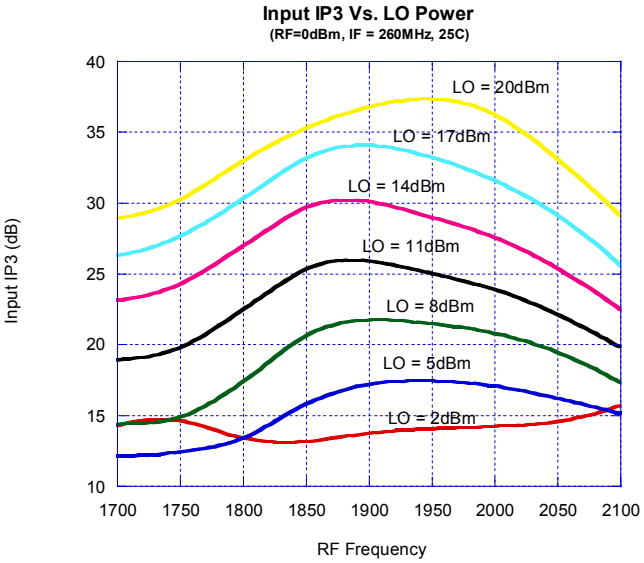


Figure 16. Conversion Loss Vs. LO Power

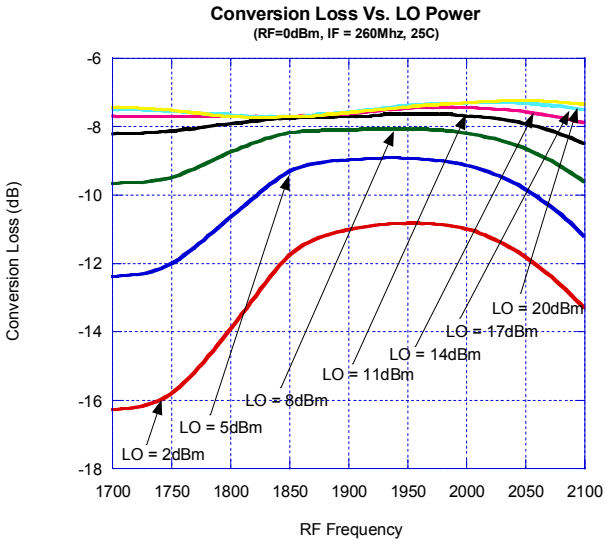


Table 5. Spurious Response

	$mF_{RF} + nF_{LO}$				
	nF_{LO}				
mF_{RF}	0	1	2	3	4
0	---	-33.09	-6.83	-11.49	-8.86
1	-27.64	-5.01	-39.91	-34.08	-58.33
2	-49.53	-50.27	-58.81	-70.85	-81.69
3	-82.93	-83.92	-88.39	-93.79	-86.81
4	>110	>110	>110	>110	>110

Normalized to dB below P_{IF}

(RF=1900 MHz @ 0 dBm, LO = 1640 MHz @ 17 dBm)

Table 6. Spurious Response

	$mF_{RF} - nF_{LO}$				
	nF_{LO}				
mF_{RF}	0	1	2	3	4
0	---	-33.09	-6.83	-11.49	-8.86
1	-27.64	0.00	-28.79	-18.38	-33.83
2	-49.53	-62.22	-53.59	-69.13	-65.66
3	-82.93	-75.81	-72.79	-73.00	-71.97
4	>110	>110	>110	-95.65	-93.44

Normalized to dB below P_{IF}

(RF=1900 MHz @ 0 dBm, LO = 1640 MHz @ 17 dBm)

Figure 17. Package Drawing

8-lead TSSOP

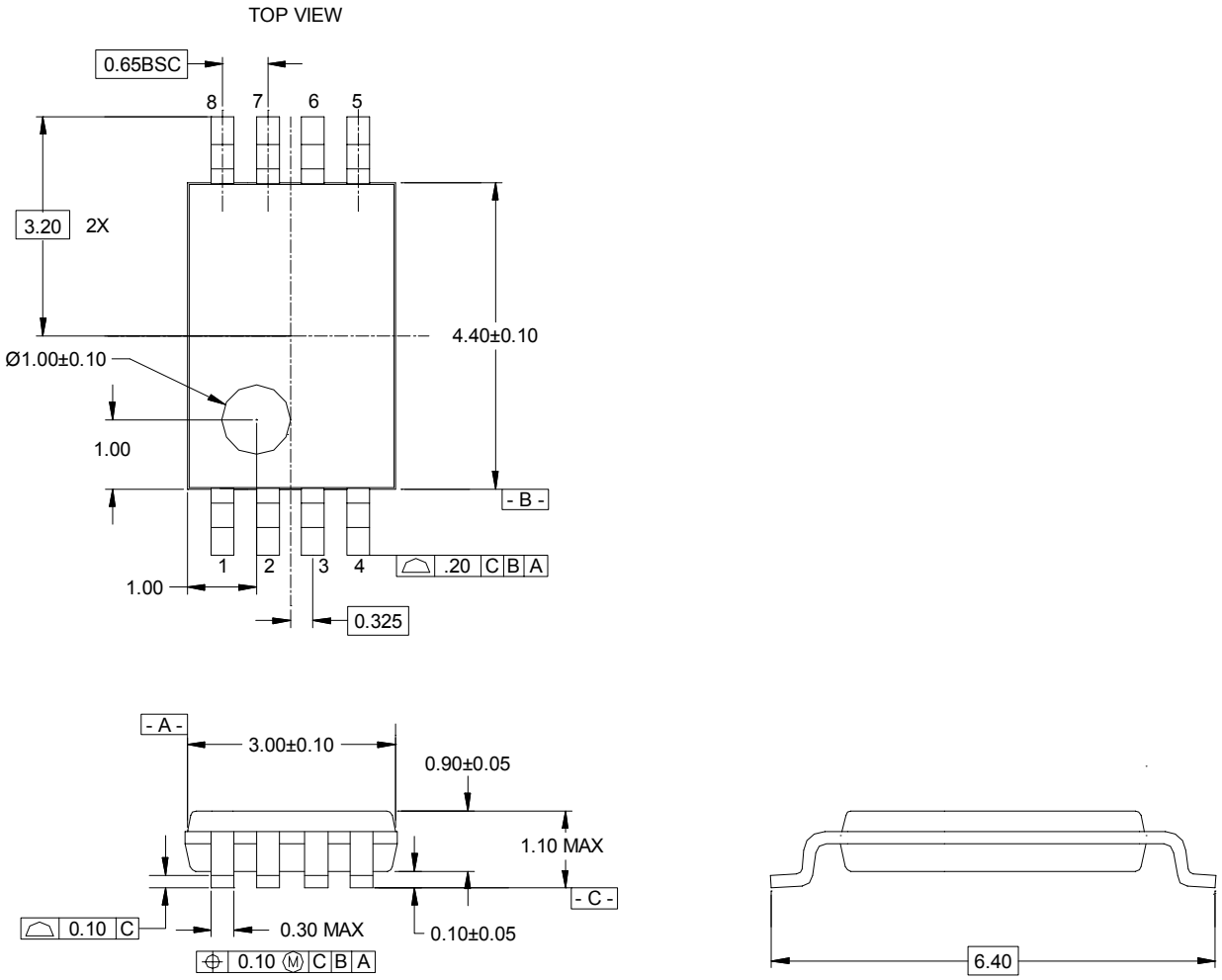


Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4122-21	4122	PE4122-260	8-lead TSSOP	100 pcs. / Tube
4122-22	4122	PE4122-260	8-lead TSSOP	2000 pcs. / T&R
4122-00	4122-EK		Evaluation Board	1 / Box

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Data Sheet Identification

Advance Information

The product is in a formative or design stage. The data sheet contains design target specifications for product development. Specifications and features may change in any manner without notice.

Preliminary Specification

The data sheet contains preliminary data. Additional data may be added at a later date. Peregrine reserves the right to change specifications at any time without notice in order to supply the best possible product.

Product Specification

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