

Precision Wide Bandwidth Analog Switches
Features

- Single-Supply Operation (+2V to +6V)
- Rail-to-Rail Analog Signal Dynamic Range
- Low On-Resistance (8Ω typ with 5V supply)
Minimizes Distortion and Error Voltages
- R_{ON} Matching Between Channels, 0.9 Ω typ
- On-Resistance Flatness, 3Ω typ
- Low Charge Injection Reduces Glitch Errors. $Q = 7pC$ typ
- High Speed. $t_{ON} = 8ns$ typ
- Very Good Off-Isolation: -55dB @ 10 MHz
- Wide -3dB Bandwidth: 230 MHz
- High-Current Channel Capability: >100mA
- TTL/CMOS Logic Compatible
- Low Power Consumption (0.5μW typ)
- Pin-compatible with DG40X, MAX38X

Applications

- Audio, Video Switching and Routing
- Battery-Powered Communication Systems
- Computer Peripherals
- Telecommunications
- Portable Instrumentation
- Replaces Mechanical Relays

Description

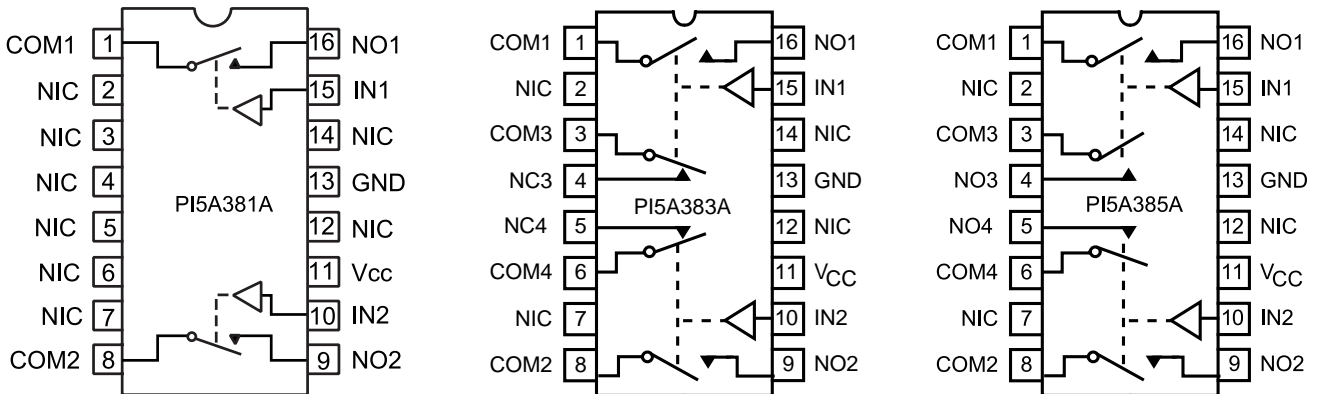
The PI5A381/383/385A are dual monolithic analog switches designed for single-supply operation. These high-precision devices are ideal for low-distortion audio, video signal switching and routing.

The PI5A381 is a dual single-pole single-throw (SPST), normally open (NO) switch. The PI5A383 is a dual single-pole double-throw (SPDT) switch. The PI5A385 is a dual double-pole single-throw (DPST), normally open (NO) function.

Each switch conducts current equally well in either direction when on. When off they block voltages up to the power-supply rails.

The PI5A381/383/385 are fully specified with +5V, and +3.3V supplies. With +5V, they guarantee 10Ω on-resistance. On-resistance matching between channels is within 2Ω. On-resistance flatness is less than 4Ω over the specified range. The PI5A38X family guarantees fast switching speeds ($t_{ON} < 15ns</math>).$

These products are available in the 16-pin narrow-body SOIC, QSOP, and PDIP packages for operation over the industrial (-40°C to +85 °C) temperature range.

Functional Diagram, Pin Configurations and Truth Tables


Switches shown for Logic "0" input
NC = Normally Closed, NO = Normally Open, NIC = Not internally Connected

PI5A381A	
Logic	Switch
0	OFF
1	ON

PI5A383A		
Logic	SW1, SW2	SW3, SW4
0	OFF	ON
1	ON	OFF

PI5A385A	
Logic	Switch
0	OFF
1	ON



Absolute Maximum Ratings

Voltages Referenced to GND

V_{CC} -0.5V to +7V

$V_{IN}, V_{COM}, V_{NC}, V_{NO}$ (Note 1) -0.5V to $V_{CC}+2V$
or 30mA, whichever occurs first

Current (any terminal except COM, NO, NC) 30mA

Current, COM, NO, NC 100 mA

(pulsed at 1ms, 10% duty cycle) 120mA

Thermal Information

Continuous Power Dissipation

PDIP (derate 10.5mW/°C above 70°C) 800mW

Narrow SO & QSOP

(derate 8.7mW/°C above +70°C) 650mW

Storage Temperature -65°C to +150°C

Lead Temperature(soldering, 10s) +300°C

Note 1 : Signals on NC, NO, COM, or IN exceeding V_{CC} or GND are clamped by internal diodes. Limit forward diode current to 30mA.

Caution: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied.

Electrical Characteristics-Single 5.0V Supply

($V_{CC} = 5V \pm 10\%$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$)

Parameter	Symbol	Test Conditions	Temp(°C)	Min. ⁽²⁾	Typ. ⁽²⁾	Max. ⁽²⁾	Unit
Analog Switch							
Analog Signal Range ⁽³⁾	V_{ANALOG}		Full	0		V_{CC}	V
ON-Resistance	R_{ON}	$V_{CC} = 4.5V, I_{COM} = -30mA$ V_{NO} or $V_{NC} = +2.5V$	25		8	10	Ω
On-Resistance Match Between Channels ⁽⁴⁾	ΔR_{ON}		Full			12	
On-Resistance Flatness ⁽⁵⁾	$R_{FLAT(ON)}$	$V_{CC} = 5V, I_{COM} = -30mA$ V_{NO} or $V_{NC} = 1V, 2.5V, 4V$	25		0.9	2	
			Full			4	
NO or NC Off Leakage Current ⁽⁶⁾	$I_{NO(OFF)}$ $I_{NC(OFF)}$	$V_{CC} = 5.5V, V_{COM} = 0V$ V_{NO} or $V_{NC} = 4.5V$	25		0.05		nA
			Full	-80		80	
COM Off Leakage Current ⁽⁶⁾	$I_{COM(OFF)}$	$V_{+} = 5.5V, V_{COM} = +4.5V$ V_{NO} or $V_{NC} = \pm 0V$	25		0.05		
			Full	-80		80	
COM On Leakage Current ⁽⁶⁾	$I_{COM(ON)}$	$V_{CC} = 5.5V, V_{COM} = +4.5V$ V_{NO} or $V_{NC} = +4.5V$	25		0.07		
			Full	-80		80	

Electrical Characteristics-Single 5.0V Supply (continued)

(V_{CC} = 5V ±10%, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V)

Parameter	Symbol	Conditions	Temp(°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Unit
Logic Input							
Input High Voltage	V _{INH}	Guaranteed logic High Level	Full	2			V
Input Low Voltage	V _{INL}	Guaranteed logic Low Level				0.8	
Input Current with Input Voltage High	I _{INH}	V _{IN} = 2.4V, all others = 0.8V		-1	0.005	1	μA
Input Current with Input Voltage Low	I _{INL}	V _{IN} = 0.8V, all others = 2.4V		-1	0.005	1	
Dynamic							
Turn-On Time	t _{ON}	V _{CC} = 5V, Figure 1	25		8	15	ns
			Full			20	
Turn-Off Time	t _{OFF}		25		3.5	7	
			Full			10	
Charge Injection ⁽³⁾	Q	C _L = 1nF, V _{GEN} = 0V, R _{GEN} = 0Ω Figure 2	25		7	10	pC
Off Isolation	OIRR	R _L = 50Ω, C _L = 5pF, f = 10MHz, Figure 3			-55		dB
Crosstalk ⁽⁸⁾	I _{COM(OFF)}	R _L = 50Ω, C _L = 5pF, f = 10MHz, Figure 4			-92		
NC or NO Capacitance	C _(OFF)	f = 1kHz, Figure 5			8		pF
COM Off Capacitance	C _{COM(OFF)}				8		
COM On Capacitance	C _{COM(ON)}	f = 1kHz, Figure 6			14		
-3dB Bandwidth	BW	R _L = 50Ω, Figure 7		Full		230	
Distortion ⁽⁹⁾	D	R _L = 10kΩ			0.03		%
Supply							
Power-Supply Range	V _{CC}		Full	2		6	V
Positive Supply Current	I _{CC}	V _{CC} = 5.5V, V _{IN} = 0V or V _{CC} , all channels on or off				1	μA

Notes:

1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design.
4. ΔR_{ON} = R_{ON} max - R_{ON} min.
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.
6. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at +25°C.
7. Off Isolation = 20log₁₀ [V_{COM} / (V_{NO} or V_{NC})]. See figure 3.
8. Between any two switches. See figure 4.
9. D = R_{FLAT(ON)}/R_L.

Electrical Specifications - Single +3.3V Supply

($V_{CC} = +3.3V \pm 10\%$, $GND = 0V$, $V_{INH} = 2.4V$, $V_{INL} = 0.8V$)

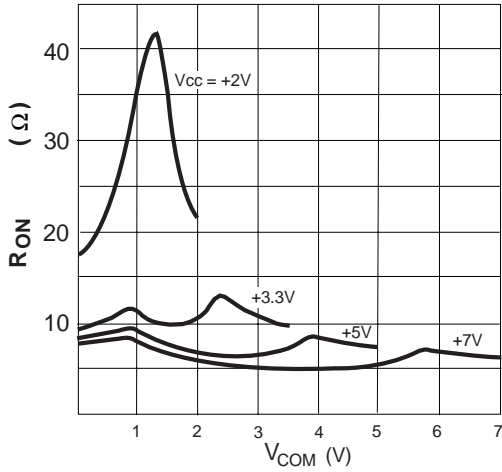
Parameter	Symbol	Conditions	Temp (°C)	Min ⁽¹⁾	Typ ⁽²⁾	Max ⁽¹⁾	Units
Analog Switch							
Analog Signal Range ⁽³⁾	V_{ANALOG}		Full	0		V_{CC}	V
On-Resistance	R_{ON}	$V_{CC} = 3V$, $I_{COM} = -30mA$, V_{NO} or $V_{NC} = 1.5V$	25		12	18	Ω
			Full			22	
On-Resistance Match Between Channels ⁽⁴⁾	ΔR_{ON}	$V_{CC} = 3.3V$, $I_{COM} = -30mA$, V_{NO} or $V_{NC} = 0.8V, 2.5V$	25		1	2	
			Full			4	
On-Resistance Flatness ^(3,5)	$R_{FLAT(ON)}$		25		4	10	
			Full			12	
Dynamic							
Turn-On Time	t_{ON}	$V_{CC} = 3.3V$, V_{NO} or $V_{NC} = 1.5V$ Figure 1	25		14	25	ns
			Full			40	
Turn-Off Time	t_{OFF}		25		5	12	
			Full			20	
Charge Injection ⁽³⁾	Q	$C_L = 1nF$, $V_{GEN} = 0V$, $R_{GEN} = 0V$, Figure 2	25		5	10	pC
Supply							
Positive Supply Current	I_{CC}	$V_{CC} = 3.6V$, $V_{IN} = 0V$ or V_{CC} , all channels on or off	Full			1	μA

Notes:

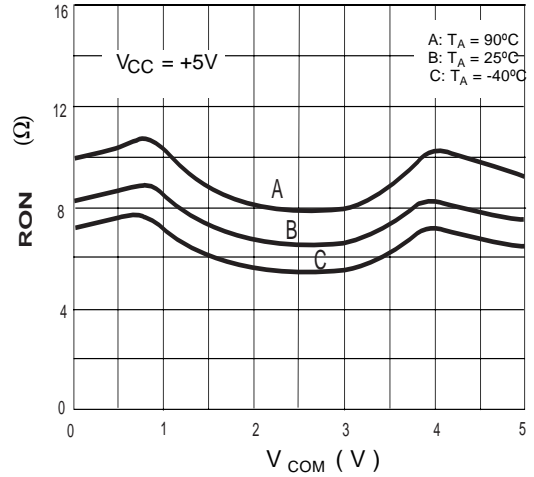
1. The algebraic convention, where the most negative value is a minimum and the most positive is a maximum, is used in this data sheet.
2. Typical values are for DESIGN AID ONLY, not guaranteed or subject to production testing.
3. Guaranteed by design
4. $\Delta R_{ON} = R_{ON \text{ max}} - R_{ON \text{ min}}$
5. Flatness is defined as the difference between the maximum and minimum value of on-resistance measured.

Typical Operating Characteristics ($T_A=+25^\circ\text{C}$, unless otherwise noted)

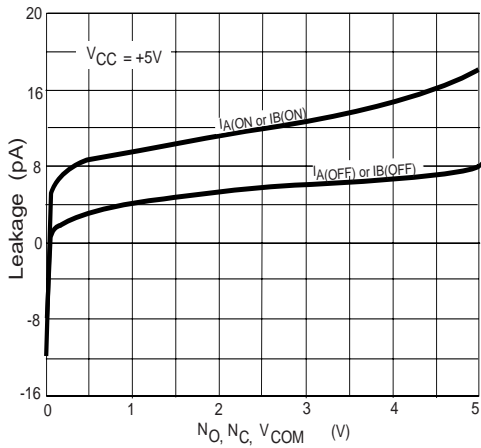
R_{ON} vs. V_{COM}



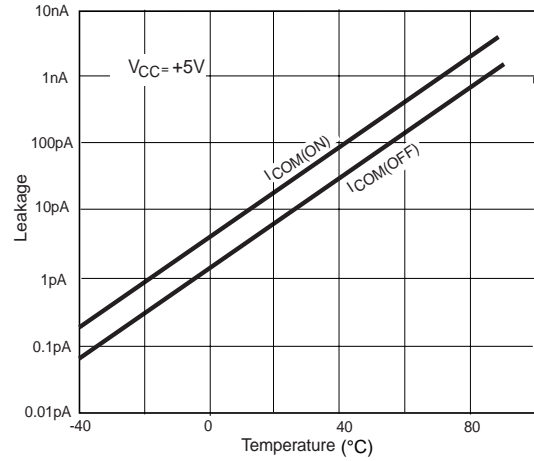
R_{ON} vs. V_{COM} and Temperature



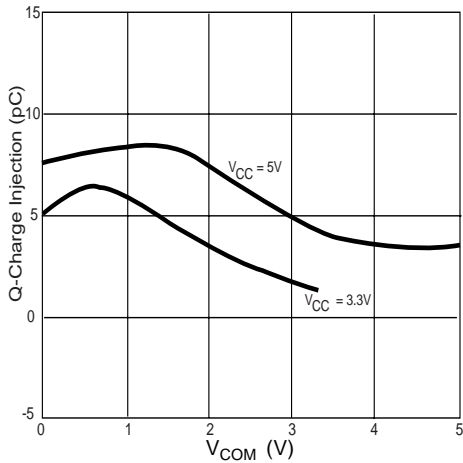
Leakage Currents vs. Analog Voltage



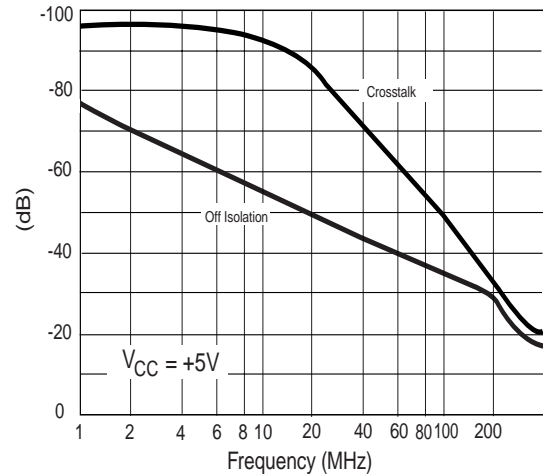
Leakage Current vs. Temperature



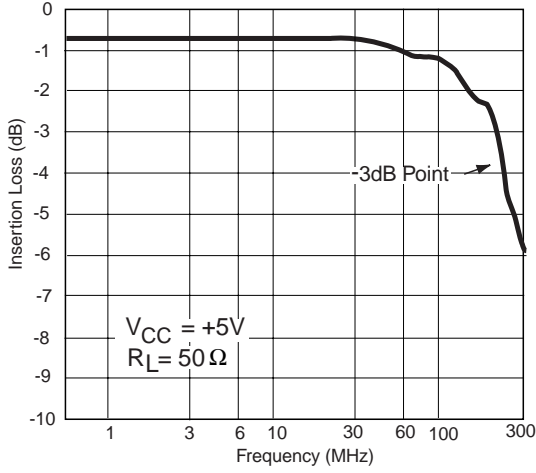
Charge Injection vs. Analog Voltage



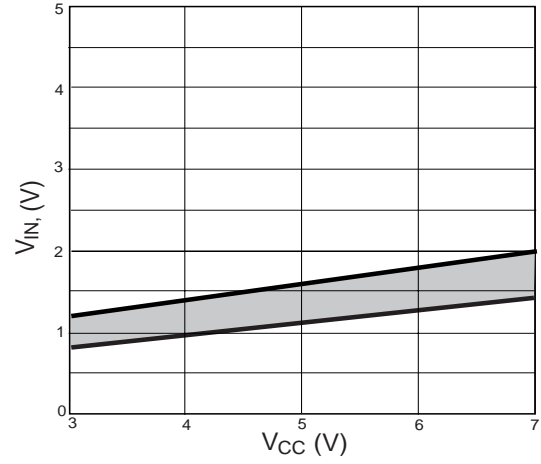
Crosstalk and Off-Isolation vs. Frequency



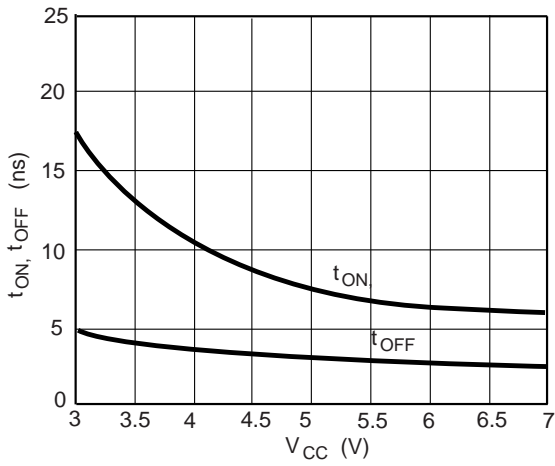
Insertion Loss vs. Frequency



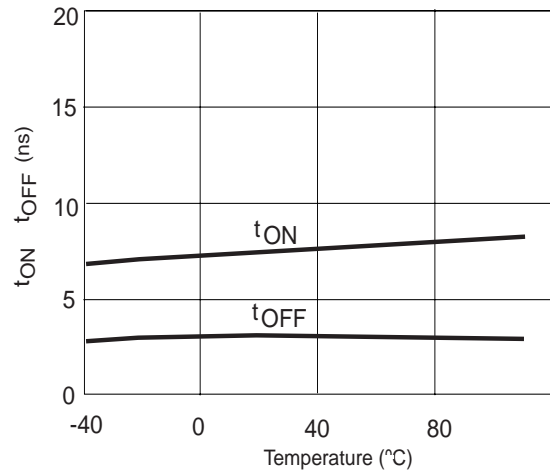
Input Switching Threshold vs. Supply Voltage



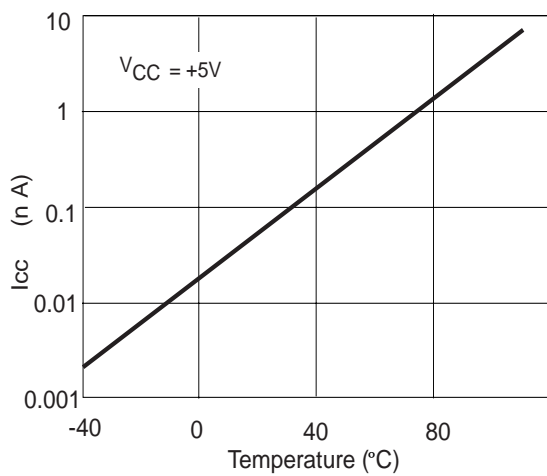
R_{ON} vs. V_{COM} and Single Supply



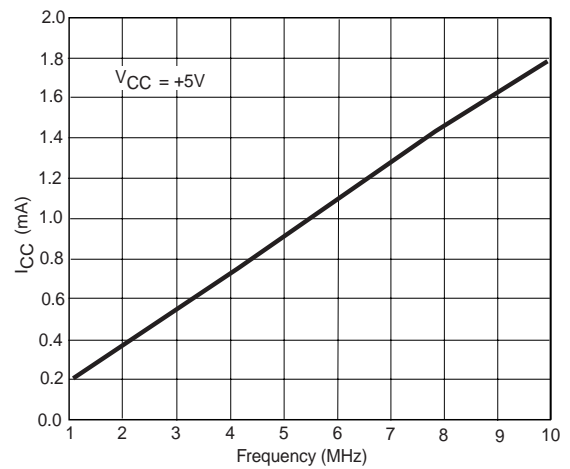
Switching Times vs. Temperature



Supply Current vs. Temperature



Supply Current vs. Input Switching Frequency



Test Circuits/Timing Diagrams

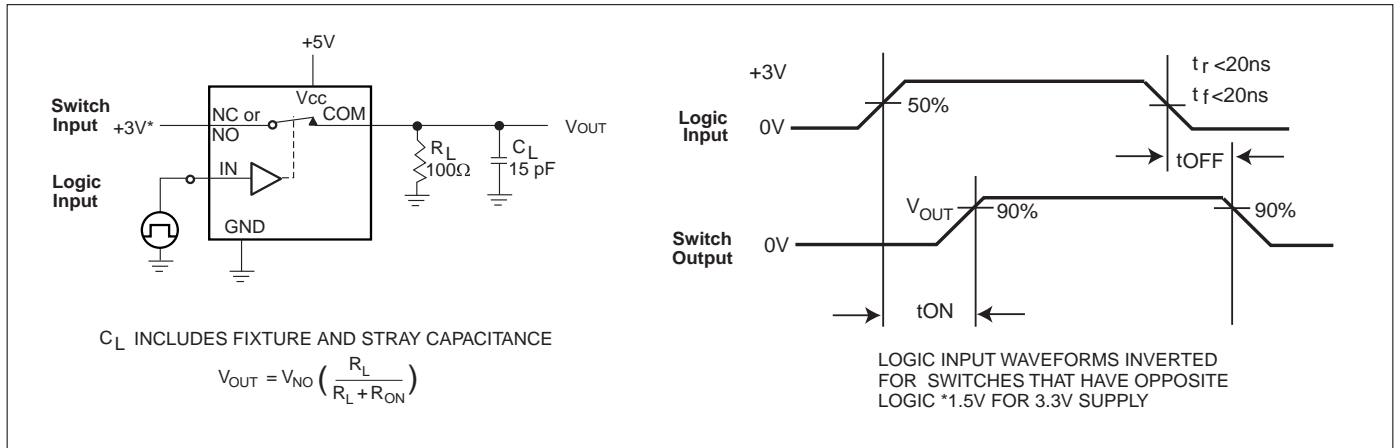


Figure 1. Switching Time

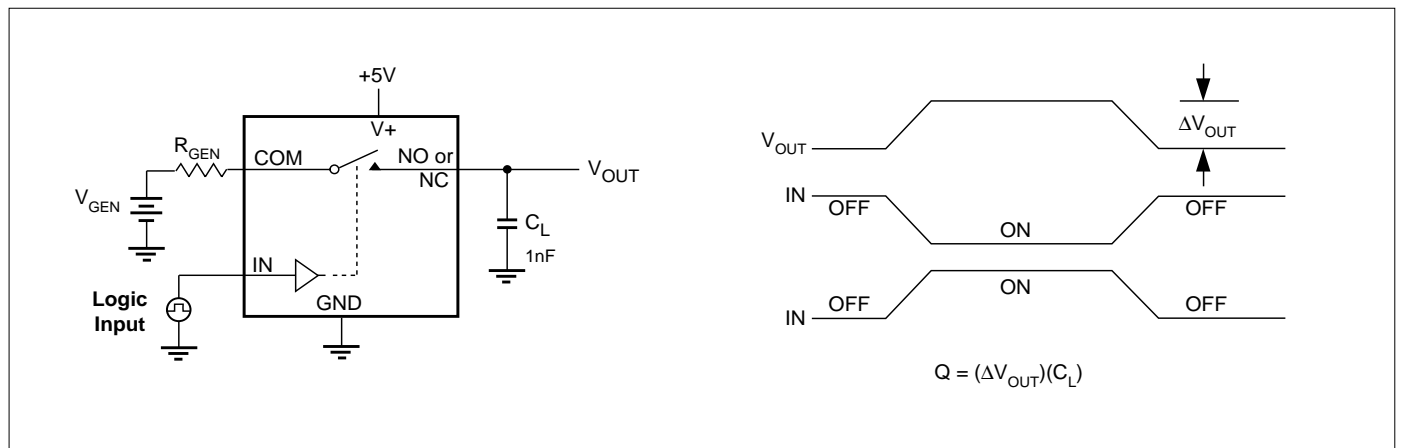


Figure 2. Charge Injection

Test Circuits/Timing Diagrams (continued)

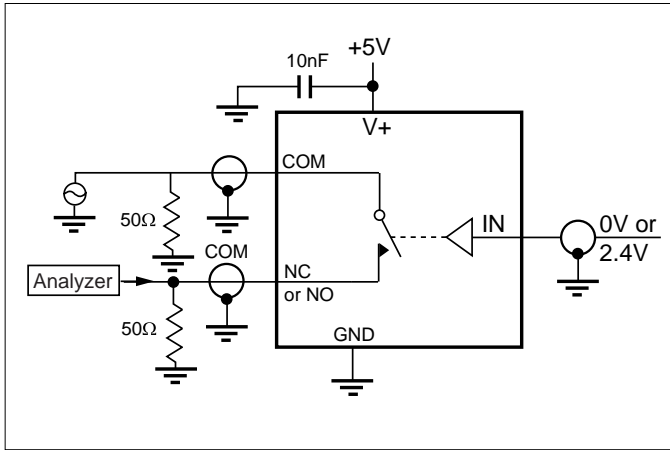


Figure 3. Off Isolation

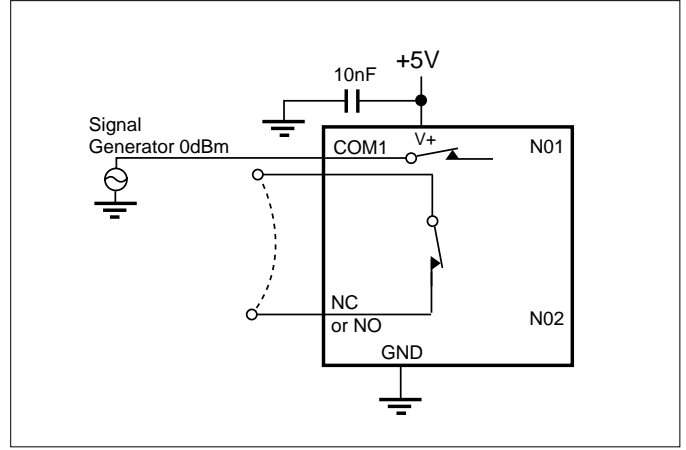


Figure 4. Crosstalk

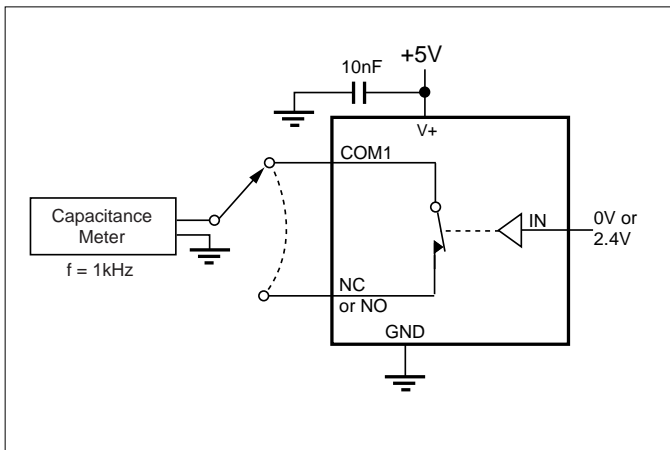


Figure 5. Channel-Off Capacitance

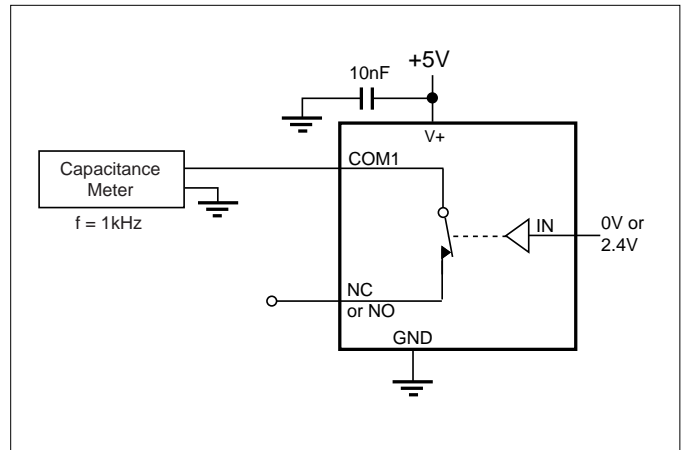


Figure 6. Channel-On Capacitance

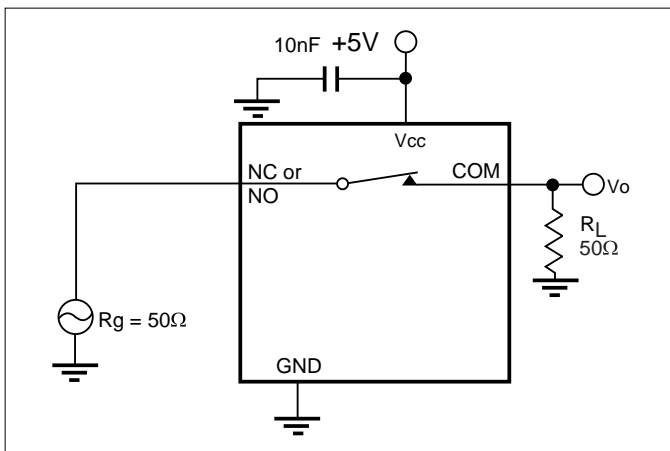


Figure 7. Bandwidth

Ordering Information

Part Number	Package
PI5A381AP	16-Pin PDIP
PI5A381AW	Narrow Body SOIC-16
PI5A381AQ	16-Pin QSOP
PI5A383AP	16-Pin PDIP
PI5A383AW	Narrow Body SOIC-16
PI5A383AQ	16-Pin QSOP
PI5A385AP	16-Pin PDIP
PI5A385AW	Narrow Body SOIC-16
PI5A385AQ	16-Pin QSOP