



# PI5C16215C

## 20-Bit, Hot Insertion, BusSwitch with Precharged Outputs & Undershoot Protection

### Product Features

- Undershoot protection up to  $-1.5V$ , 25ns width
- Near zero propagation delay
- 5 Ohm switches connect between two ports
- Fast switching speed: 4.5ns max.
- Permits hot insertion
- Isolation during power-off conditions
- B-Port outputs are precharged by bias voltage to minimize signal distortion during live insertion.
- Package options include:
  - 48-pin 150-mil wide plastic BQSOP (B)
  - 48-pin 240-mil wide plastic TSSOP (A)

### Product Description

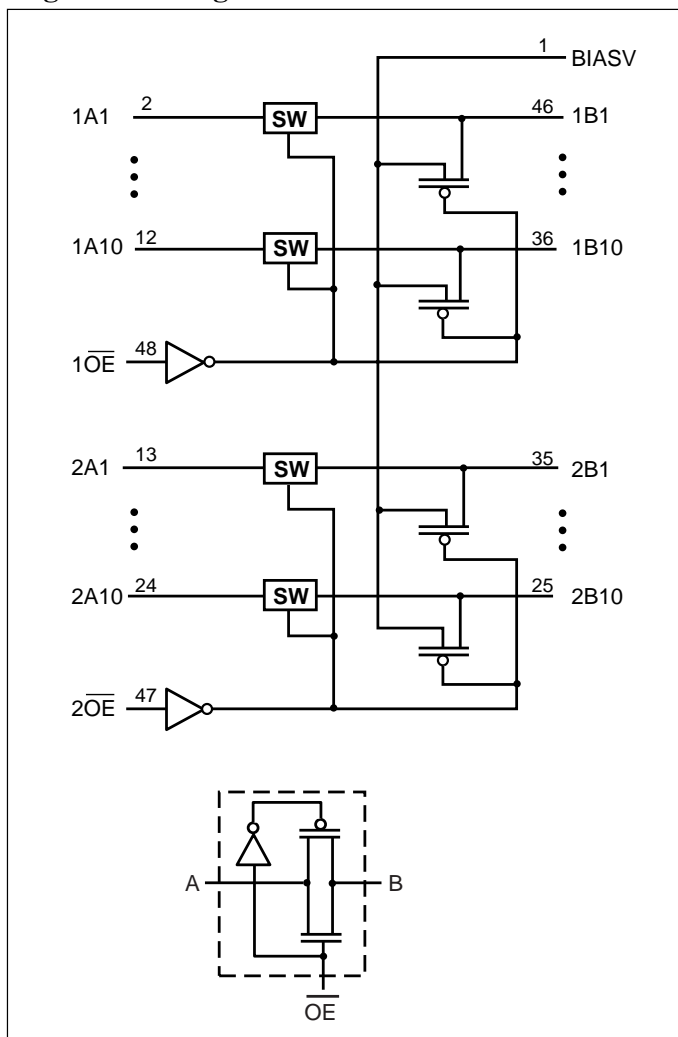
Pericom Semiconductor's PI5C series of logic circuits are produced using the company's advanced submicron CMOS technology.

The PI5C16215C provides 20-bits of high-speed bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay. The device also precharges the B-port to a user-selectable bias voltage (BIASV) to minimize live-insertion noise. The device incorporates an internal charge pump to handle input undershoot of up to  $-1.5V$  and 25ns width.

The device is organized as dual 10-bit bus switches with individual output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the corresponding 10-bit bus switch is on and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, a high-impedance state exists between the two ports, and port B is precharged to BIASV through the equivalent of a 10-k $\Omega$  resistor.

To ensure the high-impedance state on power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver connected to  $\overline{OE}$ .

### Logic Block Diagram



### Product Pin Configuration

BIASV	1	48	$1\overline{OE}$
1A1	2	47	2 $\overline{OE}$
1A2	3	46	1B1
1A3	4	45	1B2
1A4	5	44	1B3
1A5	6	43	1B4
1A6	7	42	1B5
GND	8	41	GND
1A7	9	40	1B6
1A8	10	39	1B7
1A9	11	38	1B8
1A10	12	37	1B9
2A1	13	36	1B10
2A2	14	35	2B1
$V_{CC}$	15	34	2B2
2A3	16	33	2B3
GND	17	32	GND
2A4	18	31	2B4
2A5	19	30	2B5
2A6	20	29	2B6
2A7	21	28	2B7
2A8	22	27	2B8
2A9	23	26	2B9
2A10	24	25	2B10



**Absolute Maximum Ratings Over Free-Air Temperature Range**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Supply Voltage Range .....	-0.5V to +7V
DC Input Voltage <sup>(1)</sup> .....	-0.5V to +7V
Input Clamp Current, I <sub>IK</sub> (V <sub>I</sub> < 0) .....	-50mA
DC Output Current .....	120mA
Power Dissipation <sup>(2)</sup> .....	0.5W

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Notes:**

1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

**Recommended Operating Conditions (Over Recommended Operating Free-air Temperature Range)**

Parameter	Description	Min.	Max.	Units
V <sub>CC</sub>	Supply voltage	4	5.5	V
BIASV	Supply voltage	1.3	V <sub>CC</sub>	
V <sub>IH</sub>	High-Level input voltage	2		
V <sub>IL</sub>	Low-level input voltage		0.8	
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

**Electrical Characteristics (Over Recommended Operating Free-air Temperature Range)**

Parameter	Test Conditions		Min.	Typ <sup>†</sup>	Max.	Units
V <sub>IK</sub>	V <sub>CC</sub> = 4.5V	I <sub>I</sub> = -18mA			-1.8	V
I <sub>I</sub>	V <sub>CC</sub> = 5.5V	V <sub>I</sub> = 5.5V or GND			±5	μA
I <sub>O</sub>	V <sub>CC</sub> = 4.5V	BIASV = 2.4V    V <sub>O</sub> = 0	0.25			mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5V	I <sub>O</sub> = 0            V <sub>I</sub> = V <sub>CC</sub> or GND			100	μA
ΔI <sub>CC</sub> <sup>‡</sup> Control pins	V <sub>CC</sub> = 5.5V	One input at 3.4V, Other at V <sub>CC</sub> or GND			2.5	mA
C <sub>I</sub> Control pins	V <sub>I</sub> = 3V or 0			3.5		pF
C <sub>O</sub> (OFF)	V <sub>O</sub> = 3V or 0            Switch Off			4.5		
r <sub>ON</sub> <sup>*</sup>	V <sub>CC</sub> = 4V	V <sub>I</sub> = 2.4V            I <sub>I</sub> = 15mA		9	20	Ω
	V <sub>CC</sub> = 4.5V	V <sub>I</sub> = 0,                I <sub>I</sub> = 64mA		5.5	8	
		V <sub>I</sub> = 0,                I <sub>I</sub> = 30mA		5	8	
		V <sub>I</sub> = 2.4V            I <sub>I</sub> = 15mA		9	15	

**Notes:**

- \* Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.
- ‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather the V<sub>CC</sub> or GND.
- † All typical values are at V<sub>CC</sub> = 5V, T<sub>A</sub> = 25°C.

**Truth Table**

$\overline{OE}$	Function
L	A port = B port
H	A port = Z, B Port = BIASV

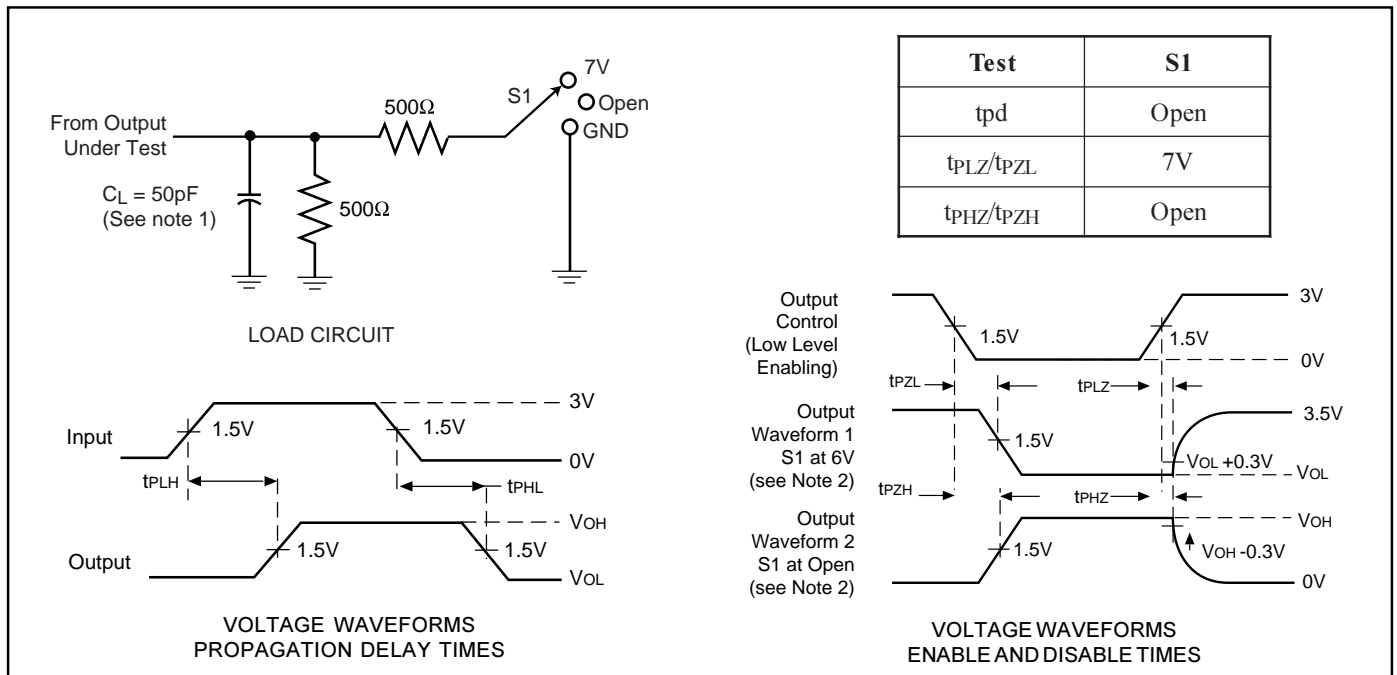
**Switching Characteristics** (Over Recommended Operating Free-air Temperature Range,  $C_L = 50\text{pF}$ )

Parameter	Test Conditions	From (Input)	To (Output)	$V_{CC} = 5V \pm 0.5V$		$V_{CC} = 4V$		Units
				Min.	Max.	Min.	Max.	
$t_{pD}$		A or B	B or A		0.25		0.25	ns
$t_{pZH}$	BIASV = GND	ON	A or B	3.1	5		6	
$t_{pZL}$	BIASV = 3V			3.0	5		6	
$t_{pHZ}$	BIASV = GND	ON	A or B	2.0	5		5.5	
$t_{pLZ}$	BIASV = 3V			3	5		5.5	

**Notes:**

1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50pF, when driven by an ideal voltage source (zero output impedance).

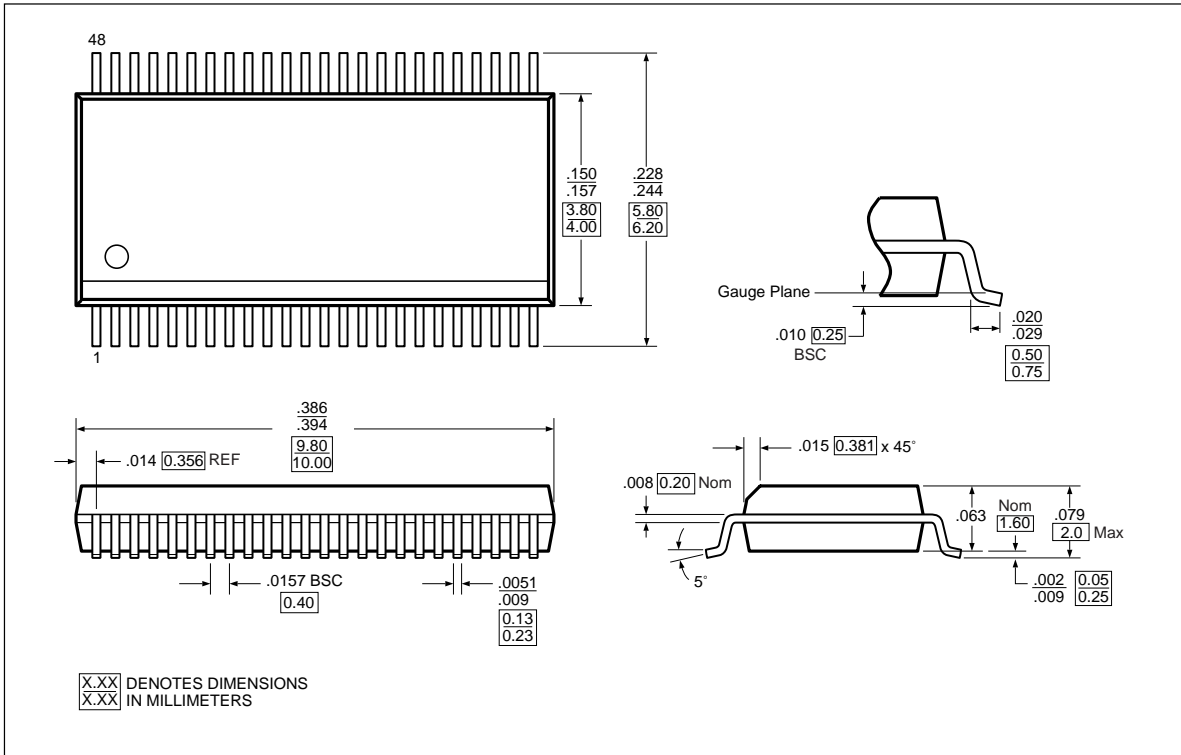
**Parameter Measurements**



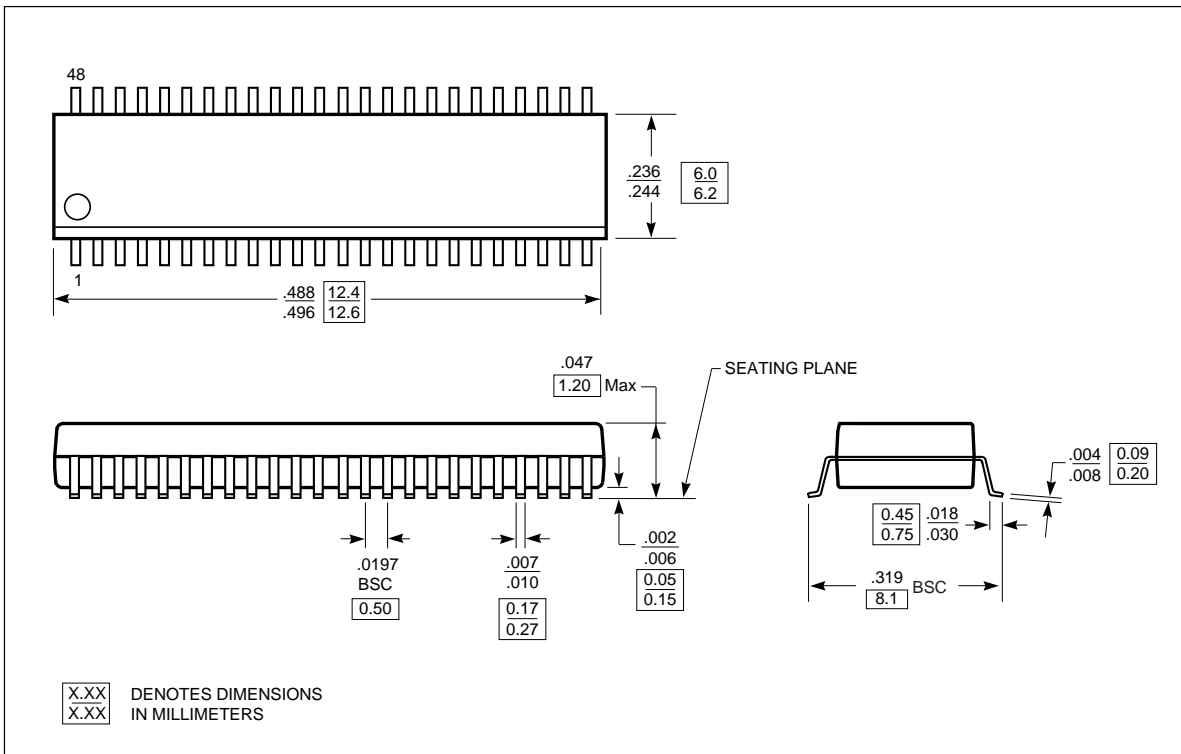
**Notes:**

1.  $C_L$  includes probe and jig capacitance.
2. Waveform 1 is for an output with internal conditions such that the output is LOW except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is HIGH except when disabled by the output control.
3. All input pulses are supplied by generators having the following characteristics:  $PRR < 10\text{MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r \leq 2.5\text{ns}$ ,  $t_f \leq 2.5\text{ns}$ .
4. The outputs are measured one at a time with one transition per measurement.
5.  $t_{pLZ}$  and  $t_{pHZ}$  are the same as  $t_{dis}$ .
6.  $t_{pZL}$  and  $t_{pZH}$  are the same as  $t_{en}$ .
7.  $t_{pLH}$  and  $t_{pHL}$  are the same as  $t_{pd}$ .

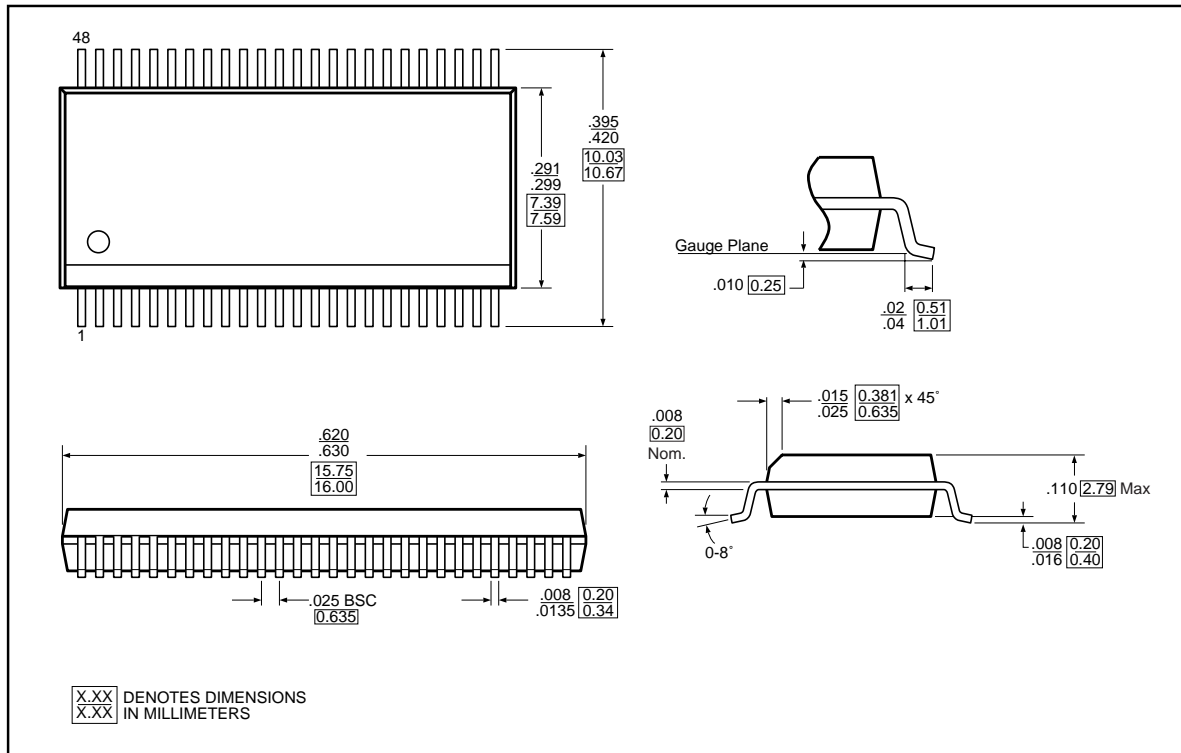
**48-pin BQSOP (B)**



**48-pin TSSOP (A)**



**48-pin SSOP (V)**



**Ordering Information**

Part	Pin - Package	Width
PI5C16215CA	48 - BQSOP (B48)	150 mil
PI5C16215CB	48 - TSSOP (A48)	240 mil

**Applications Information**

**Logic Inputs**

The logic control inputs can be driven up to +5.5V regardless of the supply voltage. For example, given a +5.0V supply, IN may be driven low to 0V and high to 5.5V. Driving IN Rail-to-Rail® minimizes power consumption.

**Power-Supply Sequencing**

Proper power-supply sequencing is recommended for all CMOS devices. Always apply V<sub>CC</sub> before applying signals to the bias voltage pin and the input/output or control pins.

*Rail-to-Rail is a registered trademark of Nippon Motorola, Ltd*