PI6C110E

Clock Solution for 133 MHz Celeron/Pentium II/III Processors

Features

- 3 of 2.5V 66/100/133 MHz CPU (CPU[0-2])
- 2 of 2.5V 33 MHz APIC (APIC[0-1])
- 9 of 3.3V 100/133 MHz SDRAM (SDRAM[0-7], DCLK)
- 8 of 3.3V 33 MHz PCI (PCI[0-7])
- 2 of 3.3V 66 MHz (3V66 [0-1])
- 2 of 3.3V 48 MHz (48MHz [0-1])
- 1 of 3.3V 14.3 MHz (REF)
- Selectable CPU and SDRAM clocks (on power up only)
- Power down function using PWR_DWN#
- Spread Spectrum Enable/Disable by I^2C
- I^2C interface to turn off unused clocks
- 56 pin SSOP package (V)

Description

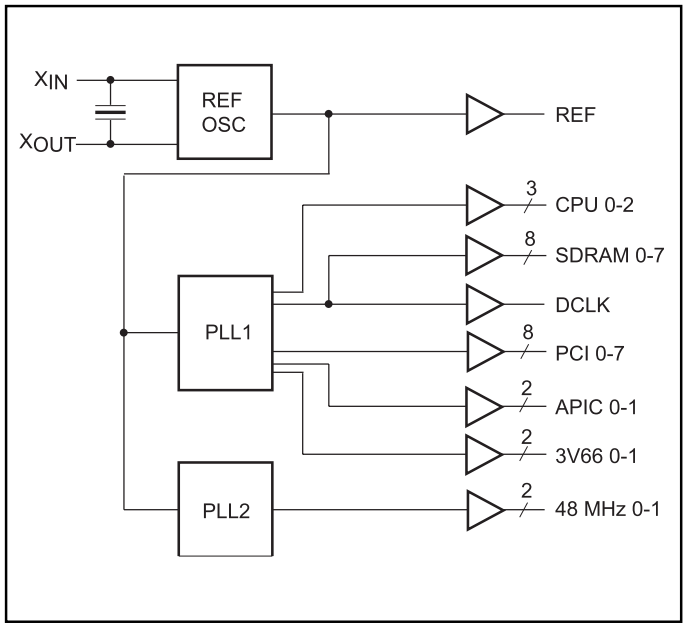
Pericom PI6C110E integrates a dual PLL clock generator, SDRAM buffer and I^2C interface. The clock generator section comprised of an oscillator, 2 low jitter phased locked loop, skew control, and power down logic. The SDRAM buffers are high speed and low skew to handle data transfers in excess of 133 MHz.

When Spread Spectrum mode is enabled, all clock outputs are modulated except for REF and 48 MHz[0-1] outputs. These clocks are down spread linearly (triangular modulation) by +0%, –0.6%.

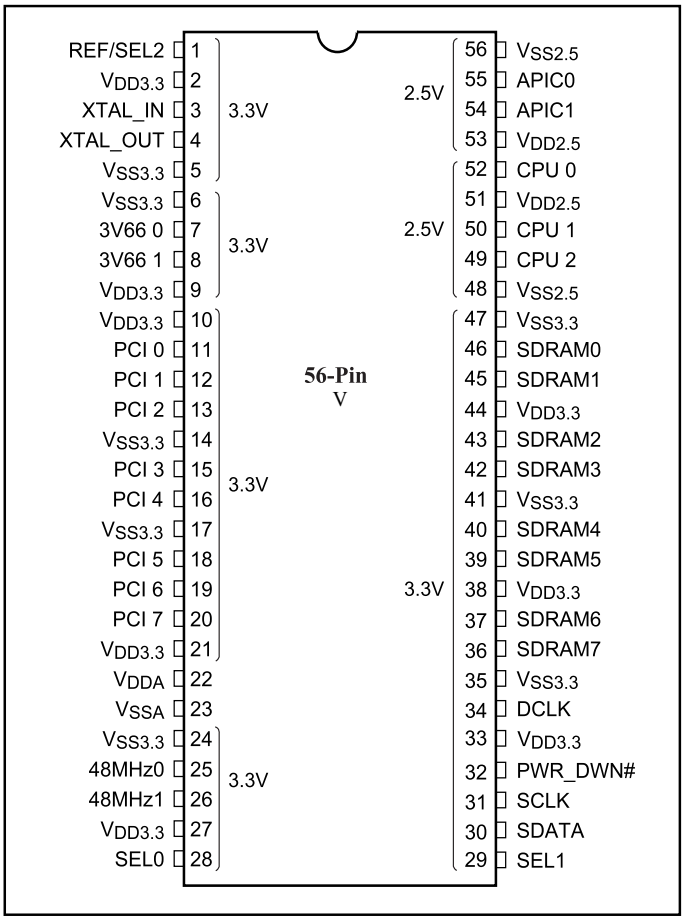
To minimize power consumption and EMI radiation some unused outputs can be turned off. Two wire I^2C interface is used to enable/disable Spread Spectrum mode, and to turned off PCI clocks, CPU clocks, and 48 MHz clocks.

For low power sleep mode, the entire device can be placed to power down mode. Driving the PWR_DWN# to low state disables the entire chip. In this state the crystal oscillator, and both PLLs are turned off. Furthermore, all outputs are deactivated to low state, all inputs are inactive except for PWR_DWN#.

Block Diagram



Pin Configuration



Pin Description Table

Pin	Type	Qty.	P/S	Symbol	Description
1	I/O	1	3.3	REF/SEL2	Normally 14.318 MHz reference output. During power up this pin is sampled as SEL2, clock bit 2. Internally pulled down w/100K Ohm.
3	I	1	3.3	XTAL_IN	14.318 MHz crystal input
4	O	1	3.3	XTAL_OUT	14.318 MHz crystal output
7, 8	O	2	3.3	3V66 [0-1]	66 MHz
11, 12, 13, 15, 16, 18, 19, 20	O	8	3.3	PCI [0-7]	PCI outputs
25, 26	O	1	3.3	48 MHz [0-1]	48 MHz output
28, 29	I	2	3.3	SEL [0-1]	LVTTL level frequency select inputs, internal pullup
30	I/O	1	3.3	SDATA	I^2C compatible SDATA, internal pullup
31	I	1	3.3	SCLOCK	I^2C compatible SCLOCK, internal pullup
32	I	1	3.3	PWRDWN#	LVTTL level Power Down control input, active low
34, 36, 37, 39, 40, 42, 43, 45, 46	O	9	3.3	DCLK, SDRAM [0-7]	SDRAM and DCLK outputs. 100/133 MHz depending on SEL [0-2]. SDRAM [0-7] can be turned off through I^2C, but not DCLK.
49, 50, 52	O	3	2.5	CPU [0-2]	Host Bus Clock output. 66/100/133 MHz depending on SEL [0-2]
54, 55	O	2	2.5	APIC [0-1]	33 MHz APIC clock, synchronous to PCI clock
2, 9, 10, 21, 27, 33, 38, 44	PWR	8	3.3	$V_{DD3.3}$	3.3V Power Supply
5, 6, 14, 17, 24, 35, 41, 47	GND	8	N/A	$V_{SS3.3}$	3.3V Ground
51, 53	PWR	2	2.5	$V_{DD2.5}$	2.5V Power Supply
48, 56	GND	2	N/A	$V_{SS2.5}$	2.5V Ground
22	PWR	1	3.3	V_{DDA}	3.3V Core Power Supply
23	GND	1	N/A	V_{SSA}	3.3V Core Ground

Frequency Select Function Table

SEL2	SEL1	SEL0	Function
X	0	0	Tri-State
X	0	1	Test
0	1	0	CPU = 66 MHz, SDRAM = 100 MHz
0	1	1	CPU = 100 MHz, SDRAM = 100 MHz
1	1	0	CPU = 133 MHz, SDRAM = 133 MHz
1	1	1	CPU = 133 MHz, SDRAM = 100 MHz

DC Specifications

DC parameters must be sustainable under steady state (DC) conditions.

Absolute Maximum DC Power Supply

Symbol	Parameter	Min.	Max.	Units	Notes
V_{DDA}	3.3V Core Supply Voltage	-0.5	4.6	V	
$V_{DD2.5}$	2.5V I/O Supply Voltage	-0.5	3.6	V	
$V_{DD3.3}$	3.3V I/O Supply Voltage	-0.5	4.6	V	
T_S	Storage Temperature	-65	150	°C	

Absolute Maximum DC I/O

Symbol	Parameter	Min.	Max.	Units	Notes
V_{IH3}	3.3V Input High Voltage	-0.5	4.6	V	1
V_{IL3}	3.3V Input Low Voltage	-0.5		V	
ESD prot.	Input ESD protection	2000		V	2

Notes:
1. Maximum V_{IH} is not to exceed maximum V_{DD}.
2. Human body model.

DC Operating Specification

Symbol	Parameter	Condition	Min.	Max.	Units	Notes
V_{DDA}	3.3V Core Supply Voltage	3.3V ±5%	3.135	3.465	V	2
$V_{DD3.3}$	3.3V I/O Supply Voltage	3.3V ±5%	3.135	3.465	V	2
$V_{DD2.5}$	2.5V I/O Supply Voltage	2.5V ±5%	2.375	2.625	V	2
V_{IH3}	3.3V Input High Voltage	V_{DDA}	2.0	V_{DD}+0.3	V	4
V_{IL3}	3.3V Input Low Voltage	V_{SS}-0.3		0.8	V	4
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DD3.3}$	-5	+5	µA	1,4
C_{in}	Input Pin Capacitance			5	pF	
C_{xtal}	Xtal Pin Capacitance		13.5	22.5	pF	3
C_{out}	Output Pin Capacitance			6	pF	
L_{PIN}	Pin Inductance			7	nH	
T_A	Ambient Temperature	No Airflow	0	70	°C	

Notes:
1. Input Leakage Current does not include inputs with Pull-Up or Pull-down resistors.
2. No power sequencing is implied or allowed to be required in the system.
3. As seen by the crystal. Device is intended to be used with a 17-20pF AT crystal.
4. All inputs referenced to 3.3V power supply.

Clock Output Buffer DC Characteristics

Buffer Name	V_{CC} Range (V)	Impedance (Ohm)	Buffer Type
CPU, APIC	2.375 - 2.625	13.5-45	Type 1
48MHz, REF	3.135-3.465	20-60	Type 3
SDRAM		10-24	Type 4
PCI, 3V66		12-55	Type 5

Type 1: CPU, APIC Clocks

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-Up Current	V_{OUT} = 1.0V	–27			mA
I_{OHMAX}		V_{OUT} = 2.375V			–27	
I_{OLMIN}	Pull-Down Current	V_{OUT} = 1.2V	30			
I_{OLMAX}		V_{OUT} = 0.3V			30	

Type 3: 48 MHz, REF Clocks

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-Up Current	V_{OUT} = 1.0V	–29			mA
I_{OHMAX}		V_{OUT} = 3.135V			–23	
I_{OLMIN}	Pull-Down Current	V_{OUT} = 1.95V	29			
I_{OLMAX}		V_{OUT} = 0.4V			27	

Type 4: SDRAM Clocks

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-Up Current	V_{OUT} = 2.0V	–54			mA
I_{OHMAX}		V_{OUT} = 3.135V			–46	
I_{OLMIN}	Pull-Down Current	V_{OUT} = 1.0V	54			
I_{OLMAX}		V_{OUT} = 0.4V			53	

Type 5: PCI, 3V66 Clocks

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
I_{OHMIN}	Pull-Up Current	V_{OUT} = 1.0V	–33			mA
I_{OHMAX}		V_{OUT} = 3.135V			–33	
I_{OLMIN}	Pull-Down Current	V_{OUT} = 1.95V	30			
I_{OLMAX}		V_{OUT} = 0.4V			38	

AC Timing Specifications

Symbol	Parameter	66 MHz		100 MHz		133 MHz		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
T Period	Host/CPU CLK period	15.0	15.5	10.0	10.5	7.5	8.0	ns	2, 7
T HIGH	Host/CPU CLK high time	5.2	N/A	3.0	N/A	1.87	N/A	ns	3
T LOW	Host/CPU CLK low time	5.0	N/A	2.8	N/A	1.67	N/A	ns	4
Edge Rate	Rising Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	1.0	4.0	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	1.0	4.0	1.0	4.0	V/ns	
T Rise	Host/CPU CLK rise time	0.4	1.6	0.4	1.6	0.4	1.6	ns	1, 6
T Fall	Host/CPU CLK fall time	0.4	1.6	0.4	1.6	0.4	1.6	ns	1, 6
T Period	APIC 33 MHz CLK period	30.0	N/A	30.0	N/A	30.0	N/A	ns	2, 7
T HIGH	APIC 33 MHz CLK high time	12.0	N/A	12.0	N/A	12.0	N/A	ns	3
T LOW	APIC 33 MHz CLK low time	12.0	N/A	12.0	N/A	12.0	N/A	ns	4
Edge Rate	Rising Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	1.0	4.0	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 1 Buffer 2.5V)	1.0	4.0	1.0	4.0	1.0	4.0	V/ns	
T Rise	APIC 33 MHz CLK rise time	0.4	1.6	0.4	1.6	0.4	1.6	ns	1, 6
T Fall	APIC 33 MHz CLK fall time	0.4	1.6	0.4	1.6	0.4	1.6	ns	1, 6
T Period	3V66 CLK period	15.0	16.0	15.0	16.0	15.0	16.0	ns	2, 7
T HIGH	3V66 CLK high time	5.25	N/A	5.25	N/A	5.25	N/A	ns	3
T LOW	3V66 CLK low time	5.5	N/A	5.5	N/A	5.5	N/A	ns	4
Edge Rate	Rising Edge Rate (Type 5 Buffer 3.3V)	1.0	4.0	1.0	4.0	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 5 Buffer 3.3V)	1.0	4.0	1.0	4.0	1.0	4.0	V/ns	
T Rise	3V66 CLK rise time	0.5	2.0	0.5	2.0	0.5	2.0	ns	1, 6
T Fall	3V66 CLK fall time	0.5	2.0	0.5	2.0	0.5	2.0	ns	1, 6
T Period	PCI & APIC CLK period	30.0	N/A	30.0	N/A	30.0	N/A	ns	2, 7
T HIGH	PCI & APIC CLK high time	12.0	N/A	12.0	N/A	12.0	N/A	ns	3
T LOW	PCI & APIC CLK low time	12.0	N/A	12.0	N/A	12.0	N/A	ns	4
Edge Rate	Rising Edge Rate (Type 5 Buffer 3.3V)	1.0	4.0	1.0	4.0	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 5 Buffer 3.3V)	1.0	4.0	1.0	4.0	1.0	4.0	V/ns	
T Rise	PCI & APIC CLK rise time	0.5	2.0	0.5	2.0	0.5	2.0	ns	1, 6
T Fall	PCI & APIC CLK fall time	0.5	2.0	0.5	2.0	0.5	2.0	ns	1, 6
T Period	SDRAM CLK period	N/A	N/A	10.5	10.5	7.5	8.0	ns	2, 7
T HIGH	SDRAM CLK high time	N/A	N/A	3.0	N/A	1.87	N/A	ns	3
T LOW	SDRAM CLK low time	N/A	N/A	2.8	N/A	1.67	N/A	ns	4
Edge Rate	Rising Edge Rate (Type 4 Buffer 3.3V)	N/A	N/A	1.5	4.0	1.0	4.0	V/ns	
Edge Rate	Falling Edge Rate (Type 4 Buffer 3.3V)	N/A	N/A	1.5	4.0	1.0	4.0	V/ns	
T Rise	SDRAM CLK rise time	N/A	N/A	0.4	1.6	0.4	1.6	ns	1, 6
T Fall	SDRAM CLK fall time	N/A	N/A	0.4	1.6	0.4	1.6	ns	1, 6
TpZL, tpZH	Output Enable Delay (All Outputs)	1.0	10.0	1.0	10.0	1.0	10.0	ns	
TpLZ, tpZH	Output Disable Delay (All Outputs)	1.0	10.0	1.0	10.0	1.0	10.0	ns	
Tstable	All clock stabilization from power-up		3		3		3	ms	5

(see notes on next page)

AC Timing Notes:

1. Output drivers must have monotonic rise/fall times through the specified V_{OL}/V_{OH} levels.
2. Period, jitter, offset and skew measured on rising edge @1.25V for 2.5V clocks and @ 1.5V for 3.3V clocks.
3. T_{HIGH} is measured at 2.0V for 2.5V outputs, 2.4V for 3.3V outputs.
4. T_{LOW} is measured at 0.4V for all outputs.
5. The time specified is measured from when the power supply achieves its nominal operating level (typical condition $V_{DD3.3V}$ = 3.3V) until the frequency output is stable and operating within specification.
6. T_{RISE} and T_{FALL} are measured as a transition through the threshold region V_{OL} = 0.4V and V_{OH} = 2.0V (1mA) JEDEC Specification.
7. The average period over any 1µs period of time must be greater than the minimum specified period.

Group Skew And Jitter Limits

Output Group	Pin-pin Skew MAX.	Cycle-Cycle Jitter	Duty Cycle	Nom V_{DD}	Skew, jitter measure point
CPU	175ps	250ps	45/55	2.5V	1.25V
SDRAM	250ps	250ps	45/55	3.3V	1.5V
APIC	250ps	500ps	45/55	2.5V	1.25V
48 MHz	N/A	500ps	45/55	3.3V	1.5V
3V66	175ps	500ps	45/55	3.3V	1.5V
PCI	500ps	500ps	45/55	3.3V	1.5V
REF	N/A	1000ps	45/55	3.3V	1.5V

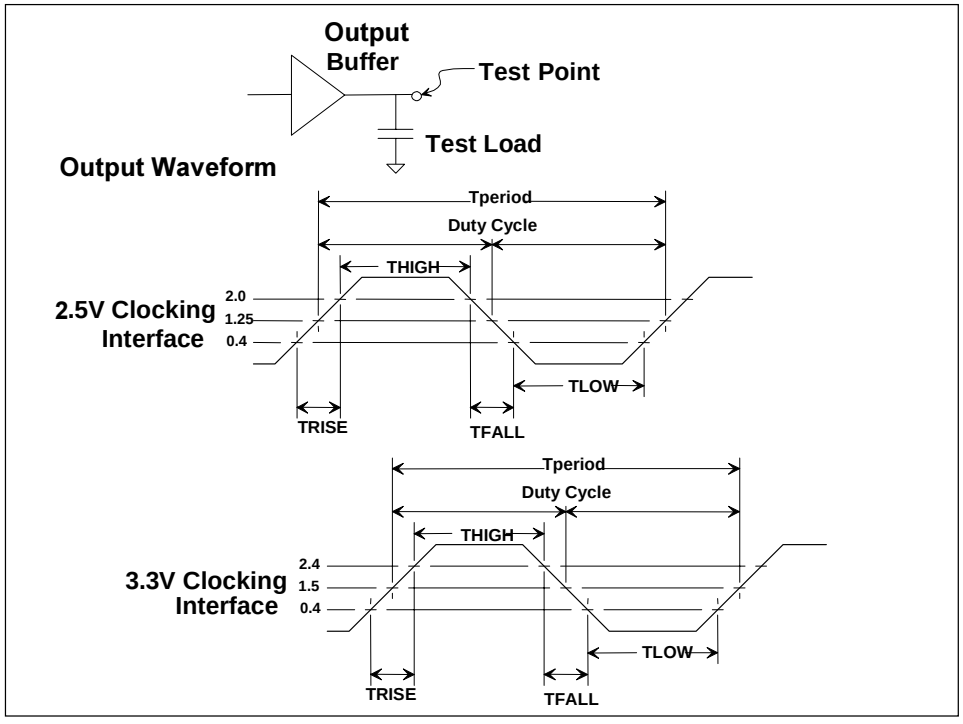


Figure 1.

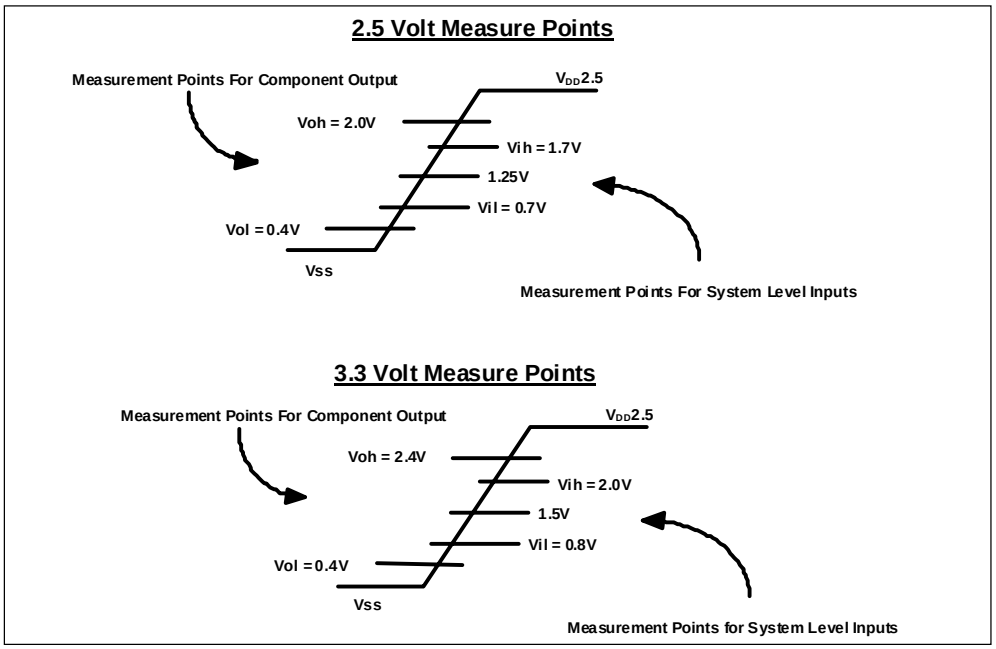


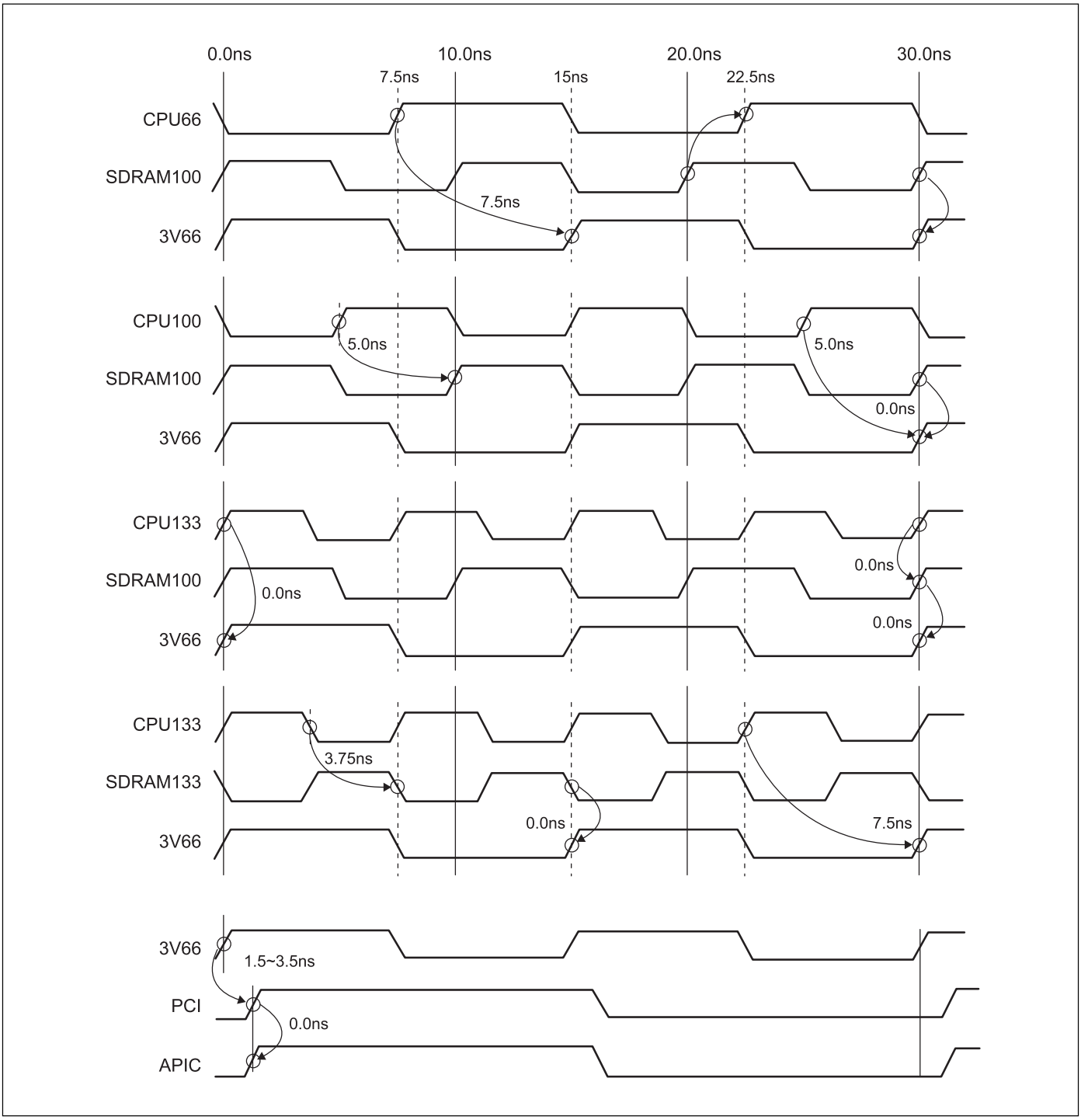
Figure 2. Component Versus System Measure Points

Group to Group Skew Tolerance

Group	CPU66	CPU66	CPU100	CPU100	CPU133	CPU133
	Offset	Tolerance	Offset	Tolerance	Offset	Tolerance
CPU to SDRAM100	2.5ns	500ps	5.0ns	500ps	0.0ns	500ps
CPU to SDRAM133	N/A	N/A	N/A	N/A	5.0ns	500ps
CPU to 3V66	5.0ns	500ps	5.0ns	500ps	0.0ns	500ps
SDRAM100 to 3V66	0.0ns	500ps	0.0ns	500ps	0.0ns	500ps
SDRAM133 to 3V66	N/A	N/A	N/A	N/A	0.0ns	500ps
3V66 to PCI	1.5~3.5ns	500ps	1.5~3.5ns	500ps	1.5~3.5ns	500ps
PCI to APIC	0.0ns	1.0ns	0.0ns	1.0ns	0.0ns	1.0ns
48 MHz & DOT	Async	N/A	Async	N/A	Async	N/A

Note:
Only offset specifications listed above are guaranteed/tested. The specification is treated as ANY output within first specified bank to ANY output of the second specified bank. Pin-pin skew is implied within offset specification, jitter is not. Previous offset specifications such as CPU to PCI offset are no longer required.

Group Offset Measurement Clarification



Clock Enable Configuration

PWR_DWN#	CPU	SDRAM	APIC	3V66	PCI	REF, 48 MHZ	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON

Notes:
1. LOW means outputs held static LOW.
2. ON means active.
3. PWR_DWN# pulled LOW, impacts all outputs including REF and 48 MHz outputs.

Truth Table

SEL2	SEL1	SEL0	CPU	SDRAM	3V66	PCI	48 MHz	REF	APIC	Notes
X	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	1
X	0	1	TCLK/2	TCLK/2	TCLK/3	TCLK/6	TCLK/2	TCLK	TCLK/6	3, 4
0	1	0	66 MHz	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	2, 5, 6
0	1	1	100 MHz	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	
1	1	0	133 MHz	133 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	
1	1	1	133 MHz	100 MHz	66 MHz	33 MHz	48 MHz	14.318 MHz	33 MHz	

Notes:

1. Required for board level “bed of nails” testing.
2. “Normal” mode of operation.
3. TCLK is a test clock over driven on the XTAL_IN input during test mode.
4. Required for DC output impedance verification.
5. Range of reference frequency allowed is min = 14.316 MHz, nominal = 14.31818 MHz, max = 14.32 MHz.
6. Frequency accuracy of 48 MHz is ±167PPM to match 48 MHz default.

System Clock Design Considerations

PI6C110E supports 4 operational modes. It varies the FSB (Front Side Bus) and SDRAM clock frequencies. FSB selection is 66 MHz, 100 MHz or 133 MHz. SDRAM frequency is either 100 MHz or 133 MHz. The supported modes are:

SEL[2:0]	Mode	CPU	SDRAM	3V66	APIC/PCI	
0 1 0	Mode 0	66	100	66	33	
0 1 1	Mode 1	100	100	66	33	default
1 1 0	Mode 2	133	133	66	33	
1 1 1	Mode 3	133	100	66	33	

The clock select pins, SEL[2:0] have the appropriate 100K (±20K) internal pull up and pull down to allow the system defaults to 100 MHz CPU clock and 100 MHz SDRAM clock without external strapping resistor. SEL2 in pulled down, SEL1 and SEL0 is pulled up to indicate “0 1 1”.

The APIC clock is a 33 MHz, the same frequency and phase as the PCI clocks, except it is powered by 2.5V supply. APIC and PCI clocks are always in phase with the other clocks. In Mode 0, CPU and 3V66 are inverted. In Mode 1 and Mode 3, CPU and SDRAM clocks are inverted.

System Debug and Timing Margin Analysis

To support system debug and to measure/test margin analysis, the internal PI6C110E oscillator circuits allows the input crystal frequency to be driven with parallel resonant crystal with frequency range of 10 MHz to 20 MHz in laboratory environment. The alternative is to put the device in TEST mode, SEL2 = “don’t care”, SEL1 = “1” and SEL0 = “0”. Then drive a clock signal to XTAL_IN (pin 3) from a signal generator and float XTAL_OUT (pin 4).

Power Management

Maximum Current

Condition	Max. 2.5 supply consumption, Max. discreet cap loads, $V_{DD2.5}$ = 2.625V All static inputs = $V_{DD3.3}$ or V_{SS}	Max. 3.3 supply consumption, Max. discreet cap loads, $V_{DD3.3}$ = 3.465V, All static inputs = $V_{DD3.3}$ or V_{SS}
Power Down Mode (PWRDWN#) = 0)	100µA	200µA
CPU = 66 MHz, SDRAM = 100 MHz SEL [0-2] = 010	70mA	280mA
CPU = 100 MHz, SDRAM = 100 MHz SEL [2-0] = 011	100mA	280mA
CPU = 133 MHz, SDRAM = 133 MHz SEL [2-0] = 110	TBD	TBD
CPU = 133 MHz, SDRAM = 100 MHz SEL [2-0] = 111	TBD	TBD

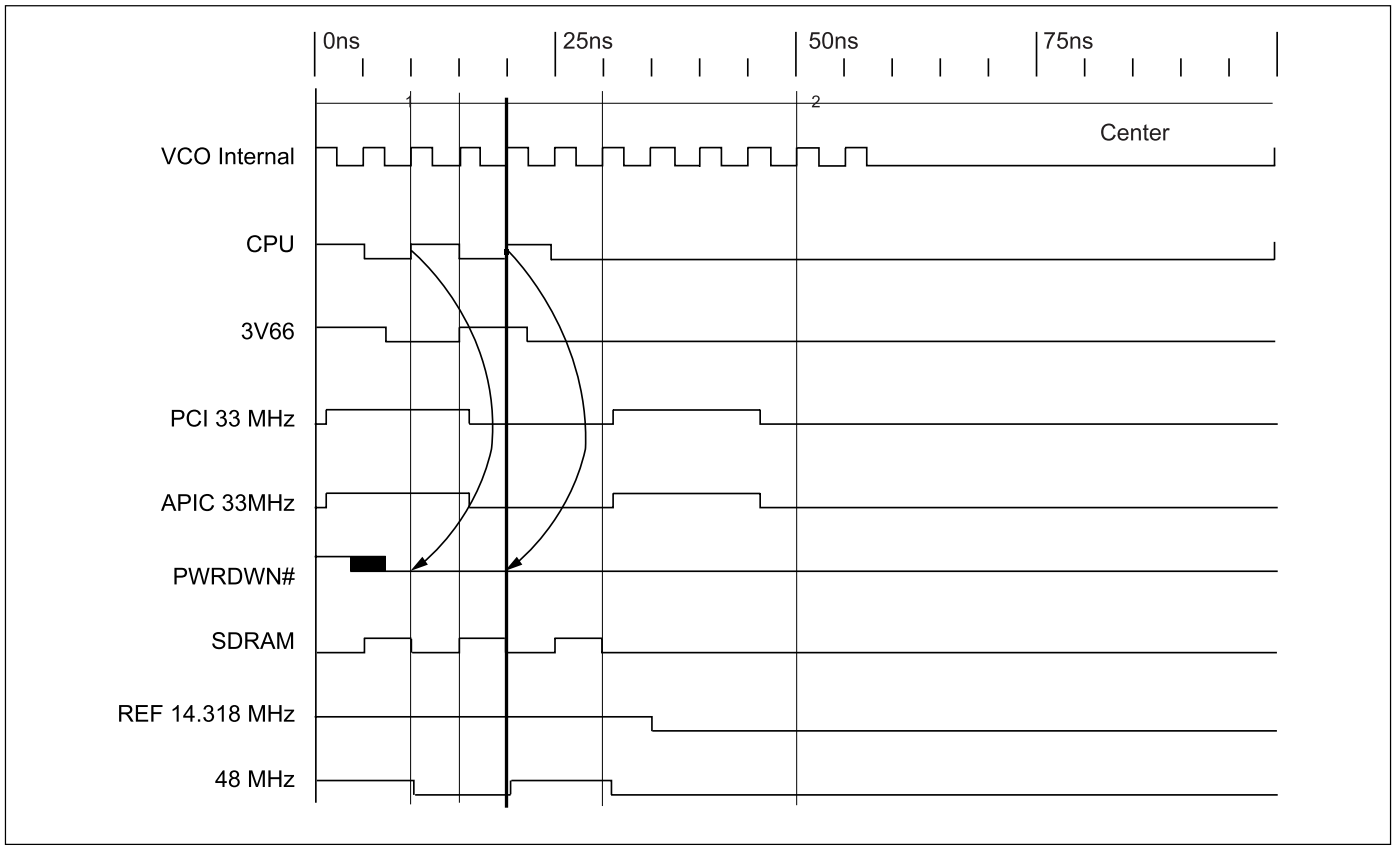
Power Management

Signal	Signal State	Latency
		No. of rising edges of PCI Clocks
PWRDWN#	1 (normal operation)	3ms
	0 (power down)	See Timing Diagram Below

Notes:

1. Clock on/off latency is defined in the number of rising edges of free running PCI clock between the clock disable goes low/high to the first valid clock comes out of the device.
2. Power up latency is when PWRDWN# goes inactive (high) to when the first valid clocks are driven from the device.

The power down selection is used to put the part into a very low power state without turning off the power to the part. PWRDWN# is an asynchronous active low input. This signal is synchronized internal to the device prior to powering down the clock synthesizer. PWRDWN# is an asynchronous function for powering up the system. Internal clocks are not running after the device is put in power down. When PWRDWN# is active low all clocks are driven to a low value and held prior to turning off the VCO's and the crystal. The power -up latency needs to be less than 3ms. The REF and 48 MHz clocks are expected to be stopped in the LOW state as soon as possible. Due to the state of the internal logic, stopping and holding the REF clock outputs in the LOW state may require more than one clock cycle to complete.



PWRDWN# Timing Diagram

Notes:
1. Once the PWRDWN# signal is sampled LOW for two consecutive rising edges of CPU clock, clocks of interest should be held LOW on the next high to low transition.
2. PWRDWN# is an asynchronous input and metastable conditions could exist. This signal is synchronized inside the part.
3. The shaded sections on the SDRAM, REF, and 48 MHz clocks indicate don't care states.
4. Diagrams shown with respect to 100 MHz. Similar operation when CPU is 66/133 MHz.

Minimum and Maximum Lumped Capacitive Loads

Clock	Min. Load	Max. Load	Units	Notes
CPU	10	20	pF	1 device load, possible 2 loads
PCI	10	30		Must meet PCI 2.1 requirements
SDRAM	20	30		PC100/PC133 specs
3V66	10	30		1 device load, possible 2 loads
48MHz	10	20		1 device load,
REF	10	20		1 device load,
APIC	10	20		1 device load,

I²C Considerations

1. **Address Assignment:** Any clock driver in this specification can use the single, 7 bit address shown below. All devices can use the address if only one master clock driver is used in a design.

The following address was confirmed by Philips on 09/04/96.

A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	0	1	0

Note:
The R/W# bit is used by the I²C controller as a data direction bit. A "zero" indicates a transmission (WRITE) to the clock device. A 'one' indicates a request for data (READ) from the clock driver. Since the definition of the clock buffer only allows the controller to WRITE data; the R/W# bit of the address will always be seen as a "zero."

2. **Slave/Receiver:** The clock driver is assumed to require only slave/receiver functionality.

3. **Data Transfer Rate:** 100 kbits/s (standard mode) is the base functionality.

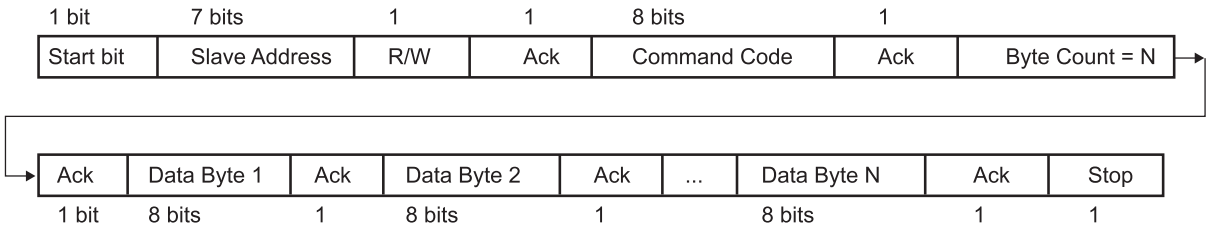
4. **Logic Levels:** Assume all devices are based on a 3.3 Volt supply.

5. **Data Byte Format:** Byte format is 8-bits.

6. **Data Protocol:**
To simplify the clock I²C interface, the clock driver serial protocol was specified to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. Indexed bytes are not allowed.

The clock driver must meet this protocol which is more rigorous than previously stated I²C protocol. Treat the description from the viewpoint of controller. The controller "writes" to the clock driver and if possible would "read" from the clock driver.

"The block write begins with a slave address and a write condition. After the command code the host (controller) issues a byte count which describes how many more bytes will follow in the message. If the host had 20 bytes to send, the first byte would be the number 20 (14h), followed by the 20 bytes of data. The byte count may not be 0. A block write command is allowed to transfer a maximum of 32 data bytes."



Note: The acknowledgment bit is returned by the slave/receiver (the clock driver).

Consider the command code and the byte count bytes required as the first two bytes of any transfer. The command code is software programmable via the controller, but will be specified as 0000 0000 in the clock specification. The byte count byte is the number of additional bytes required for the transfer, not counting the command code and byte count bytes. Additionally, the byte count byte is required to be a minimum of 1 byte and a maximum of 32 bytes to satisfy the above requirement. For example:

Byte count byte		Notes
MSB	LSB	
0000	0000	Not allowed. Must have at least one byte.
0000	0001	Data for functional and frequency select register (currently byte 0 in spec)
0000	0010	Reads first two bytes of data (byte 0, then byte 1)
0000	0011	Reads first three bytes of data (byte 0, 1, 2 in order)
0000	0100	Reads first four bytes of data (byte 0, 1, 2, 3 in order)
0000	0101	Reads first five bytes of data (byte 0, 1, 2, 3, 4 in order)
0000	0110	Reads first six bytes of data (byte 0, 1, 2, 3, 4, 5 in order)
0000	0111	Reads first seven bytes of data (byte 0, 1, 2, 3, 4, 5, 6 in order)
0010	0000	Max. byte count supported = 32

A transfer is considered valid after the acknowledge bit corresponding to the byte count is read by the controller. The serial controller interface can be simplified by discarding the information in both the command code and the byte count bytes and simply reading all the bytes that are sent to the clock driver after being addressed by the controller. It is expected that the controller will not provide more bytes than the clock driver can handle.

7. **Clock Stretching:** The clock device must not hold/stretch the SCLK or SDATA lines low for more than 10 mS. Clock stretching is discouraged and should only be used as a last resort. Stretching the clock/data lines for longer than this time puts the device in an error/time-out mode and may not be supported in all platforms. It is assumed that all data transfers can be completed as specified without the use of clock/data stretching.

8. **General Call:** It is assumed that the clock driver will not have to respond to the "general call."

9. **Electrical Characteristics:** All electrical characteristics must meet the standard mode specifications found in section 15 of the I^2C specification.

   A) **Pull-Up Resistors:** There is a 100k internal resistor pull-ups on the SDATA and SCLK inputs. Assume that the board designer will use a single external pull-up resistor for each line and that these values are in the 5-6K Ohm range. Assume one I^2C device per DIMM (serial presence detect), one I^2C controller, one clock driver plus one/two more I^2C devices on the platform for capacitive loading purposes.

   B) **Input Glitch Filters:** Only fast mode I^2C devices require input glitch filters to suppress bus noise. The clock driver is specified as a standard mode device and is not required to support this feature.

10. **PWRDWN#:** If a clock driver is placed in Power down mode, the SDATA and SCLK inputs are Tri-Stated and the device must retain all programming information.

For specific I^2C information consult the Philips I^2C Peripherals Data Handbook ICI2 (1996)

PI6C110E Conditions

At power up all SDRAM outputs are enabled and active. The SDATA and SCLK inputs have internal pull-up resistors with values above 100K Ohms as well for complete platform flexibility.

PI6C110E Serial Configuration Map

A) The serial bits will be read by the clock driver in the following order:

Byte 0 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte 1 - Bits 7, 6, 5, 4, 3, 2, 1, 0

Byte N - Bits 7, 6, 5, 4, 3, 2, 1, 0

B) All unused register bits (reserved and N/A) are designed as don't care. The controller will force all of these bits to a "0" level.

C) All reserved bits should be programmed to a logic level " 0."

Note:
1. Default is for ALL clocks to be enabled and all reserved bits should be programmed to a logic level "0."
Spread spectrum modulation should power up disabled (Byte 0 bit 3 = 0).

Byte 0 : Control Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Pin Description
Bit 7	–	Reserved Drive to '0'	(Active/Inactive)
Bit 6	–	Reserved Drive to '0'	
Bit 5	–	Reserved Drive to '0'	
Bit 4	–	Reserved Drive to '0'	
Bit 3	–	Spread Spectrum (1 = On / 0 = Off)	
Bit 2	26	USB1	
Bit 1	25	USB0	
Bit 0	49	CPU2	

Byte 1: Control Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Pin Description
Bit 7	36	SDRAM7	(Active/Inactive)
Bit 6	37	SDRAM6	
Bit 5	39	SDRAM5	
Bit 4	40	SDRAM4	
Bit 3	42	SDRAM3	
Bit 2	43	SDRAM2	
Bit 1	45	SDRAM1	
Bit 0	46	SDRAM0	

Byte 2: Control Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Pin Description
Bit 7	20	PCI7	(Active/Inactive)
Bit 6	19	PCI6	
Bit 5	18	PCI5	
Bit 4	16	PCI4	
Bit 3	15	PCI3	
Bit 2	13	PCI2	
Bit 1	12	PCI1	
Bit 0	–	Reserved Drive to '0'	

Byte 3 and Byte 4: Reserved Register (1 = Enable, 0 = Disable)

Bit	Pin#	Name	Pin Description
Bit 7	–	Reserved Drive to '0'	(Active/Inactive)
Bit 6	–	Reserved Drive to '0'	
Bit 5	–	Reserved Drive to '0'	
Bit 4	–	Reserved Drive to '0'	
Bit 3	–	Reserved Drive to '0'	
Bit 2	–	Reserved Drive to '0'	
Bit 1	–	Reserved Drive to '0'	
Bit 0	–	Reserved Drive to '0'	

Note: Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.

Ordering Information

P/N	Description
PI6C110EV	56-pin SSOP Package

56 Pin SSOP Package Data