PI6C2309-1

3.3V Zero-Delay Buffer

Product Features

- Zero input-output propagation delay
- Less than 200ps input to output propagation delay
- Multiple low-skew outputs
  - Output-output skew less than 250ps
  - Device-device skew less than 700ps
  - Two banks of four outputs and one ON-chip
  - Internal feedback connection
- 10 MHz to 100 MHz operating range
- Low Jitter <200ps
- 3.3V operation
- High drive option (PI6C2309-1H)
- Temperature Rating: Commercial & Industrial
- Space-saving 16-pin, 150-mil SOIC package (W16) and 16-pin TSSOP package (L16)

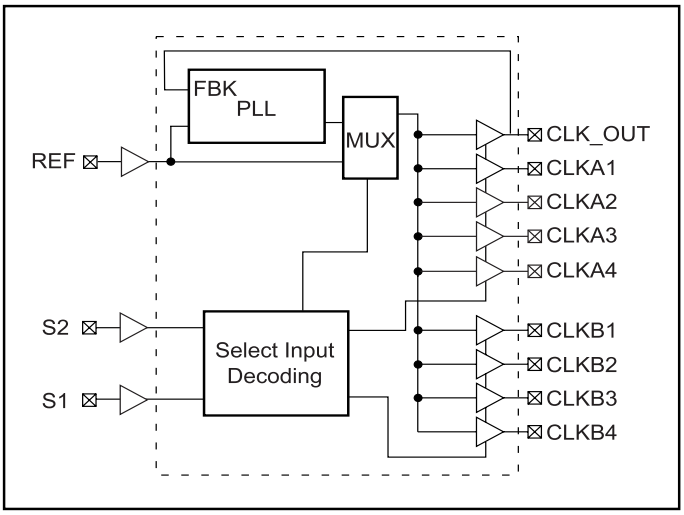
Functional Description

Providing two banks of four outputs, the PI6C2309-1 is a 3.3V zero-delay buffer designed to distribute clock signals in applications including PC, workstation, datacom, telecom, and high-performance systems.

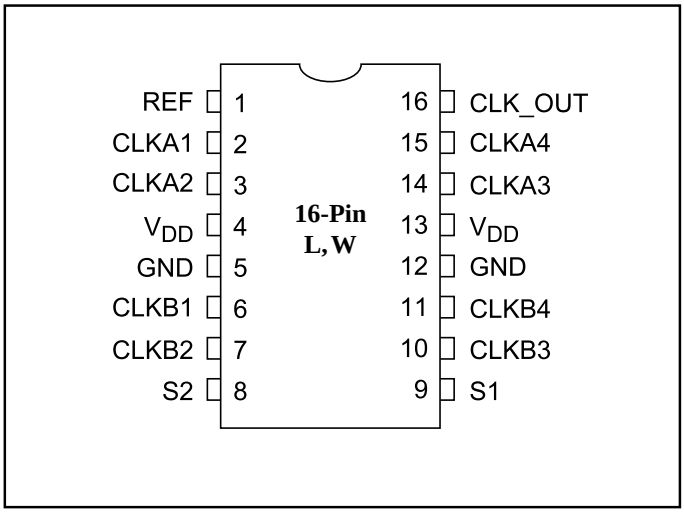
The PI6C2309-1 provides 9 copies of a clock signal that has less than 200ps propagation delay compared to the reference clock. The skew among the output clock signals for PI6C2309-1 is less than 250ps. When there are no rising edges on the REF input, the PI6C2309-1 enters a power-down state. In this mode, the PLL is off and all outputs are three-stated. This results in less than 50μA of current draw.

The PI6C2309-1 has two banks of four outputs and a CLK_OUT that can be controlled by the select inputs (see table below). If all output clocks are not required, Bank B can be three-stated. For test purposes or if the internal PLL is not needed, it can be bypassed.

Block Diagrams



Pin Configuration PI6C2309-1

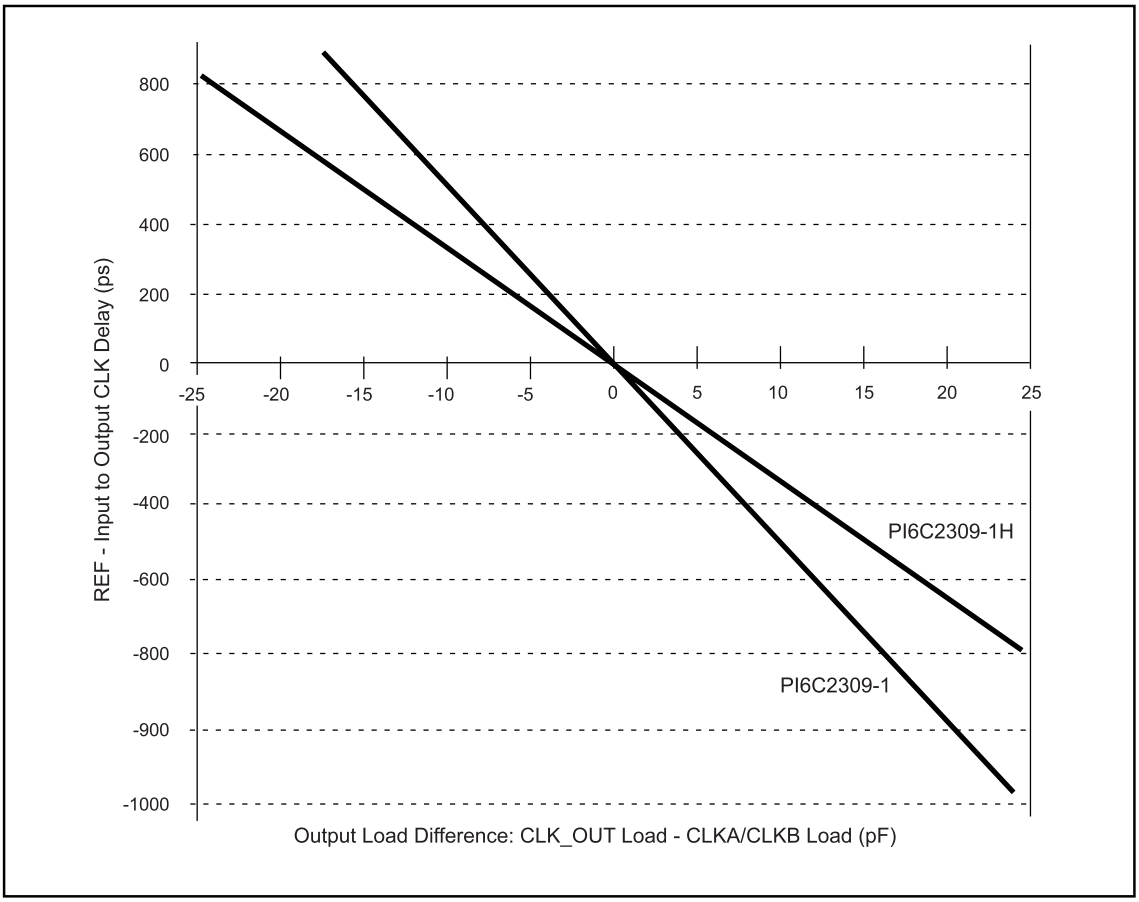


Select Input Decoding for PI6C2309-1

S2	S1	CLKA[1-4]	CLKB[1-4]	CLK_OUT	Output Source	PLL Shutdown
0	0	Three-State	Three-State	Driven	PLL	N
0	1	Driven	Three-State	Driven	PLL	N
1	0	Driven	Driven	Driven	Reference	Y
1	1	Driven	Driven	Driven	PLL	N

Zero Delay and Skew Control

REF. Input to CLKA/CLKB Delay vs. Difference in Loading between CLK_OUT pin and CLKA/CLKB pins.



To achieve a Zero Delay between the input and output, all outputs should be uniformly loaded. The relative loading of CLK_OUT(with respect to the remaining outputs) can adjust the input-output delay. This is shown in the graph above.

For applications requiring zero input-output delay, all outputs, including CLK_OUT, should be equally loaded. Even if CLK_OUT is not used, it must have a capacitive load that is equal to that on every other output. If input-output delay adjustments are required, use the above graph to calculate loading differences between the feedback output and remaining outputs.

Maximum Ratings

Supply Voltage to Ground	–0.5V to +7.0V
DC Input Voltage (Except REF)	–0.5V to V_{DD} +0.5V
DC Input Voltage REF	–0.5 to 7V
Storage Temperature	–65° C to +150°C
Maximum Soldering Temperature (10 seconds)	260°C
Junction Temperature	150°C
Static Discharge Voltage (per MIL-STD-883, Method 3015)	>2000V

Operating Conditions

Parameter	Description	Min.	Max.	Units
V_{DD}	Supply Voltage	3.0	3.6	V
T_A (2309-1, 2309-1H)	Commercial Temperature (Ambient)	0	70	°C
T_A (2309-1I, 2309-1HI)	Industrial Temperature (Ambient)	–40	85	
C_L	Load Capacitance	—	30	pF
C_{IN}	Input Capacitance	—	7	

Pin Description

Pin	Signal	Description
1	REF(1)	Input reference frequency, 5V tolerant input, allows spread spectrum clock input
2	CLKA1(2)	Clock output, Bank A
3	CLKA2(2)	Clock output, Bank A
4	V_{DD}	3.3V supply
5	GND	Ground
6	CLKB1(2)	Clock output, Bank B
7	CLKB2(2)	Clock output, Bank B
8	S2(3)	Select input, bit 2
9	S1(3)	Select input, bit 1
10	CLKB3(2)	Clock output, Bank B
11	CLKB4(2)	Clock output, Bank B
12	GND	Ground
13	V_{DD}	3.3V, supply
14	CLKA3(2)	Clock output, Bank A
15	CLKA4(2)	Clock output, Bank A
16	CLK_OUT(2)	Clock output, internal feedback on this pin

Notes:
1. Weak pull-down.
2. Weak pull-down on all outputs.
3. Weak pull-ups on these inputs.
4. REF and CLK_OUT inputs have a threshhold voltage of $V_{DD}/2$.
5. Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics (Over the operating condition)

Parameter	Description	Test Conditions	Min.	Max.	Units
V_{IL}	Input LOW Voltage(4)	—	—	0.8	V
V_{IH}	Input HIGH Voltage(4)	—	2.0	—	
I_{IL}	Input LOW Current	V_{IN} = 0V	—	50	µA
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	—	200	
V_{OL}	Output LOW Voltage(5)	I_{OL} = 8mA I_{OL} = 12mA (-1H)	—	0.4	V
V_{OH}	Output HIGH Voltage(5)	I_{OH} = –8mA I_{OH} = –12mA (–1H)	2.4	—	
I_{DD} (PD mode)	Power Down SupplyCurrent	REF = 0 MHz, S2 = 1, S1 = 0	—	50	µA
I_{DD}	Supply Current	Unloaded outputs, 66.66 MHz, Select inputs at V_{DD} or GND	—	50	mA

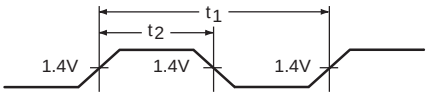
Switching Characteristics[5,6] (Over the operating condition)

Parameters	Name	Test Conditions	Min.	Typ.	Max.	Units
F_{CLK}	Output Frequency	30pF load	10		100	MHz
	Duty Cycle[5] = $t_2 \div t_1$	Measured at $V_{DD}/2$, F_{OUT} <66.66 MHz	45	50	55	%
	Duty Cycle[5] = $t_2 \div t_1$	Measured at 1.4V, F_{OUT} = 66.6 MHz	40	50	60	
t_3	Rise Time[5] @30pF	Measured between 0.8V and 2.0V			2.5	ns
t_3	Rise Time[5] @15pF				1.5	
t_3	Rise Time[5]@30pF (-1H)				1.5	
t_4	Fall Time[5] @30pF				2.5	
t_4	Fall Time[5]@15pF				1.5	
t_4	Fall Time[5]@30pF (-1H)				1.5	
t_5	Output to Output Skew[5]	All outputs equally loaded			250	ps
t_6	Delay, REF Input Rising Edge to CLK_OUT Rising Edge[5]	Measured at $V_{DD}/2$		0	±350	
t_7	Device to Device Skew[5]	Measured at $V_{DD}/2$ on the CLK_OUT pins of devices		0	700	
t_8	Output Slew Rate[5]	Measured between 0.8V and 2.0V on –1H device using Test Circuit #2	1			V/ns
t_J	Cycle to Cycle Jitter[5]	Measured at 66.67 MHz, loaded outputs @ 15pF			200	ps
t_{LOCK}	PLL Lock Time[5]	Stable power supply, valid clocks presented on REF and CLK_OUT pins			1.0	ms

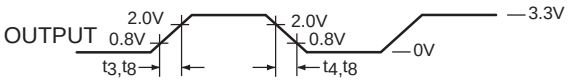
Notes:
5. Parameter is guaranteed by design and characterization. Not 100% tested in production.
6. For definition of $t_{1\text{-}8}$, see Switching Waveforms on page 5

Switching Waveforms

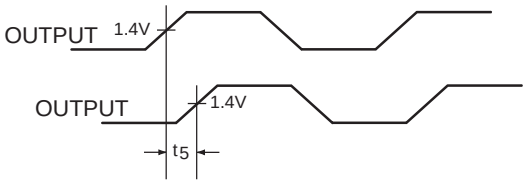
Duty Cycle Timing



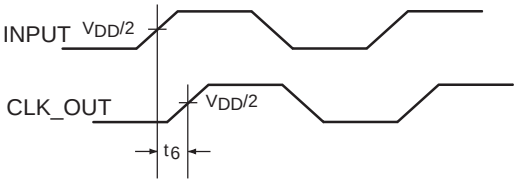
All Outputs Rise/Fall Time



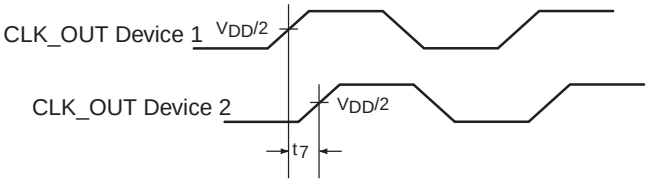
Output-Output Skew



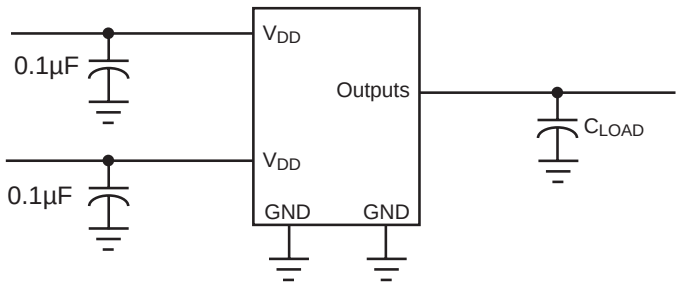
Input-Output Propagation Delay



Device-Device Skew



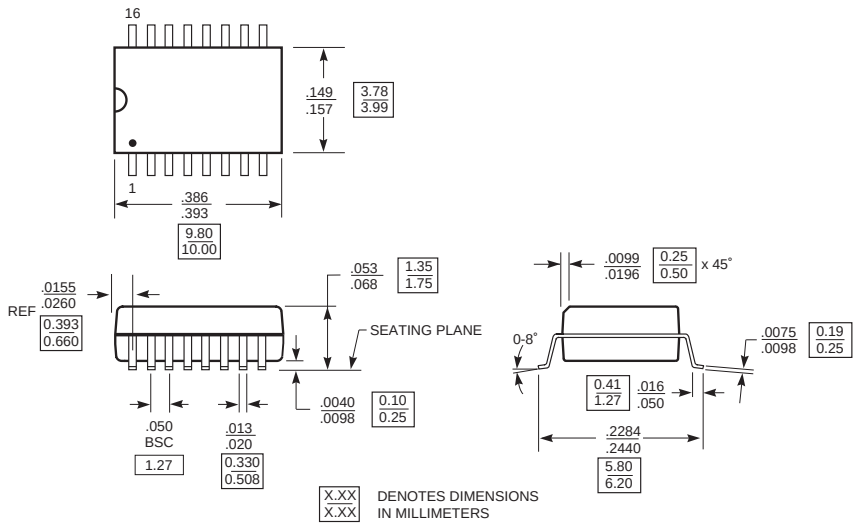
Test Circuit #1



Test Circuit for all parameters except t_8

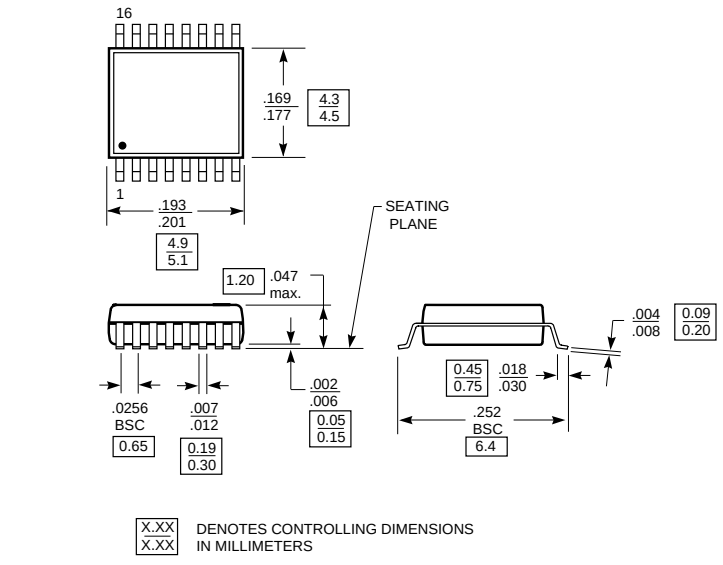
Package Diagrams

16-Pin SOIC (150-Mil Wide) W Package



Note: Controlling dimensions in millimeters. Ref: JEDEC MS - 012 AC

16-Pin TSSOP L Package



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI6C2309-1W	W16	16-pin 150-mil SOIC	Commercial
PI6C2309-1HW			
PI6C2309-1L	L16	16-pin 4.4 mm TSSOP	
PI6C2309-1HL			
PI6C2309-1WI	W16	16-pin 150-mil SOIC	Industrial
PI6C2309-1HWI			
PI6C2309-1LI	L16	16-pin 4.4 mm TSSOP	
PI6C2309-1HLI			