



# PI74ALVCH16344

## 1-Bit to 4-Bit Address/Driver with 3-State Outputs

### Product Features

- PI74ALVCH16344 is designed for low voltage operation
- $V_{CC} = 2.3V$  to  $3.6V$
- Hysteresis on all inputs
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8V$  at  $V_{CC} = 3.3V, T_A = 25^\circ C$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $< 2.0V$  at  $V_{CC} = 3.3V, T_A = 25^\circ C$
- Bus Hold retains last active bus state during 3-State, eliminating the need for external pullup resistors
- Industrial operation at  $-40^\circ C$  to  $+85^\circ C$
- Packages available:
  - 56-pin 240 mil wide plastic TSSOP (A)
  - 56-pin 300 mil wide plastic SSOP (V)

### Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

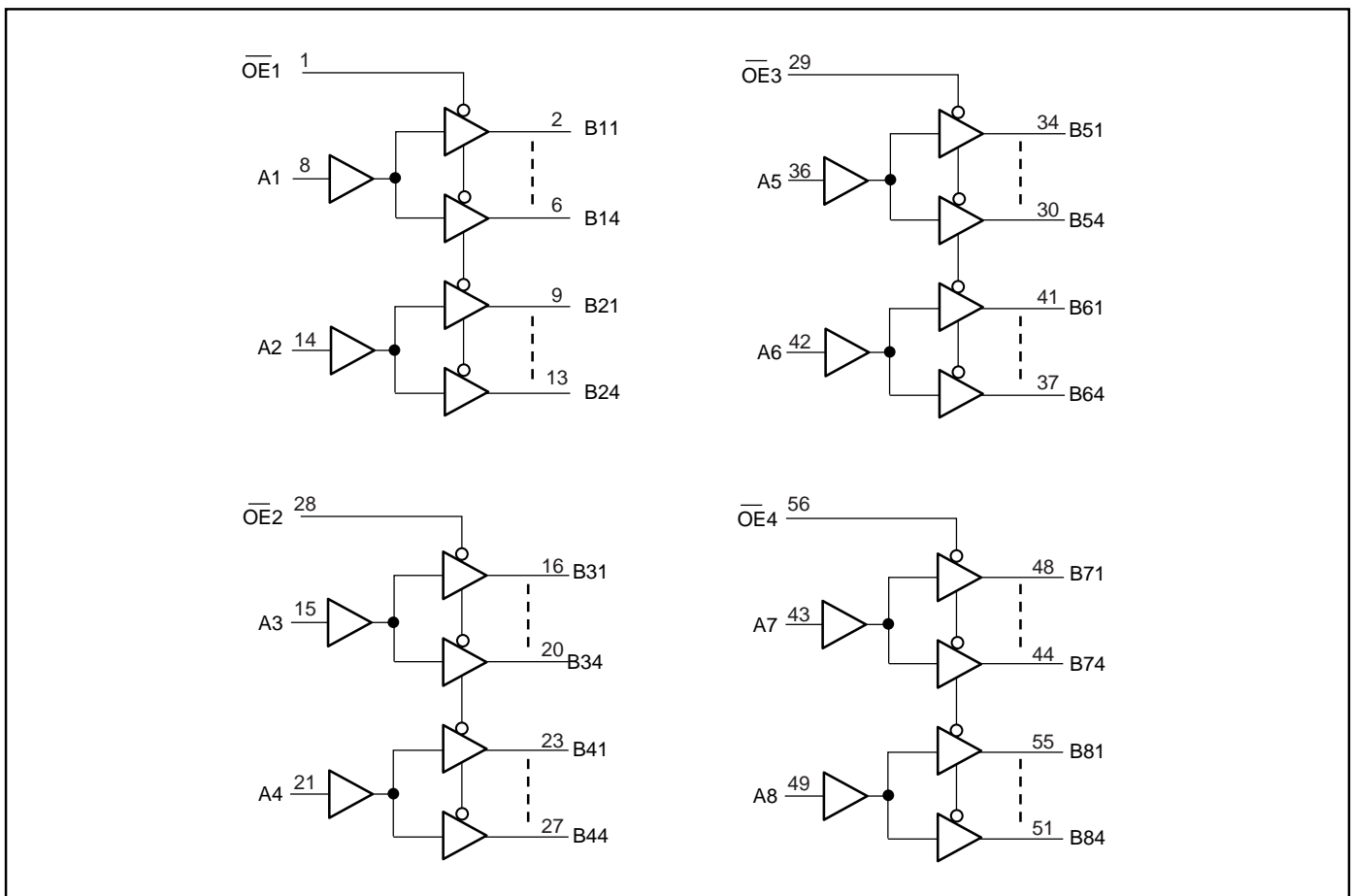
The PI74ALVCH16344 is a 1-bit to 4-bit buffer/driver designed for 2.3V to 3.6V  $V_{CC}$  operation.

The address/driver is designed for applications where four separate memory locations must be addressed by a single address.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The PI74ALVCH16344 has "Bus Hold" which retains the data input's last state whenever the data input goes to high-impedance preventing "floating" inputs and eliminating the need for pullup/down resistors.

### Logic Block Diagram



**Product Pin Description**

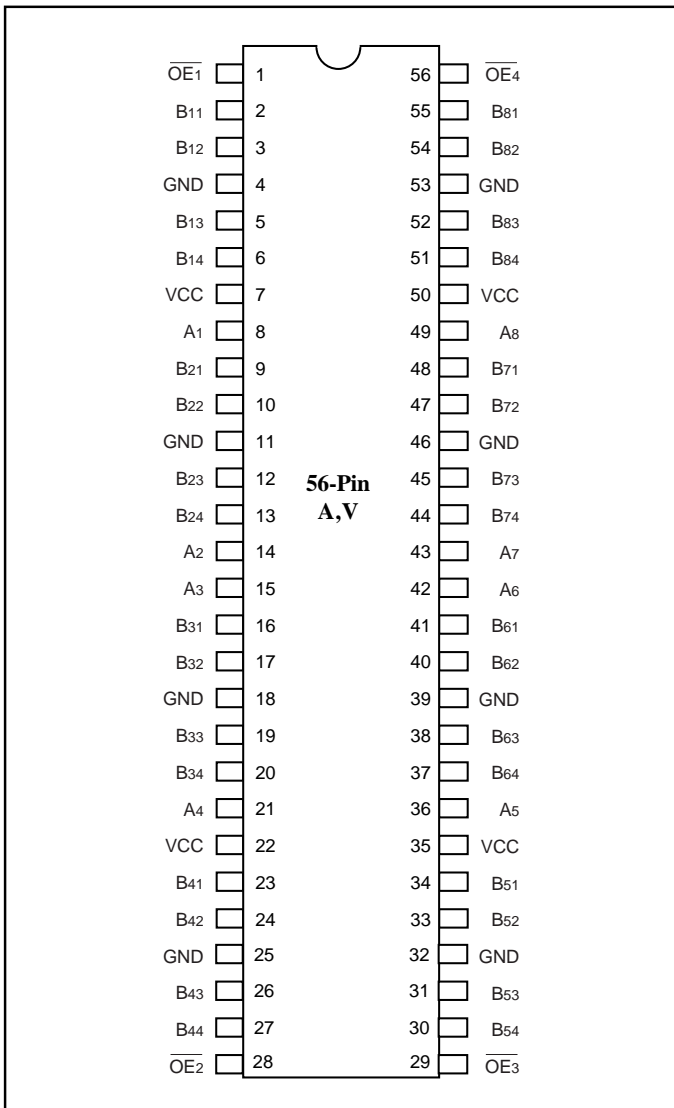
Pin Name	Description
$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
A	Inputs
B	3-State Outputs
GND	Ground
VCC	Power

**Truth Table<sup>(1)</sup>**

Inputs		Outputs
$\overline{OE}$	A	B <sub>n</sub>
L	H	H
L	L	L
H	H	Z

**Notes:**

- H = High Signal Level  
L = Low Signal Level  
X = Don't Care or Irrelevant  
Z = High Impedance

**Product Pin Configuration**


**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage Range, $V_{CC}$ .....	-0.5V to 4.6V
Input Voltage Range, $V_I$ : Except I/O ports <sup>(1)</sup> .....	-0.5V to 4.6V
I/O ports <sup>(1,2)</sup> .....	-0.5V to $V_{CC} + 0.5V$
Output Voltage Range, $V_O$ <sup>(1,2)</sup> .....	-0.5V to $V_{CC} + 0.5V$
Input Clamp Current, $I_{IK}$ ( $V_I < 0$ ) .....	-50mA
Output Clamp Current, $I_{OK}$ ( $V_O < 0$ ) .....	-50mA
Continuous Output Current, $I_O$ .....	$\pm 50mA$
Continuous Current through each $V_{CC}$ or GND .....	$\pm 100mA$
Package Thermal Impedance, $\theta_{JA}$ <sup>(3)</sup> .....	39°C/W
Storage Temperature Range, $T_{STG}$ .....	-65°C to 150°C

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Note:**

1. The input negative voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 4.6V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51.

**Recommended Operating Condition<sup>(1)</sup>**

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{CC}$	Supply Voltage		1.65		3.6	V
$V_{IH}$	HIGH Level Input Voltage	$V_{CC} = 1.65V$ to 1.95V	$0.65 \times V_{CC}$			
		$V_{CC} = 2.3V$ to 2.7V	1.7			
		$V_{CC} = 2.7V$ to 3.6V	2			
$V_{IL}$	LOW Level Input Voltage	$V_{CC} = 1.65V$ to 1.95V			$0.35 \times V_{CC}$	
		$V_{CC} = 2.3V$ to 2.7V			0.7	
		$V_{CC} = 2.7V$ to 3.6V			0.8	
$V_I$	Input Voltage		0		$V_{CC}$	
$V_O$	Output Voltage		0		$V_{CC}$	
$I_{OH}$	High-level Output Current	$V_{CC} = 1.65V$			-4	mA
		$V_{CC} = 2.3V$			-12	
		$V_{CC} = 2.7V$			-12	
		$V_{CC} = 3.0V$			-24	
$I_{OL}$	Low-level Output Current	$V_{CC} = 1.65V$			4	
		$V_{CC} = 2.3V$			12	
		$V_{CC} = 2.7V$			12	
		$V_{CC} = 3.0V$			24	
$\Delta t/\Delta v$	Input Transition rise or fall time		0		10	ns/V
$T_A$	Operating Free-Air Temperature		-40		85	°C

**Note:**

1. Unused control inputs must be held at  $V_{CC}$  or GND to ensure proper device operation.

**DC Electrical Characteristics** (Over the Operating Range,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 10\%$ )

Parameters	Test Conditions	$V_{CC}$	Min.	Typ. <sup>(1)</sup>	Max.	Units
$V_{OH}$	$I_{OH} = -100\mu\text{A}$	1.65V to 3.6V	$V_{CC} - 0.2$			V
	$I_{OH} = -4\text{mA}$	1.65V	1.2			
	$I_{OH} = -6\text{mA}$	2.3V	2.0			
	$I_{OH} = -12\text{mA}$	2.3V	1.7			
		2.7V	2.2			
		3.0V	2.4			
$I_{OH} = -24\text{mA}$	3.0V	2.0				
$V_{OL}$	$I_{OL} = 100\mu\text{A}$	1.65V to 3.6V			0.2	V
	$I_{OL} = 4\text{mA}$	1.65V			0.45	
	$I_{OL} = 6\text{mA}$	2.3V			0.4	
	$I_{OL} = 12\text{mA}$	2.3V			0.7	
		2.7V			0.4	
	$I_{OL} = 24\text{mA}$	3V			0.55	
$I_I$	$V_I = V_{CC}$ or GND	3.6V			$\pm 5$	$\mu\text{A}$
$I_I$ (Hold)	$V_I = 0.58\text{V}$	1.65V	25			
	$V_I = 1.07\text{V}$		-25			
	$V_I = 0.7\text{V}$	2.3V	45			
	$V_I = 1.7\text{V}$		-45			
	$V_I = 0.8\text{V}$	3V	75			
	$V_I = 2\text{V}$		-75			
	$V_I = 0$ to $3.6\text{V}^{(2)}$	3.6V			$\pm 500$	
$I_{OZ}^{(3)}$	$V_O = V_{CC}$ or GND	3.6V			$\pm 10$	
$I_{CC}$	$V_I = V_{CC}$ or GND $I_O = 0$	3.6V			20	
$\Delta I_{CC}$	One input at $V_{CC} - 0.6\text{V}$ , Other inputs at $V_{CC}$ or GND	3V to 3.6V			750	
$C_I$ Control Inputs	$V_I = V_{CC}$ or GND	3.3V		4		pF
$C_{IO}$ A or B ports	$V_O = V_{CC}$ or GND	3.3V		8		

**Notes:**

- All typical values are at  $V_{CC} = 3.3\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
- This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
- For I/O ports, the  $I_{OZ}$  includes the input leakage current.

**Switching Characteristics over Operating Range<sup>(1)</sup>**

Parameters	From (INPUT)	To (OUTPUT)	V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ± 0.3V		Units
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PD</sub>	A	B	1.0	5.0		4.0	1.0	3.6	ns
t <sub>EN</sub>	$\overline{OE}$	B	1.0	6.8		6.0	1.0	5.0	
t <sub>DIS</sub>	$\overline{OE}$	B	1.0	6.0		5.2	1.0	5.0	
tsk(0) <sup>(3)</sup>							-	0.35	
tsk(0) <sup>(4)</sup>							-	0.5	

**Notes:**

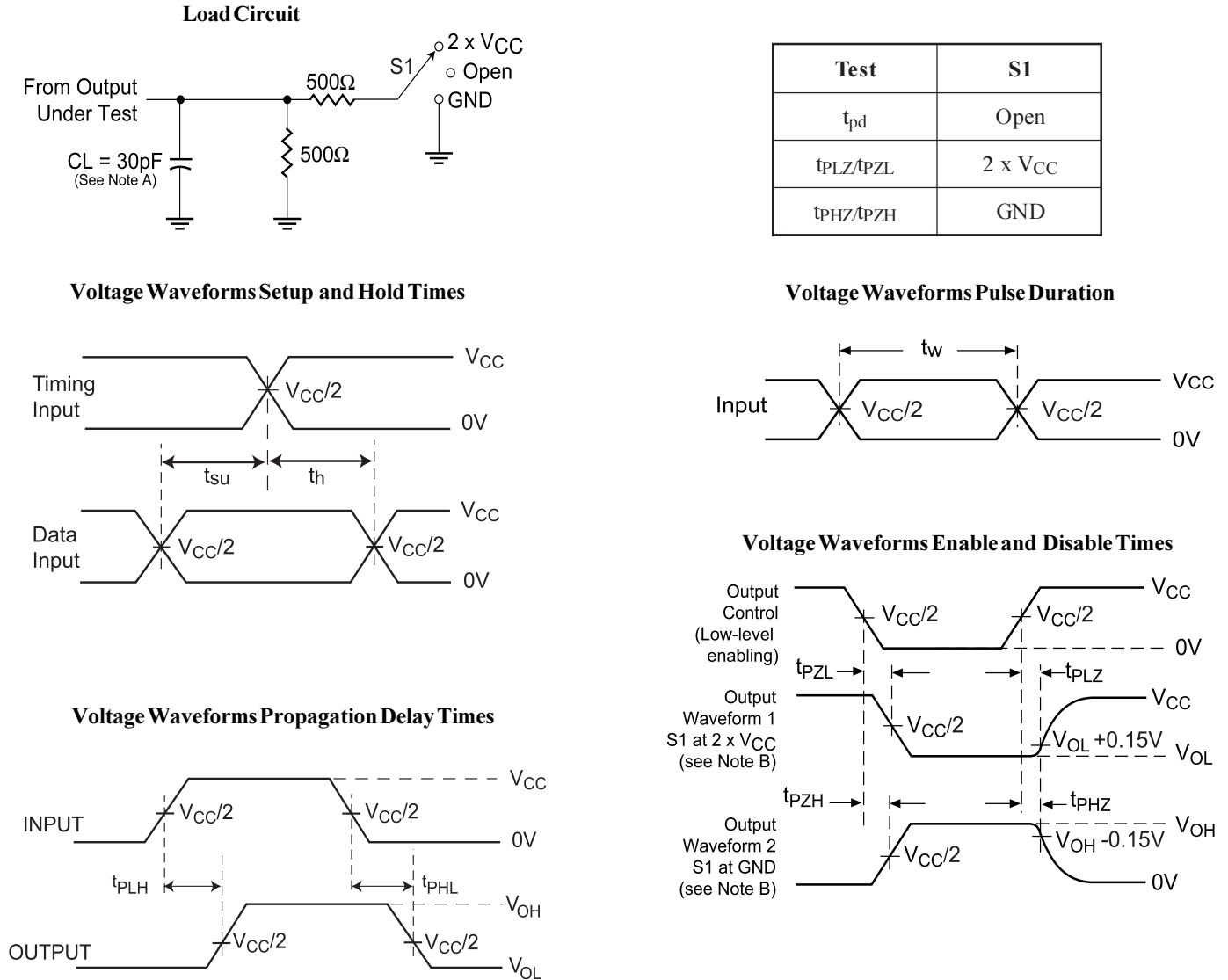
1. See test circuit and waveforms, Figures 1 and 2.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. Skew between outputs of same bank, and same device and same transition.  
This parameter is warranted but not production tested.
4. Skew between outputs of all banks, and same device, A1-A8 tied together.  
This parameter is warranted but not production tested.

**Operating Characteristics, T<sub>A</sub> = 25°C**

Parameter		Test Conditions	V <sub>CC</sub> = 2.5V ± 0.2V	V <sub>CC</sub> = 3.3V ± 0.3V	Units
			Typical		
C <sub>PD</sub> Power Dissipation Capacitance	Outputs Enabled	C <sub>L</sub> = 50pF, f = 10 MHz	68	84	pF
	Outputs Disabled		11	14	

**Parameter Measurement Information**

$V_{CC} = 2.5V \pm 0.2V$

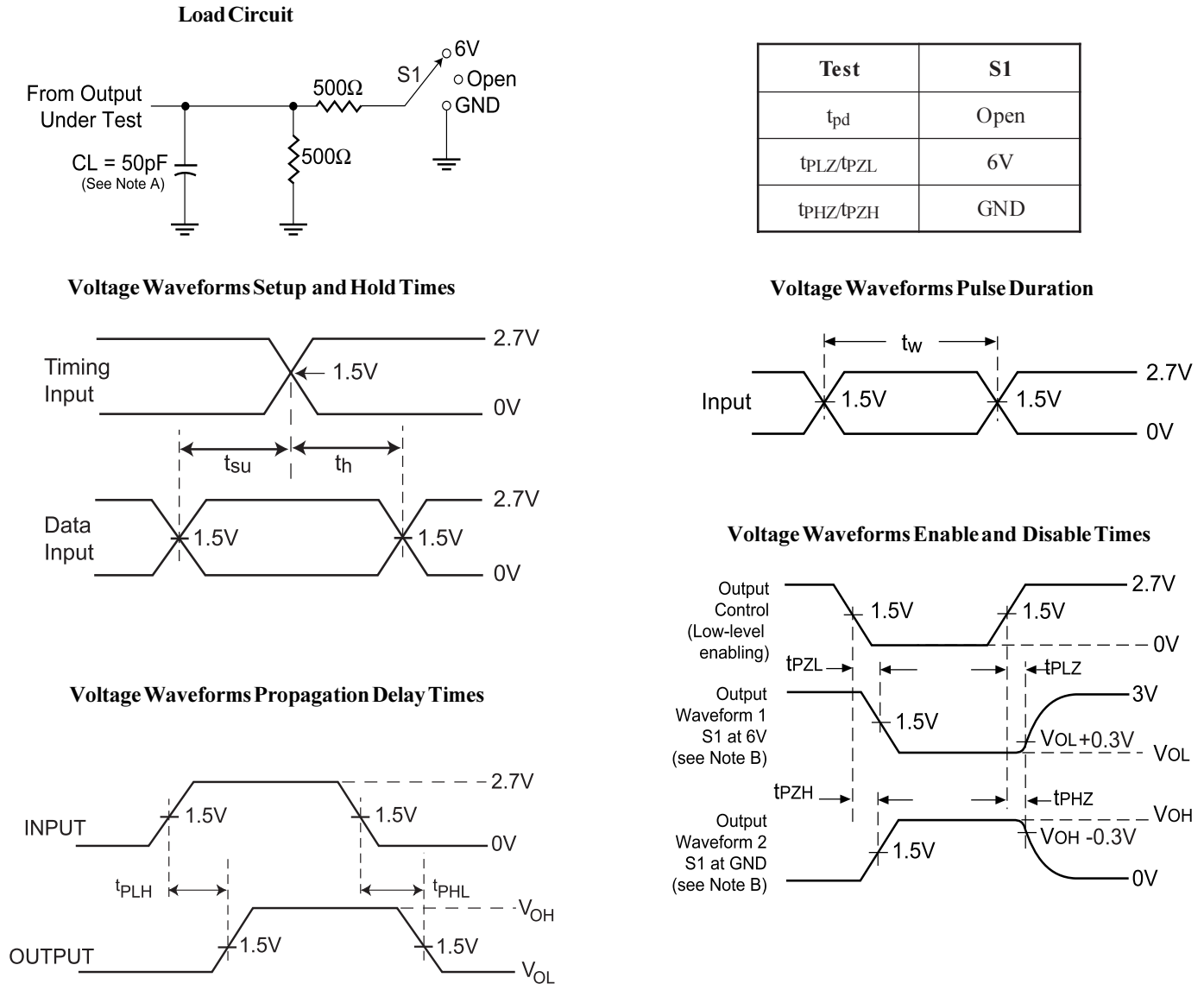


**Figure 1. Load Circuit and Voltage Waveforms**

**Notes:**

- A.** CL includes probe and jig capacitance.
- B.** Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C.** All inputs pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50\Omega$ ,  $t_r \leq 2\text{ns}$ ,  $t_f \leq 2\text{ns}$ .
- D.** The outputs are measured one at a time with one transition per measurement.
- E.**  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.**  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{ten}$ .
- G.**  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Parameter Measurement Information**  
 $V_{CC} = 2.7V$  and  $3.3V \pm 0.3V$



**Figure 2. Load Circuit and Voltage Waveforms**

**Notes:**

- A. CL includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.  
 Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All inputs pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_O = 50\Omega$ ,  $t_r \leq 2$  ns,  $t_f \leq 2$  ns.
- D. The outputs are measured one at a time with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{ten}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .