



## PI74ALVCH16374

### 16-Bit Edge Triggered D-Type Flip-Flop with 3-State Outputs

#### Product Features

- PI74ALVCH16374 is designed for low voltage operation
- $V_{CC} = 2.3V$  to  $3.6V$
- Hysteresis on all inputs
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8V$  at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $< 2.0V$  at  $V_{CC} = 3.3V$ ,  $T_A = 25^\circ C$
- Bus Hold retains last active bus state during 3-STATE eliminating the need for external pullup resistors
- Industrial operation at  $-40^\circ C$  to  $+85^\circ C$
- Packages available:
  - 48-pin 240 mil wide plastic TSSOP (A)
  - 48-pin 300 mil wide plastic SSOP (V)

#### Product Description

Pericom Semiconductor's PI74ALVCH series of logic circuits are produced in the Company's advanced 0.5 micron CMOS technology, achieving industry leading speed.

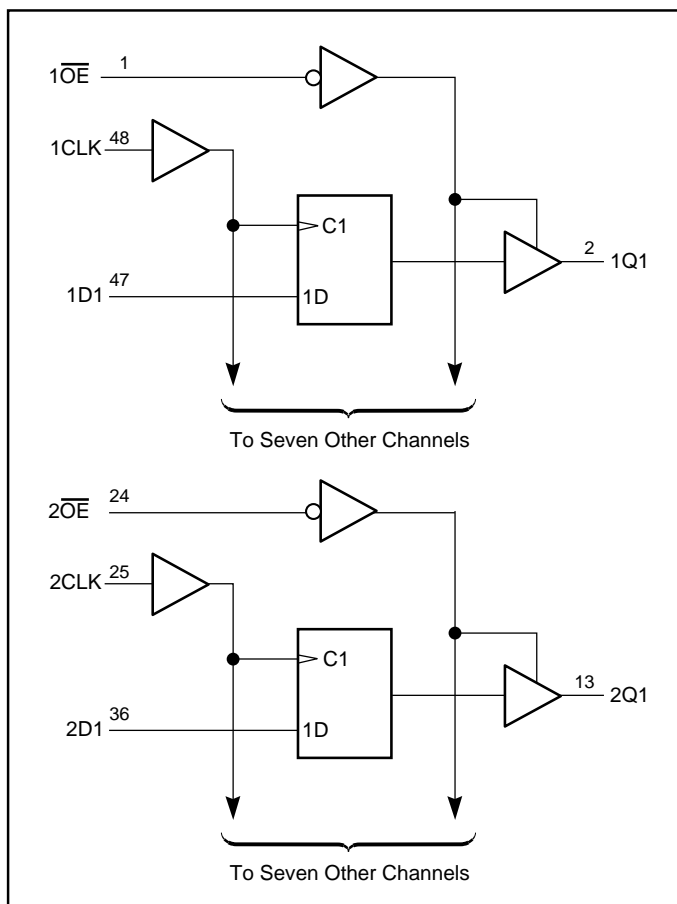
This 16-bit edge-triggered D-type flip-flop is designed for 2.3V to 3.6V  $V_{CC}$  operation.

The PI74ALVCH16374 is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. This device can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the Clock (CLK) input, the Q outputs of the flip-flop take on the logic levels set up at the data (D) inputs.  $\overline{OE}$  can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In that state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

#### Logic Block Diagram



### Product Pin Description

Pin Name	Description
$\overline{OE}$	Output Enable Input (Active LOW)
CLK	Clock Input (Active HIGH)
Dx	Data Inputs
Qx	3-State Outputs
GND	Ground
VCC	Power

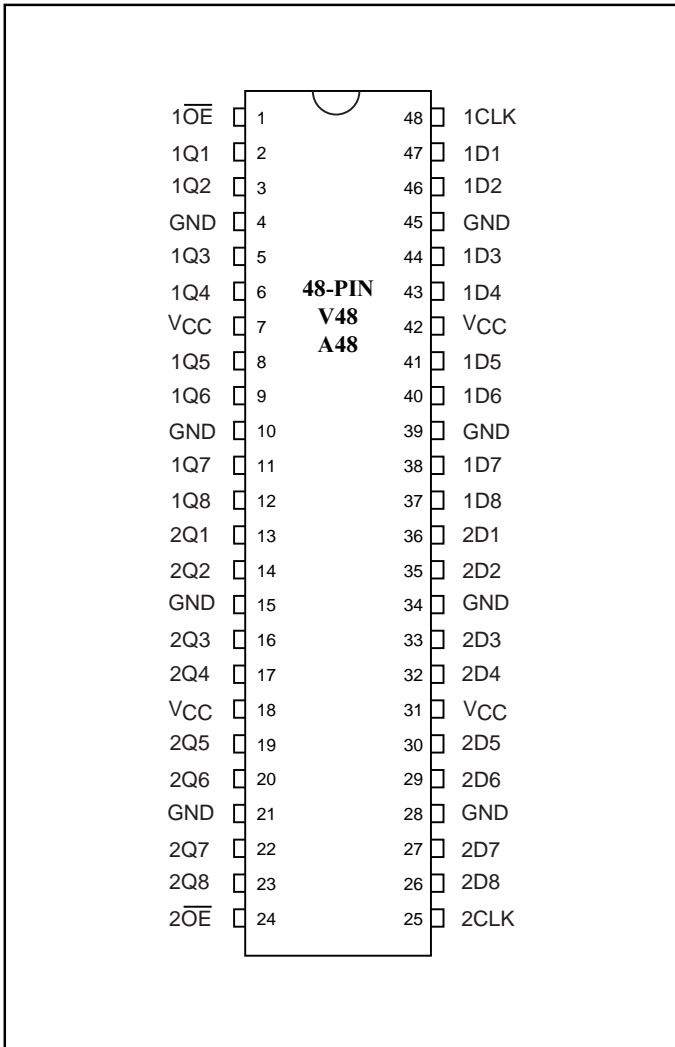
### Truth Table<sup>(1)</sup>

Inputs			Outputs
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q <sub>0</sub>
H	X	X	Z

#### Notes:

1. H = High Signal Level  
 L = Low Signal Level  
 X = Irrelevant  
 Z = High Impedance  
 ↑ = LOW to HIGH Transition  
 n = 1,2

### Product Pin Configuration





**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-65°C to +150°C
Ambient Temperature with Power Applied .....	-40°C to +85°C
Input Voltage Range, $V_{IN}$ .....	-0.5V to $V_{CC} + 0.5V$
Output Voltage Range, $V_{OUT}$ .....	-0.5V to $V_{CC} + 0.5V$
DC Input Voltage .....	-0.5V to +5.0V
DC Output Current .....	100 mA
Power Dissipation .....	1.0W

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Electrical Characteristics** (Over the Operating Range,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 3.3V \pm 10\%$ )

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units
$V_{CC}$	Supply Voltage		2.3		3.6	
$V_{IH}^{(3)}$	Input HIGH Voltage	$V_{CC} = 2.3V$ to $2.7V$	1.7			
		$V_{CC} = 2.7V$ to $3.6V$	2.0			
$V_{IL}^{(3)}$	Input LOW Voltage	$V_{CC} = 2.3V$ to $2.7V$			0.7	
		$V_{CC} = 2.7V$ to $3.6V$			0.8	
$V_{IN}^{(3)}$	Input Voltage		0		$V_{CC}$	
$V_{OUT}^{(3)}$	Output Voltage		0		$V_{CC}$	
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -100\mu A$ , $V_{CC} = \text{Min. to Max.}$	$V_{CC} - 0.2$			
		$V_{IH} = 1.7V$ , $I_{OH} = -6mA$ , $V_{CC} = 2.3V$	2.0			
		$V_{IH} = 1.7V$ , $I_{OH} = -12mA$ , $V_{CC} = 2.3V$	1.7			
		$V_{IH} = 2.0V$ , $I_{OH} = -12mA$ , $V_{CC} = 2.7V$	2.2			
		$V_{IH} = 2.0V$ , $I_{OH} = -12mA$ , $V_{CC} = 3.0V$	2.4			
		$V_{IH} = 2.0V$ , $I_{OH} = -24mA$ , $V_{CC} = 3.0V$	2.0			
$V_{OL}$	Output LOW Voltage	$I_{OL} = 100\mu A$ , $V_{IL} = \text{Min. to Max.}$			0.2	
		$V_{IL} = 0.7V$ , $I_{OL} = 6mA$ , $V_{CC} = 2.3V$			0.4	
		$V_{IL} = 0.7V$ , $I_{OL} = 12mA$ , $V_{CC} = 2.3V$			0.7	
		$V_{IL} = 0.8V$ , $I_{OL} = 12mA$ , $V_{CC} = 2.7V$			0.4	
		$V_{IL} = 0.8V$ , $I_{OL} = 24mA$ , $V_{CC} = 3.0V$			0.55	
$I_{OH}^{(3)}$	Output HIGH Current	$V_{CC} = 2.3V$			-12	mA
		$V_{CC} = 2.7V$			-12	
		$V_{CC} = 3.0V$			-24	
$I_{OL}^{(3)}$	Output LOW Current	$V_{CC} = 2.3V$			12	
		$V_{CC} = 2.7V$			12	
		$V_{CC} = 3.0V$			24	



**DC Electrical Characteristics-Continued** (Over the Operating Range,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 10\%$ )

Parameters	Description	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Units
$I_{IN}$	Input Current	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.6\text{V}$			$\pm 5$	$\mu\text{A}$
$I_{IN (HOLD)}$	Input Hold Current	$V_{IN} = 0.7\text{V}$ , $V_{CC} = 2.3\text{V}$	45			
		$V_{IN} = 1.7\text{V}$ , $V_{CC} = 2.3\text{V}$	-45			
		$V_{IN} = 0.8\text{V}$ , $V_{CC} = 3.0\text{V}$	75			
		$V_{IN} = 2.0\text{V}$ , $V_{CC} = 3.0\text{V}$	-75			
		$V_{IN} = 0$ to $3.6\text{V}$ , $V_{CC} = 3.6\text{V}$			$\pm 500$	
$I_{OZ}$	Output Current (3-STATE Outputs)	$V_{OUT} = V_{CC}$ or GND, $V_{CC} = 3.6\text{V}$			$\pm 10$	
$I_{CC}$	Supply Current	$V_{CC} = 3.6\text{V}$ , $I_{OUT} = 0\mu\text{A}$ , $V_{IN} = \text{GND}$ or $V_{CC}$			40	
$\Delta I_{CC}$	Supply Current per Input @ TTL HIGH	$V_{CC} = 3.0\text{V}$ to $3.6\text{V}$ One Input at $V_{CC} - 0.6\text{V}$ Other Inputs at $V_{CC}$ or GND			750	
$C_I$	Control Inputs	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 3.3\text{V}$		3		pF
	Data Inputs			6		
$C_O$	Outputs	$V_O = V_{CC}$ or GND, $V_{CC} = 3.3\text{V}$		7		

**Notes:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at  $V_{CC} = 3.3\text{V}$ ,  $+25^{\circ}\text{C}$  ambient and maximum loading.
3. Unused Control Inputs must be held HIGH or LOW to prevent them from floating.

**Timing Requirements over Operating Range**

Parameters	Description	$V_{CC} = 2.5\text{V} \pm 0.2\text{V}$		$V_{CC} = 2.7\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
$f_{\text{CLOCK}}$	Clock Frequency	0	150	0	150	0	150	MHz
$t_W$	Pulse Duration CLK HIGH or LOW	3.3		3.3		3.3		ns
$t_{SU}$	Setup Time Data Before CLK $\uparrow$	2.1		2.2		1.9		
$t_H$	Hold Time Data After CLK $\uparrow$	0.6		0.5		0.5		
$\Delta t/\Delta v^{(1)}$	Input Transition Rise or Fall							ns/V

**Note:**

1. Unused control inputs must be held HIGH or LOW to prevent them from floating.



**Switching Characteristics over Operating Range<sup>(1)</sup>**

Parameters	From (INPUT)	To (OUTPUT)	V <sub>CC</sub> = 2.5V ±0.2V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 3.3V ±0.3V		Units
			Min. <sup>(2)</sup>	Max.	Min.	Max.	Min. <sup>(2)</sup>	Max.	
f <sub>MAX</sub>			150		150		150		MHz
t <sub>PD</sub>	CLK	Q	1.0	5.3		4.9	1.0	4.2	ns
t <sub>EN</sub>	$\overline{\text{OE}}$		1.0	6.2		5.9	1.0	4.8	
t <sub>DIS</sub>	$\overline{\text{OE}}$		1.7	5.3		4.7	1.0	4.3	

**Notes:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.

**Operating Characteristics, T<sub>A</sub> = 25°C**

Parameter		Test Conditions	V <sub>CC</sub> = 2.5V ±0.2V	V <sub>CC</sub> = 3.3V ±0.3V	Units
			Typ.		
C <sub>PD</sub> Power Dissipation Capacitance	Outputs Enabled	C <sub>L</sub> = 50pF, f = 10 MHz	31	30	pF
	Outputs Disabled		16	18	