



**PI74FCT16841T
PI74FCT162841T**

**Fast CMOS 20-Bit
Transparent Latch**

Product Features:

Common Features:

- PI74FCT16841T and PI74FCT162841T are high-speed, low power devices with high current drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 300 mil wide plastic SSOP (V)

PI74FCT16841T Features:

- High output drive: $I_{OH} = -32\text{ mA}$; $I_{OL} = 64\text{ mA}$
- Power off disable outputs permit “live insertion”
- Typical VOLP (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162841T Features:

- Balanced output drivers: $\pm 24\text{ mA}$
- Reduced system switching noise
- Typical VOLP (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

Product Description:

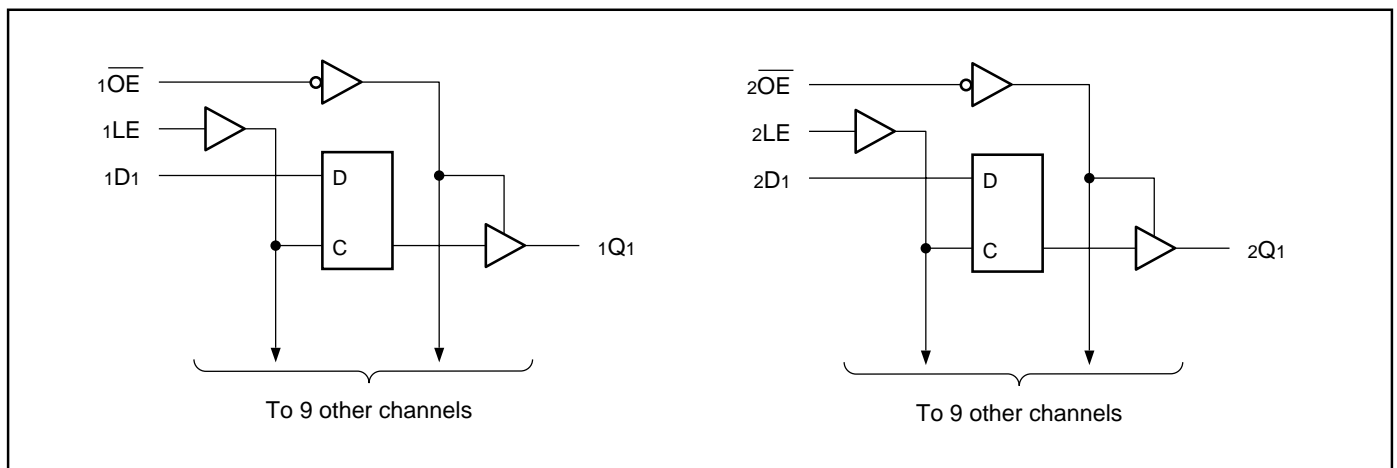
Pericom Semiconductor’s PI74FCT series of logic circuits are produced in the Company’s advanced 0.8 micron CMOS technology, achieving industry leading speed grades.

The PI74FCT16841T and PI74FCT162841T are 20-bit wide transparent latches designed to provide temporary storage of data and can be used as I/O ports, memory address latches, and bus drivers. The Output Enable and Latch Enable controls allow the devices to be operated as two 10-bit latches or one 20-bit latch. Signal pins are arranged in a flow-through organization for ease of layout and hysteresis is designed into all inputs to improve noise margin.

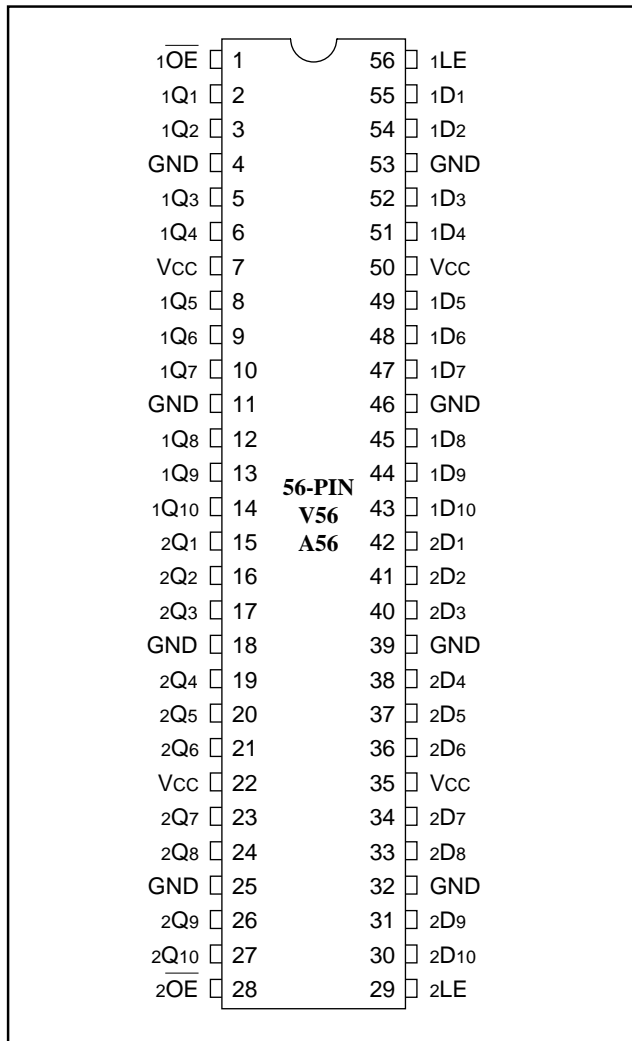
The output buffers on the PI74FCT16841T and PI74FCT162841T are especially designed for driving high-capacitance loads and low impedance backplanes and include a Power-Off Disable function allowing “live insertion” of boards when the devices are used as backplane drivers.

The PI74FCT162841T has $\pm 24\text{ mA}$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Logic Block Diagram



Product Configuration



Product Pin Description

Pin Name	Description
xD _x	Data Inputs
xLE	Latch Enable Input (Active LOW)
xOE	Output Enable Input (Active LOW)
xQ _x	3-State Outputs

Truth Table(1)

Inputs			Outputs
xD _x	xLE	xOE	xQ _x
H	H	L	H
L	H	L	L
X	L	L	Q ⁽²⁾
X	X	H	Z

1. H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance
2. Output level before xLE HIGH-to-LOW Transition.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = -40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IL}	Input LOW Current	V _{CC} = Max.	V _{IN} = GND			-1	μA
I _{OZH}	High Impedance	V _{CC} = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL}	Output Current	V _{CC} = Max.	V _{OUT} = 0.5V			-1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA			-0.7	-1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		-80	-140	-200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V		-50		-180	mA
V _H	Input Hysteresis				100		mV

PI74FCT16841T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3.0 mA	2.5	3.5		V
			I _{OH} = -15.0 mA	2.4	3.5		
			I _{OH} = -32.0 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 64 mA		0.2	0.55	V
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V		—	—	±100	μA

PI74FCT162841T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24.0 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} = Min., V _{IN} = V _{IH} or V _{IL}	I _{OL} = 24 mA		0.3	0.55	V
I _{ODL}	Output LOW Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		60	115	150	mA
I _{ODH}	Output HIGH Current	V _{CC} = 5V, V _{IN} = V _{IH} or V _{IL} , V _{OUT} = 1.5V ⁽³⁾		-60	-115	-150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	500	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	2.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open \overline{OE} = GND; LE = V _{CC} One Input Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.15	0.25	mA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle \overline{OE} = GND; LE = V _{CC} f _I = 5 MHz One Bit Toggling	V _{IN} = V _{CC} V _{IN} = GND		1.7	4.0 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		2.0	5.0 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz 50% Duty Cycle \overline{OE} = GND; LE = V _{CC} Eight Bits Toggling f _I = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.2	6.5 ⁽⁵⁾	
			V _{IN} = 3.4V V _{IN} = GND		5.2	14.5 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.

$$I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$$

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_I = Input Frequency

N_I = Number of Inputs at f_I

All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16841 Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	16841AT		16841BT		16841CT		16841DT		16841ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay xDx to xQx (LE = HIGH)	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	1.5	4.2	1.5	3.4	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	13.0	1.5	13.0	1.5	13.0	1.5	13.0	1.5	7.5	ns
tPLH tPHL	Propagation Delay xLE to xQx	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	1.5	4.0	1.5	3.7	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	1.5	8.0	1.5	7.5	ns
tPZH tPZL	Output Enable Time xOE to xQx	CL = 50 pF RL = 500Ω	1.5	11.5	1.5	8.0	1.5	6.5	1.5	4.8	1.5	4.4	ns
		CL = 300 pF ⁽⁴⁾ RL = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	1.5	9.0	1.5	9.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ xOE to xQx	CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	1.5	4.0	1.5	4.0	ns
		CL = 50 pF RL = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	1.5	5.4	1.5	4.0	ns
tsu	Setup Time HIGH or LOW, xDx to xLE	CL = 50 pF RL = 500Ω	2.5	—	2.5	—	2.5	—	1.0	—	1.0	—	ns
th	Hold Time HIGH or LOW, xDx to xLE		2.5	—	2.5	—	2.5	—	1.0	—	1.0	—	ns
tw	xLE Pulse Width HIGH ⁽³⁾		4.0	—	4.0	—	4.0	—	4.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT16841 Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	162841AT		162841BT		162841CT		162841DT		162841ET		Unit
			Com.		Com.		Com.		Com.		Com.		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
tPLH tPHL	Propagation Delay xDx to xQx (LE = HIGH)	CL = 50 pF RL = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	1.5	4.2	1.5	3.4	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	13.0	1.5	13.0	1.5	13.0	1.5	13.0	1.5	7.5	ns
tPLH tPHL	Propagation Delay xLE to xQx	CL = 50 pF RL = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	1.5	4.0	1.5	3.7	ns
		CL = 300 pF ⁽³⁾ RL = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	1.5	8.0	1.5	7.5	ns
tPZH tPZL	Output Enable Time xOE to xQx	CL = 50 pF RL = 500Ω	1.5	11.5	1.5	8.0	1.5	6.5	1.5	4.8	1.5	4.4	ns
		CL = 300 pF ⁽⁴⁾ RL = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	1.5	9.0	1.5	9.0	ns
tPHZ tPLZ	Output Disable Time ⁽³⁾ xOE to xQx	CL = 5 pF ⁽³⁾ RL = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	1.5	4.0	1.5	4.0	ns
		CL = 50 pF RL = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	1.5	5.4	1.5	4.0	ns
tsu	Setup Time HIGH or LOW, xDx to xLE	CL = 50 pF RL = 500Ω	2.5	—	2.5	—	2.5	—	1.0	—	1.0	—	ns
th	Hold Time HIGH or LOW, xDx to xLE		2.5	—	2.5	—	2.5	—	1.0	—	1.0	—	ns
tw	xLE Pulse Width HIGH ⁽³⁾		4.0	—	4.0	—	4.0	—	4.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.