PI74FCT841T/843T/845T
(25Ω Series) PI74FCT2841T

Fast CMOS
Bus Interface Latches

Product Features:

- PI74FCT841/843/845/2841T is pin compatible with bipolar FAST™ Series at a higher speed and lower power consumption
- 25Ω series resistor on all outputs (FCT2XXX only)
- TTL input and output levels
- Low ground bounce outputs
- Extremely low static power
- Hysteresis on all inputs
- Industrial operating temperature range: –40°C to +85°C
- Packages available:
  – 24-pin 300 mil wide plastic DIP (P)
  – 24-pin 150 mil wide plastic QSOP (Q)
  – 24-pin 150 mil wide plastic TQSOP (R)
  – 24-pin 300 mil wide plastic SOIC (S)

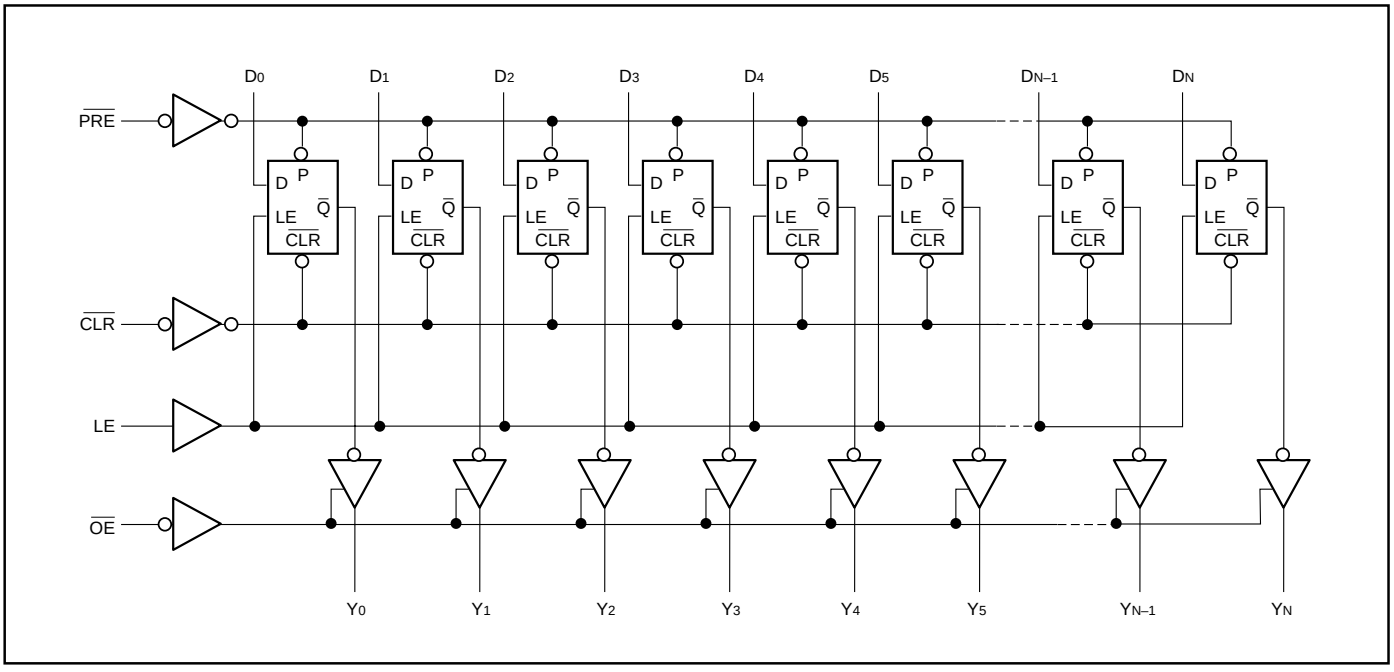
Product Description:

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.8 micron CMOS technology, achieving industry leading speed grades. All PI74FCT2XXX devices have a built-in 25-ohm series resistor on all outputs to reduce noise because of reflections, thus eliminating the need for an external terminating resistor.

The PI74FCT841T/843T/845T and P174FCT2841T series are buffered interface latches. These transparent latches designed with 3-state outputs and are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. When Latch Enable (LE) is HIGH, the flip-flops appear transparent to the data. The data that meets the set-up time when LE is LOW is latched. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

The PI74FCT841/2841T is a 10-bit latch, the PI74FCT843T is a 9-bit latch, and the PI74FCT845T is an 8-bit latch.

PI74FCT841/843/845/2842T Logic Block Diagram



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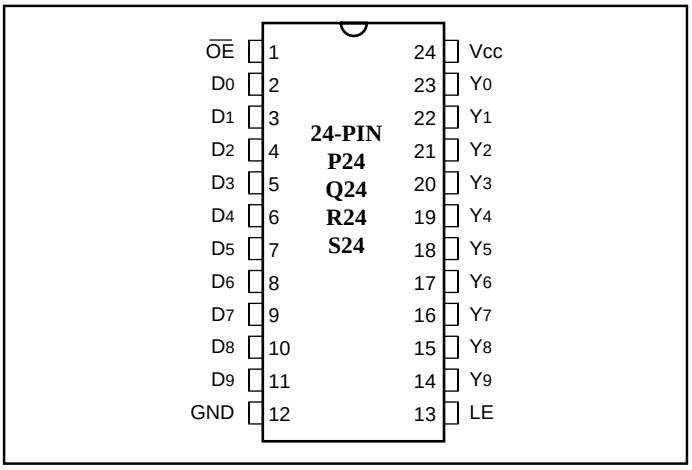
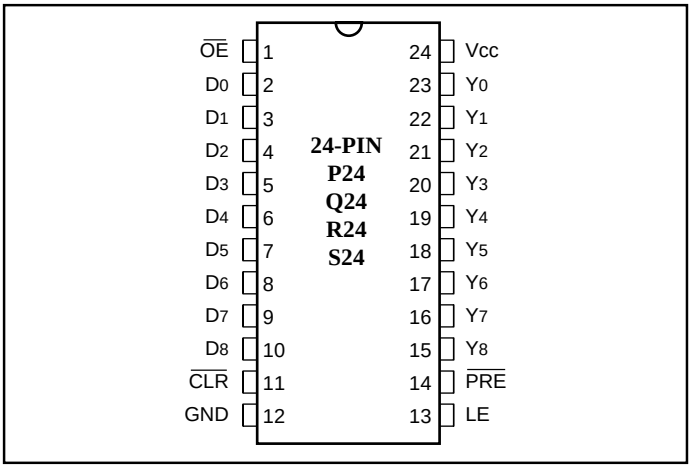
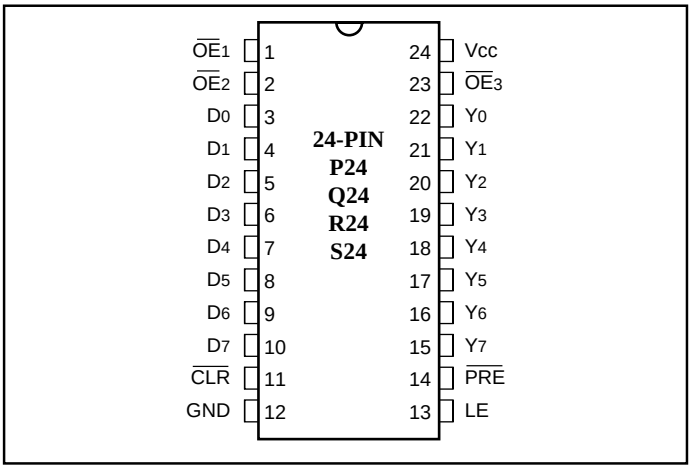
PI74FCT841/2841T 10-Bit Latch Product Configuration



PI74FCT843T 9-Bit Latch Product Configuration



PI74FCT845T 8-Bit Latch Product Configuration



Product Pin Description

Pin Name	Description
Y_N	3-State Latch Outputs
D_N	Latch Data Inputs
LE	Latch Enable Input
$\overline{OE}$	Output Enable Control
$\overline{CLR}$	Clear Latch
$\overline{PRE}$	Preset Latch High, Preset Overrides CLR
GND	Ground
V_{CC}	Power

Truth Table[1]

Function	Inputs					Outputs	Internal
	$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_N	Y_N	Q_N
High-Z	H	H	H	X	X	Z	X
	H	H	H	H	L	Z	L
	H	H	H	H	H	Z	H
Latched (High Z)	H	H	H	L	X	Z	NC
Transparent	H	H	L	H	L	L	L
	H	H	L	H	H	H	H
Latched	H	H	L	L	X	NC	NC
Preset	H	L	L	X	X	H	H
Clear	L	H	L	X	X	L	L
Preset	L	L	L	X	X	H	H
Latched (High Z)	L	H	H	L	X	Z	L
Latched (High Z)	H	L	H	L	X	Z	H

1. H = High Voltage Level
   L = Low Voltage Level
   X = Don't Care
   NC = No Change
   Z = High Impedance

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	0.5W

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 5%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15.0 mA	2.4	3.0		V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 48 mA		0.3	0.50	V
V_{OL}	Output LOW Current	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12 mA (25Ω Series)		0.3	0.50	V
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	V_{CC} = Max.	V_{IN} = V_{CC}			1	µA
I_{IL}	Input LOW Current	V_{CC} = Max.	V_{IN} = GND			–1	µA
I_{OZH}	High Impedance	V_{CC} = Max.	V_{OUT} = 2.7V			1	µA
I_{OZL}	Output Current		V_{OUT} = 0.5V			–1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OFF}	Power Down Disable	V_{CC} = GND, V_{OUT} = 4.5V		—	—	100	µA
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–60	–120		mA
V_H	Input Hysteresis				200		mV

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	µA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	2.0	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $\overline{OE}$ = GND; LE = Vcc One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{OE}$ = GND; LE = Vcc f_I = 5 MHz One Bit Toggling	V_{IN} = V_{CC} V_{IN} = GND		1.5	3.5[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		1.8	4.5[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $\overline{OE}$ = GND; LE = Vcc Eight Bits Toggling f_I = 2.5 MHz 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND		3.0	6.0[5]	
			V_{IN} = 3.4V V_{IN} = GND		5.0	14.0[5]	

Notes:
1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

PI74FCT841/2841T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	841AT/2841AT Com. Min	841AT/2841AT Com. Max	841BT/2841BT Com. Min	841BT/2841BT Com. Max	841CT/2841CT Com. Min	841CT/2841CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to Y_N (LE = HIGH)	C_L = 50 pF R_L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C_L = 300 pF[3] R_L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
t_{SU}	Setup Time Data to LE	C_L = 50 pF R_L = 500Ω	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time Data to LE		2.5	—	2.5	—	2.5	—	ns
t_{PLH} t_{PHL}	Propagation Delay LE to Y_N	C_L = 50 pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C_L = 300 pF[3] R_L = 500Ω	—	16.0	—	15.5	—	15.0	ns
t_W	LE Pulse Width[3] (HIGH)	C_L = 50 pF R_L = 500Ω	4.0	—	4.0	—	4.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_N	C_L = 50 pF R_L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C_L = 300 pF[3] R_L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OE}$ to Y_N	C_L = 50 pF R_L = 500Ω	1.5	7.0	1.5	6.0	1.5	5.7	ns
		C_L = 5 pF[3] R_L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT843T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	843AT Com. Min	843AT Com. Max	843BT Com. Min	843BT Com. Max	843CT Com. Min	843CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to Y_N (LE = HIGH)	C_L = 50 pF R_L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C_L = 300 pF[3] R_L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
t_{SU}	Setup Time Data to LE	C_L = 50 pF R_L = 500Ω	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time Data to LE		2.5	—	2.5	—	2.5	—	ns
t_{PLH} t_{PHL}	Propagation Delay LE to Y_N	C_L = 50 pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C_L = 300 pF[3] R_L = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	ns
t_{PLH}	Propagation Delay $\overline{PRE}$ to Y_N	C_L = 50 pF R_L = 500Ω	1.5	11.0	1.5	8.0	1.5	7.0	ns
t_{REM}	Recovery Time $\overline{PRE}$ to Y_N		1.5	11.0	1.5	10.0	1.5	9.0	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to Y_N		1.5	11.0	1.5	10.0	1.5	9.0	ns
t_{REM}	Recovery Time[3] $\overline{CLR}$ to Y_N		1.5	13.0	1.5	10.0	1.5	9.0	ns
t_W	LE Pulse Width[3] (HIGH)		4.0	—	4.0	—	4.0	—	ns
t_W	$\overline{PRE}$ Pulse Width[3] (LOW)		5.0	—	4.0	—	4.0	—	ns
t_W	$\overline{CLR}$ Pulse Width[3] (LOW)		4.0	—	4.0	—	4.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_N	C_L = 50 pF R_L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C_L = 300 pF[3] R_L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OE}$ to Y_N	C_L = 50 pF R_L = 500Ω	1.5	7.0	1.5	6.5	1.5	5.7	ns
		C_L = 5 pF[3] R_L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.

PI74FCT845T Switching Characteristics over Operating Range

Parameters	Description	Conditions[1]	845AT Com. Min	845AT Com. Max	845BT Com. Min	845BT Com. Max	845CT Com. Min	845CT Com. Max	Unit
t_{PLH} t_{PHL}	Propagation Delay D_N to Y_N (LE = HIGH)	C_L = 50 pF R_L = 500Ω	1.5	9.0	1.5	6.5	1.5	5.5	ns
		C_L = 300 pF[3] R_L = 500Ω	1.5	8.0	1.5	13.0	1.5	13.0	ns
t_{SU}	Setup Time Data to LE	C_L = 50 pF R_L = 500Ω	2.5	—	2.5	—	2.5	—	ns
t_H	Hold Time Data to LE		2.5	—	2.5	—	2.5	—	ns
t_{PLH} t_{PHL}	Propagation Delay LE to Y_N	C_L = 50 pF R_L = 500Ω	1.5	12.0	1.5	8.0	1.5	6.4	ns
		C_L = 300 pF[3] R_L = 500Ω	1.5	16.0	1.5	15.5	1.5	15.0	ns
t_{PLH}	Propagation Delay $\overline{PRE}$ to Y_N	C_L = 50 pF R_L = 500Ω	1.5	11.0	1.5	8.0	1.5	7.0	ns
t_{REM}	Recovery Time[3] $\overline{PRE}$ to Y_N		1.5	11.0	1.5	10.0	1.5	9.0	ns
t_{PLH}	Propagation Delay $\overline{CLR}$ to Y_N		1.5	11.0	1.5	10.0	1.5	9.0	ns
t_{REM}	Recovery Time[3] $\overline{CLR}$ to Y_N		1.5	13.0	1.5	10.0	1.5	9.0	ns
t_W	LE Pulse Width[3] (HIGH)		4.0	—	4.0	—	4.0	—	ns
t_W	$\overline{PRE}$ Pulse Width[3] (LOW)		5.0	—	4.0	—	4.0	—	ns
t_W	$\overline{CLR}$ Pulse Width[3] (LOW)		4.0	—	4.0	—	4.0	—	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_N	C_L = 50 pF R_L = 500Ω	1.5	10.0	1.5	8.0	1.5	6.5	ns
		C_L = 300 pF[3] R_L = 500Ω	1.5	23.0	1.5	14.0	1.5	12.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] $\overline{OE}$ to Y_N	C_L = 50 pF R_L = 500Ω	1.5	7.0	1.5	6.5	1.5	5.7	ns
		C_L = 5 pF[3] R_L = 500Ω	1.5	8.0	1.5	7.0	1.5	6.0	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.