



**PI74LPT16374**

**Fast CMOS 3.3V  
16-Bit Register (3-State)**

**Product Features**

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
  - Input can be 3V or 5V
  - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:  
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- ESD Protection exceeds 2000V
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
  - 48-pin 240 mil wide plastic TSSOP (A)
  - 48-pin 300 mil wide plastic SSOP (V)

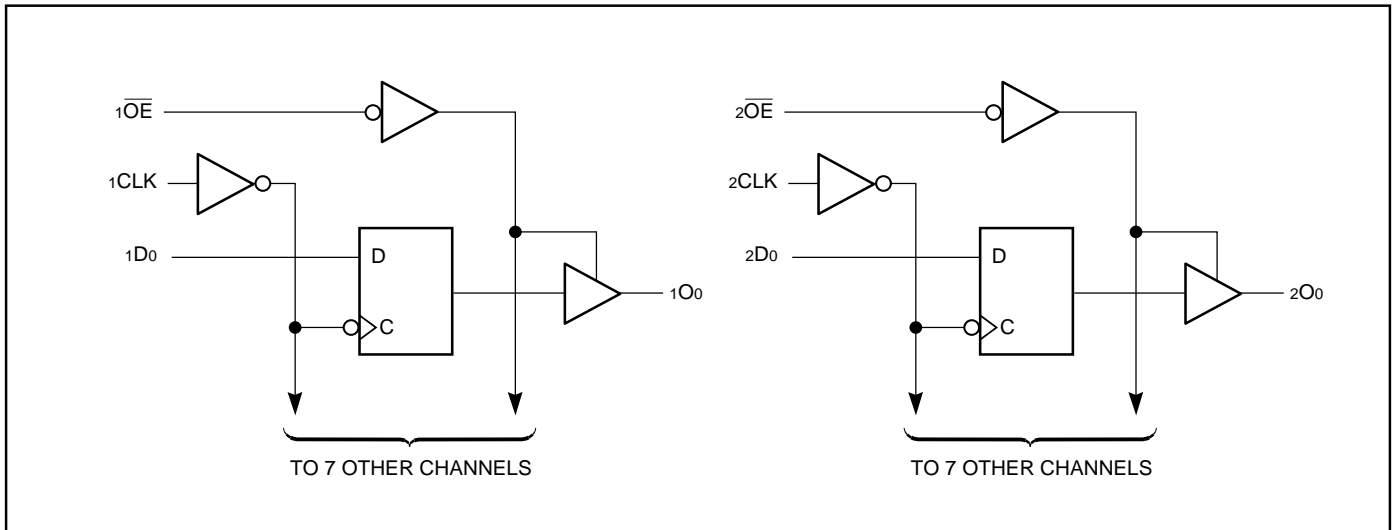
**Product Description**

Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16374 is a 16-bit octal register designed with 16 D-type flip-flops with a buffered common clock and 3-state outputs. The Output Enable ( $\overline{xOE}$ ) and clock ( $xCLK$ ) controls are organized to operate as two 8-bit registers or one 16-bit register. When  $\overline{OE}$  is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

The PI74LPT16374 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3/5.0V system.

**Logic Block Diagram**



### Product Pin Description

Pin Name	Description
$\overline{xOE}$	3-State Output Enable Inputs (Active LOW)
xCLK	Clock Inputs
xDx	Data Inputs
xOx	3-State Outputs
GND	Ground
Vcc	Power

### Truth Table

Function	Inputs <sup>(1)</sup>			Outputs <sup>(1)</sup>
	xDx	xCLK	$\overline{xOE}$	xOx
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L		L	L
	H		L	H
	L		H	Z
	H		H	Z

### Product Pin Configuration

$\overline{1OE}$	□	1		48	□	1CLK
$1O_0$	□	2		47	□	$1D_0$
$1O_1$	□	3		46	□	$1D_1$
GND	□	4		45	□	GND
$1O_2$	□	5		44	□	$1D_2$
$1O_3$	□	6		43	□	$1D_3$
Vcc	□	7		42	□	Vcc
$1O_4$	□	8		41	□	$1D_4$
$1O_5$	□	9		40	□	$1D_5$
GND	□	10		39	□	GND
$1O_6$	□	11	<b>48-PIN V48 A48</b>	38	□	$1D_6$
$1O_7$	□	12		37	□	$1D_7$
$2O_0$	□	13		36	□	$2D_0$
$2O_1$	□	14		35	□	$2D_1$
GND	□	15		34	□	GND
$2O_2$	□	16		33	□	$2D_2$
$2O_3$	□	17		32	□	$2D_3$
Vcc	□	18		31	□	Vcc
$2O_4$	□	19		30	□	$2D_4$
$2O_5$	□	20		29	□	$2D_5$
GND	□	21		28	□	GND
$2O_6$	□	22		27	□	$2D_6$
$2O_7$	□	23		26	□	$2D_7$
$2OE$	□	24		25	□	$2CLK$

### Note:

- H = High Voltage Level, X = Don't Care,  
L = Low Voltage Level, Z = High Impedance

### Capacitance ( $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ )

Parameters <sup>(1)</sup>	Description	Test Conditions	Typ.	Max.	Units
$C_{IN}$	Input Capacitance	$V_{IN} = 0V$	4.5	6	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 0V$	5.5	8	pF

### Note:

- This parameter is determined by device characterization but is not production tested.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....	-55°C to +125°C
Ambient Temperature with Power Applied .....	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only) .....	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) ...	-0.5V to +7.0V
DC Input Voltage .....	-0.5V to +7.0V
DC Output Current .....	120 mA
Power Dissipation .....	1.0W

**Note:**

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**DC Electrical Characteristics** (Over the Operating Range,  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 2.7\text{V}$  to  $3.6\text{V}$ )

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
V <sub>IH</sub>	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	5.5	V
V <sub>IL</sub>	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I <sub>IH</sub>	Input HIGH Current (Input pins)	V <sub>CC</sub> = Max.	V <sub>IN</sub> = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	V <sub>CC</sub> = Max.	V <sub>IN</sub> = V <sub>CC</sub>	—	—	±1	µA
I <sub>IL</sub>	Input LOW Current (Input pins)	V <sub>CC</sub> = Max.	V <sub>IN</sub> = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	V <sub>CC</sub> = Max.	V <sub>IN</sub> = GND	—	—	±1	µA
I <sub>OZH</sub>	High Impedance Output Current (3-State Output pins)	V <sub>CC</sub> = Max.	V <sub>OUT</sub> = 5.5V	—	—	±1	µA
I <sub>OZL</sub>		V <sub>CC</sub> = Max.	V <sub>OUT</sub> = GND	—	—	±1	µA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18 mA		—	-0.7	-1.2	V
I <sub>ODH</sub>	Output HIGH Current	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = 1.5V <sup>(3)</sup>		-36	-60	-110	mA
I <sub>ODL</sub>	Output LOW Current	V <sub>CC</sub> = 3.3V, V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub> , V <sub>O</sub> = 1.5V <sup>(3)</sup>		50	90	200	mA
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min.	I <sub>OH</sub> = -0.1 mA	V <sub>CC</sub> -0.2	—	—	V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -3 mA	2.4	3.0	—	V
		V <sub>CC</sub> = 3.0V,	I <sub>OH</sub> = -8 mA	2.4 <sup>(5)</sup>	3.0	—	V
		V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -24 mA	2.0	—	—	V
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min.	I <sub>OL</sub> = 0.1 mA	—	—	0.2	V
			I <sub>OL</sub> = 16 mA	—	0.2	0.4	V
			I <sub>OL</sub> = 24 mA	—	0.3	0.5	V
I <sub>OS</sub>	Short Circuit Current <sup>(4)</sup>	V <sub>CC</sub> = Max. <sup>(3)</sup> , V <sub>OUT</sub> = GND		-60	-85	-240	mA
I <sub>OFF</sub>	Power Down Disable	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>OUT</sub> ≤ 4.5V		—	—	±100	µA
V <sub>H</sub>	Input Hysteresis			—	150	—	mV

**Notes:**

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V<sub>OH</sub> = V<sub>CC</sub> - 0.6V at rated current.

**Power Supply Characteristics**

Parameters	Description	Test Conditions <sup>(1)</sup>		Min.	Typ <sup>(2)</sup>	Max.	Units
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max.	V <sub>IN</sub> = GND or V <sub>CC</sub>		0.1	10	μA
ΔI <sub>CC</sub>	Quiescent Power Supply Current TTL Inputs HIGH	V <sub>CC</sub> = Max.	V <sub>IN</sub> = V <sub>CC</sub> - 0.6V <sup>(3)</sup>		2.0	30	μA
I <sub>CCD</sub>	Dynamic Power Supply <sup>(4)</sup>	V <sub>CC</sub> = Max., Outputs Open x $\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	V <sub>IN</sub> = V <sub>CC</sub> V <sub>IN</sub> = GND		50	75	μA/ MHz
I <sub>C</sub>	Total Power Supply Current <sup>(6)</sup>	V <sub>CC</sub> = Max., Outputs Open f <sub>i</sub> = 10 MHz 50% Duty Cycle x $\overline{OE}$ = GND One Bit Toggling	V <sub>IN</sub> = V <sub>CC</sub> - 0.6V V <sub>IN</sub> = GND		0.6	2.3	mA
		V <sub>CC</sub> = Max., Outputs Open f <sub>i</sub> = 2.5 MHz 50% Duty Cycle x $\overline{OE}$ = GND 16 Bits Toggling	V <sub>IN</sub> = V <sub>CC</sub> - 0.6V V <sub>IN</sub> = GND		2.1	4.7 <sup>(5)</sup>	

**Notes:**

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V<sub>CC</sub> = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V<sub>CC</sub> or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
- I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current (I<sub>CC1</sub>, I<sub>CC2</sub> and I<sub>CCZ</sub>)  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 N<sub>CP</sub> = Number of Clock Inputs at f<sub>CP</sub>  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.

**Switching Characteristics over Operating Range<sup>(1)</sup>**

Parameters	Description	Conditions <sup>(2)</sup>	LPT16374		LPT16374A		LPT16374C		Units
			Com.		Com.		Com.		
			Min. <sup>(3)</sup>	Max.	Min. <sup>(3)</sup>	Max.	Min. <sup>(3)</sup>	Max.	
tPLH tPHL	Propagation Delay xCLK to xOx	CL = 50 pF RL = 500Ω	2.0	7.0	2.0	6.5	2.0	5.2	ns
tpZH tpZL	Output Enable Time xOE to xOx		1.5	7.2	1.5	6.5	1.5	5.5	ns
tpHZ tPLZ	Output Disable Time <sup>(4)</sup> xOE to xOx		1.5	7.2	1.5	5.5	1.5	5.0	ns
tsu	Setup Time HIGH or LOW, xDx to xCLK		2.0		2.0		2.0		ns
th	Hold Time HIGH or LOW, xDx to xCLK		1.5		1.5		1.5		ns
tw	xCLK Pulse Width <sup>(4)</sup> HIGH		7.0		5.0		5.0		ns
tsk(o)	Output Skew <sup>(5)</sup>			0.5		0.5		0.5	ns

**Notes:**

1. Propagation Delays and Enable/Disable times are with Vcc = 3.3V ±0.3V, normal range. For Vcc = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.