

Fast CMOS 18-Bit Registered Transceivers

Product Features

- Compatible with LCX™ and LVT™ families of products
- Supports 5V Tolerant Mixed Signal Mode Operation
 - Input can be 3V or 5V
 - Output can be 3V or connected to 5V bus
- Advanced Low Power CMOS Operation
- Excellent output drive capability:
Balanced drives (24 mA sink and source)
- Pin compatible with industry standard double-density pinouts
- Low ground bounce outputs
- Hysteresis on all inputs
- Industrial operating temperature range: -40°C to +85°C
- Multiple center pins and distributed Vcc/GND pins minimize switching noise
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 300 mil wide plastic SSOP (V)

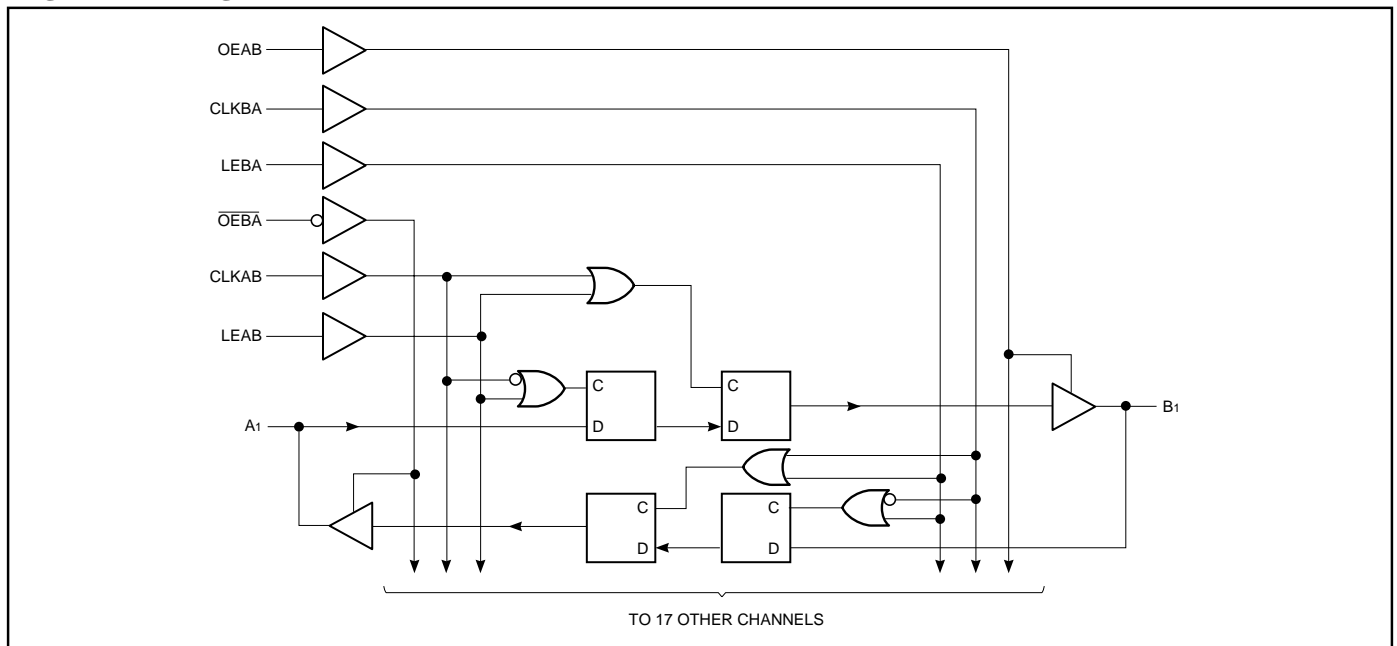
Product Description

Pericom Semiconductor's PI74LPT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

The PI74LPT16501 is an 18-bit registered bus transceiver designed with D-type latches and flip-flops to allow data flow in transparent, latched, and clocked modes. The Output Enable (OEAB and OEBA, Latch Enable (LEAB and LEBA) and Clock (CLKAB and CLKBA) inputs control the data flow in each direction. When LEAB is HIGH, the device operates in transparent mode for A-to-B data flow. When LEAB is LOW, the A data is latched if CLKAB is held at a HIGH or LOW logic level. The A bus data is stored in the latch/flip-flop on the LOW-to-HIGH transition of CLKAB, if LEAB is LOW. OEAB performs the output enable function on the B port. Data flow from B port to A port is similar using OEBA, LEBA and CLKBA. This high-speed, low power device offers a flow-through organization for ease of board layout.

The PI74LPT16501 can be driven from either 3.3V or 5.0V devices allowing this device to be used as a translator in a mixed 3.3V/5.0V system.

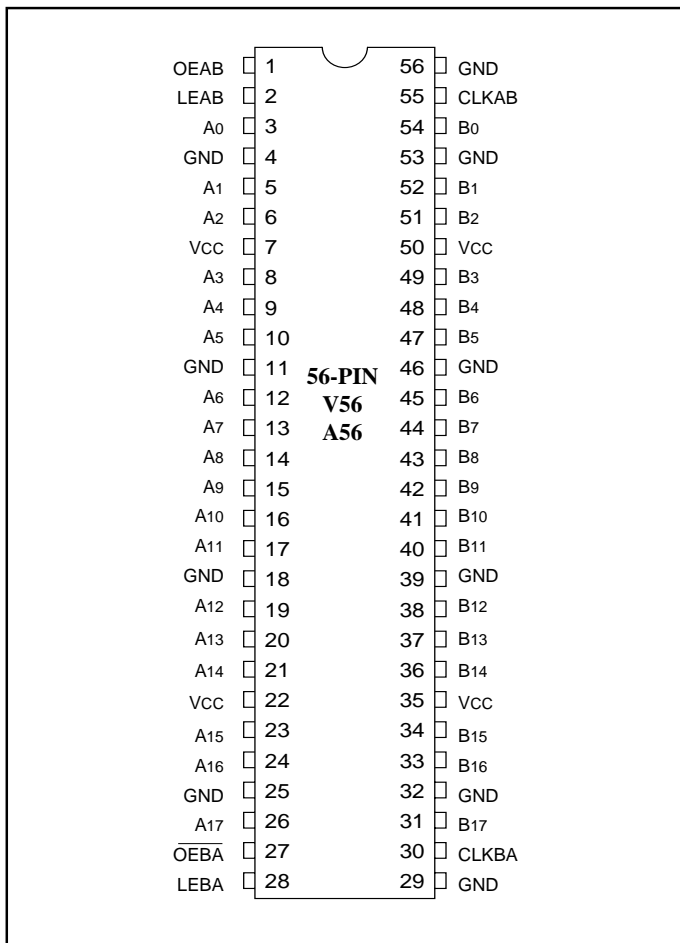
Logic Block Diagram



Product Pin Description

Pin Name	Description
OEAB	A-to-B Output Enable Input
$\overline{\text{OEBA}}$	B-to-A Output Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input
LEBA	B-to-A Latch Enable Input
CLKAB	A-to-B Clock Input
CLKBA	B-to-A Clock Input
A _x	A-to-B Data Inputs or B-to-A 3-State Outputs
B _x	B-to-A Data Inputs or A-to-B 3-State Outputs
GND	Ground
V _{CC}	Power

Product Pin Configuration



Truth Table^(1,4)

Inputs				Outputs
OEAB	LEAB	CLKAB	A _x	B _x
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↑	L	L
H	L	↑	H	H
H	L	L	X	B ⁽²⁾
H	L	H	X	B ⁽³⁾

Notes:

1. A-to-B data flow is shown. B-to-A data flow is similar but uses $\overline{\text{OEBA}}$, LEBA, and CLKBA.
2. Output level before the indicated steady-state input conditions were established.
3. Output level before the indicated steady-state input conditions were established, provided that CLKAB was HIGH before LEAB went LOW.
4. H = High Voltage Level
L = Low Voltage Level
Z = High Impedance
↑ = LOW-to-HIGH Transition

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Inputs & Vcc Only)	-0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only) ..	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Current	120 mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 2.7\text{V}$ to 3.6V)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage (Input pins)	Guaranteed Logic HIGH Level		2.2	—	5.5	V
	Input HIGH Voltage (I/O pins)			2.0	—	5.5	V
V _{IL}	Input LOW Voltage (Input and I/O pins)	Guaranteed Logic LOW Level		-0.5	—	0.8	V
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max.	V _{IN} = 5.5V	—	—	±1	µA
	Input HIGH Current (I/O pins)	V _{CC} = Max.	V _{IN} = V _{CC}	—	—	±1	µA
I _{IL}	Input LOW Current (Input pins)	V _{CC} = Max.	V _{IN} = GND	—	—	±1	µA
	Input LOW Current (I/O pins)	V _{CC} = Max.	V _{IN} = GND	—	—	±1	µA
I _{OZH}	High Impedance Output Current (3-State Output pins)	V _{CC} = Max.	V _{OUT} = 5.5V	—	—	±1	µA
I _{OZL}		V _{CC} = Max.	V _{OUT} = GND	—	—	±1	µA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18 mA		—	-0.7	-1.2	V
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾		-36	-60	-110	mA
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾		50	90	200	mA
V _{OH}	Output HIGH Voltage	V _{CC} = Min.	I _{OH} = -0.1 mA	V _{CC} -0.2	—	—	V
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = -3 mA	2.4	3.0	—	V
		V _{CC} = 3.0V,	I _{OH} = -8 mA	2.4 ⁽⁵⁾	3.0	—	V
		V _{IN} = V _{IH} or V _{IL}	I _{OH} = -24 mA	2.0	—	—	
V _{OL}	Output LOW Voltage	V _{CC} = Min.	I _{OL} = 0.1 mA	—	—	0.2	V
			I _{OL} = 16 mA	—	0.2	0.4	V
			I _{OL} = 24 mA	—	0.3	0.5	V
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		-60	-85	-240	mA
I _{OFF}	Power Down Disable	V _{CC} = 0V, V _{IN} or V _{OUT} ≤ 4.5V		—	—	±100	µA
V _H	Input Hysteresis			—	150	—	mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.1	10	μA
ΔI _{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max.	V _{IN} = V _{CC} - 0.6V ⁽³⁾		2.0	30	μA
I _{CCD}	Dynamic Power Supply ⁽⁴⁾	V _{CC} = Max., Outputs Open x \overline{OE} = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		50	75	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _i = 10 MHz 50% Duty Cycle x \overline{OE} = GND One Bit Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		0.6	2.3	mA
		V _{CC} = Max., Outputs Open f _i = 2.5 MHz 50% Duty Cycle x \overline{OE} = GND 16 Bits Toggling	V _{IN} = V _{CC} - 0.6V V _{IN} = GND		2.1	4.7 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input; all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CCZ})
 ΔI_{CC} = Power Supply Current for a TTL High Input
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
 N_{CP} = Number of Clock Inputs at f_{CP}
 f_i = Input Frequency
 N_i = Number of Inputs at f_i
 All currents are in milliamperes and all frequencies are in megahertz.

PI74LPT16501 Switching Characteristics over Operating Range⁽¹⁾

Parameters	Description	Conditions ⁽²⁾	LPT16501		LPT16501A		LPT16501C		Unit	
			Com.		Com.		Com. Preliminary			
			Min ⁽³⁾	Max	Min ⁽³⁾	Max	Min ⁽³⁾	Max		
t _{MAX}	CLKAB or CLKBA frequency	C _L = 50 pF R _L = 500 Ω	—	100	—	150	—	150	MHz	
t _{PLH} t _{PHL}	Propagation Delay Ax to Bx or Ax to Bx		1.5	6.5	1.5	5.1	1.5	4.6	ns	
t _{PLH} t _{PHL}	Propagation Delay LEBA to Ax, LEAB to Bx		1.5	7.5	1.5	5.6	1.5	5.3	ns	
t _{PLH} t _{PHL}	Propagation Delay CLKBA to Ax, CLKAB to Bx		1.5	8.0	1.5	5.6	1.5	5.3	ns	
t _{PZH} t _{PZL}	Output Enable Time OEBA to Ax, OEAB to Bx		1.5	8.0	1.5	6.0	1.5	5.6	ns	
t _{PHZ} t _{PLZ}	Output Disable Time ⁽⁴⁾ OEBA to Ax, OEAB to Bx		1.5	7.5	1.5	5.6	1.5	5.2	ns	
t _{SU}	Setup Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		4.0	—	3.0	—	3.0	—	ns	
t _H	Hold Time HIGH or LOW Ax to CLKAB, Bx to CLKBA		0	—	0	—	0	—	ns	
t _{SU}	Setup Time HIGH or LOW Ax to LEAB, Bx to LEBA		Clock HIGH	4.0	—	3.0	—	3.0	—	ns
			Clock LOW	1.5	—	1.5	—	1.5	—	ns
t _H	Hold Time HIGH or LOW Ax to LEAB, Bx to LEBA		1.5	—	1.5	—	1.5	—	ns	
t _w	LEAB or LEBA Pulse Width HIGH ⁽⁴⁾		3.0	—	3.0	—	3.0	—	ns	
t _w	CLKAB or CLKBA Pulse Width HIGH or LOW ⁽⁴⁾	3.0	—	3.0	—	3.0	—	ns		
t _{SK(O)}	Output Skew ⁽⁵⁾	—	0.5	—	0.5	—	0.5	ns		

Notes:

1. Propagation Delays and Enable/Disable times are with V_{CC} = 3.3V ±0.3V, normal range. For V_{CC} = 2.7V, extended range, all Propagation Delays and Enable/Disable times should be degraded by 20%.
2. See test circuit and waveforms.
3. Minimum limits are guaranteed but not tested on Propagation Delays.
4. This parameter is guaranteed but not production tested.
5. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters ⁽¹⁾	Description	Test Conditions	Typ.	Max.	Units
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

Note:

1. This parameter is determined by device characterization but is not production tested.

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