LVDS Dual 2x2 Crosspoint/Repeater Switch

Features

- Dual 2x2 Crosspoint/Repeater Switch
- Meets or Exceeds the Requirements of ANSI TIA/ EIA-644-1995
- Designed for Signaling Rates up to 650 Mbit/s (325 MHz)
- Operates from a 3.3V Supply: –40°C to 85°C
- Low Voltage Differential Signaling with Output Voltages of ±350mV into:
  – 100 Ohm load (PI90LV024)
  –50 Ohm load Bus LVDS Signaling (PI90LVB024)
- Accepts ±350mV differential inputs
- Wide common mode input range: 0.2V to 2.7V
- Output drivers are high impedance when disabled or when $V_{CC} \leq 1.5V$
- Inputs are open, short, and terminated fail safe
- Propagation Delay Time: 3.5ns
- ESD protection is 10kV on bus pins
- Bus Pins are High Impedance when disabled or with V_{CC} less than 1.5V
- TTL Inputs are 5V Tolerant
- Power Dissipation at 400Mbit/s of 250mW
- Available Packaging: 28-pin QSOP, 28-pin TSSOP

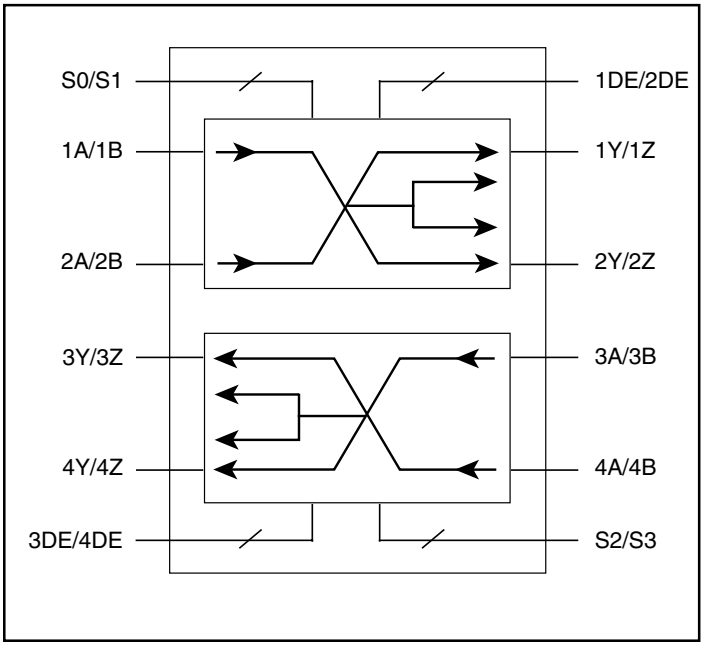
Description

The PI90LV024 and PI90LVB024 are monolithic dual 2x2 asynchronous crosspoint/repeater switches. The crosspoint function is based on a multiplexer tree architecture. Each 2x2 switch can be considered as a pair of 2:1 multiplexers that share the same inputs. The signal path through each switch is fully differential with minimal propagation delay. The signal path is unregistered, so no clock is required for the data inputs. The signal line drivers and receivers use Low Voltage Differential Signaling (LVDS) to achieve signaling rates as high as 650 Mbps.

The LVDS standard provides a minimum differential output voltage magnitude of 247mV into a 100 Ohm load and receipt of 100mV signals with up to 1V of ground potential difference between a transmitter and receiver. The PI90LVB024 doubles the output drive current to achieve Bus LVDS signaling levels with a 50 Ohm load.

The intended application of these devices is for loop-through and redundant channel switching for both point-to-point base-band (PI90LV024) and multipoint (PI90LVB024) data transmissions over controlled impedance media. The package pin assignments enables easy routing for applications requiring signal feedback.

Block Diagram



Pin Configuration

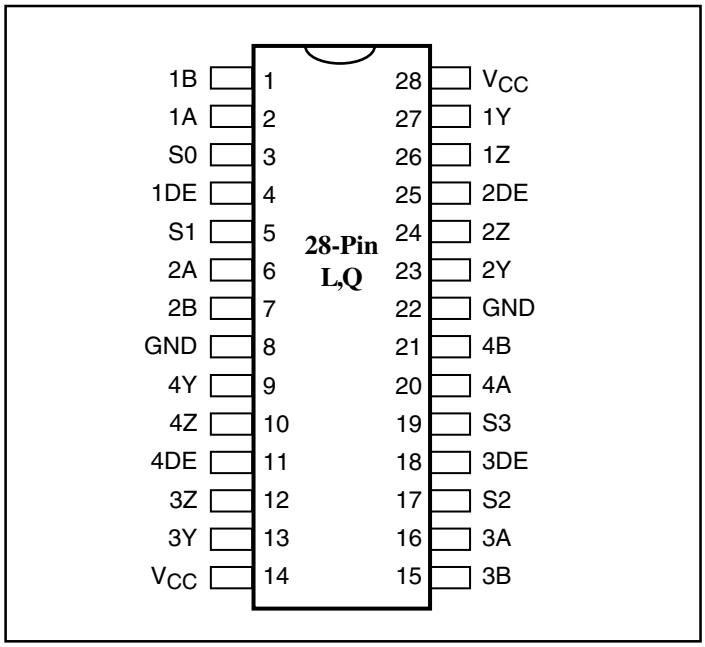


Table 1. MUX Truth Table

Input		Output		Function
S3,S1	S2,S0	1Y/1Z-3Y/3Z	2Y/2Z-4Y/4Z	
0	0	1A/1B - 3A/3B	1A/1B - 3A/3B	Splitter
0	1	2A/2B - 4A/4B	2A/2B - 4A/4B	Splitter
1	0	1A/1B - 3A/3B	2A/2B - 4A/4B	Router
1	1	2A/2B - 4A/4B	1A/1B - 3A/3B	Router

Note: Setting *n*DE to 0 will set Ouput *n*Y/*n*Z to High Impedance.

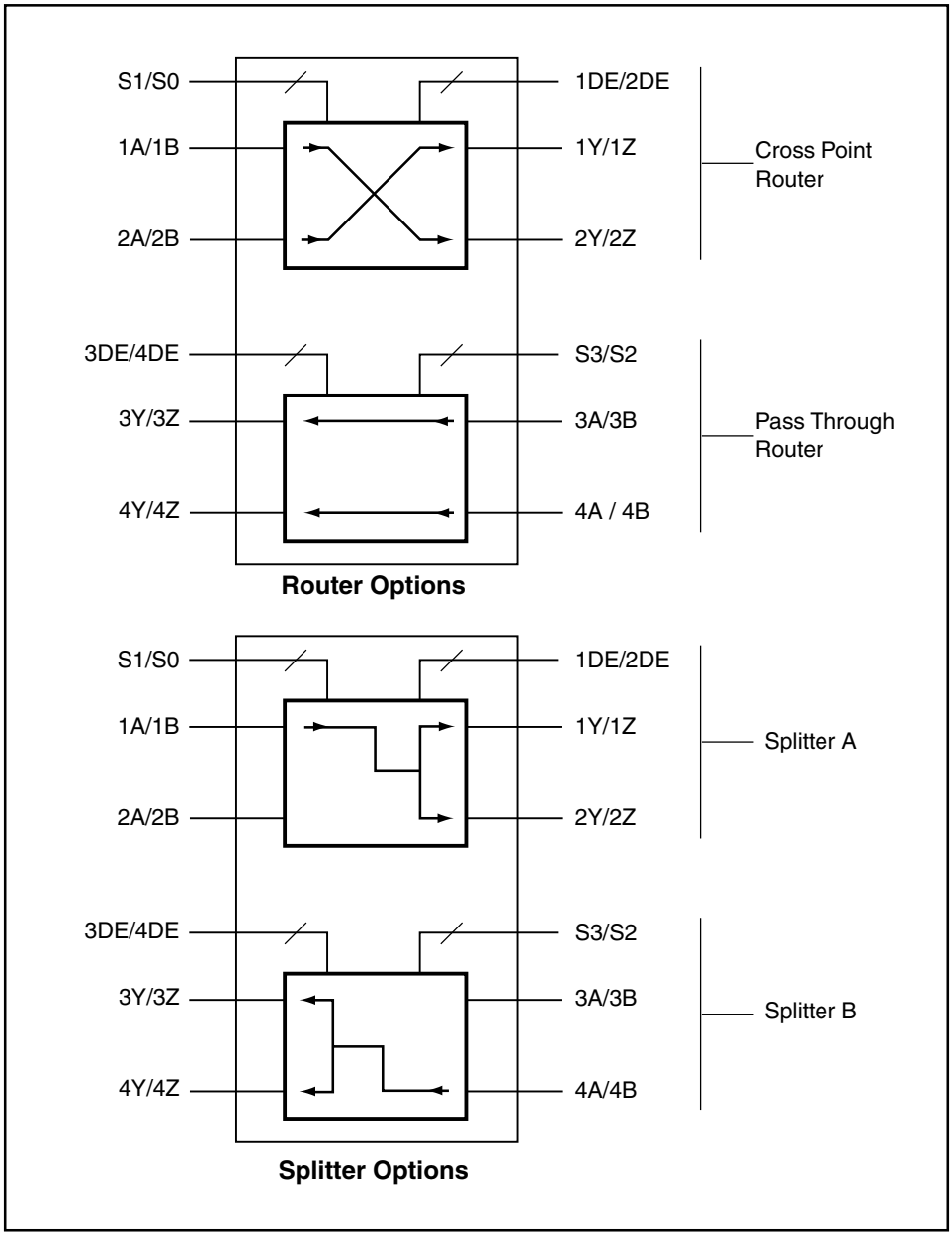


Figure 1. Possible Signal Routing

Absolute Maximum Ratings Over Operating Free-Air Temperature†

Supply Voltage Range, V_{CC}(1)	–0.5V to 4V
Voltage Range (DE, S0, S1)	–0.5 to 6V
Input Voltage Range, V_I (A or B)	–0.5V to V_{CC} + 0.5V
Electrostatic Discharge: A, B, Y, Z, and GND(2)	Class 3, A: 16kV, B:600V
All Pins	Class 3, A: 7kV, B:500V
Storage Temperature Range	–65°C to 150°C
Lead Temperature 1, 6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability.

Notes:
1. All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
2. Tested in accordance with MIL-STD-883C Method 3015.7

Recommended Operating Conditions

		Min.	Nom.	Max.	Units
Supply Voltage, V_{CC}		3.0	3.3	3.6	V
High-Level Input Voltage, V_{IH}	S0-S3, 1DE-4DE	2			
Low-Level Input Voltage, V_{IL}				0.8	
Magnitude of Differential Input Voltage $\lvert V_{ID} \rvert$		0.1		0.6	
Common-Mode input Voltage, V_{IC} (see Figure 2)		$\frac{\lvert V_{ID} \rvert}{2}$		$2.4 - \frac{\lvert V_{ID} \rvert}{2}$	
				V_{CC} –0.8	
Operating free-air temperature, T_A		–40		85	°C

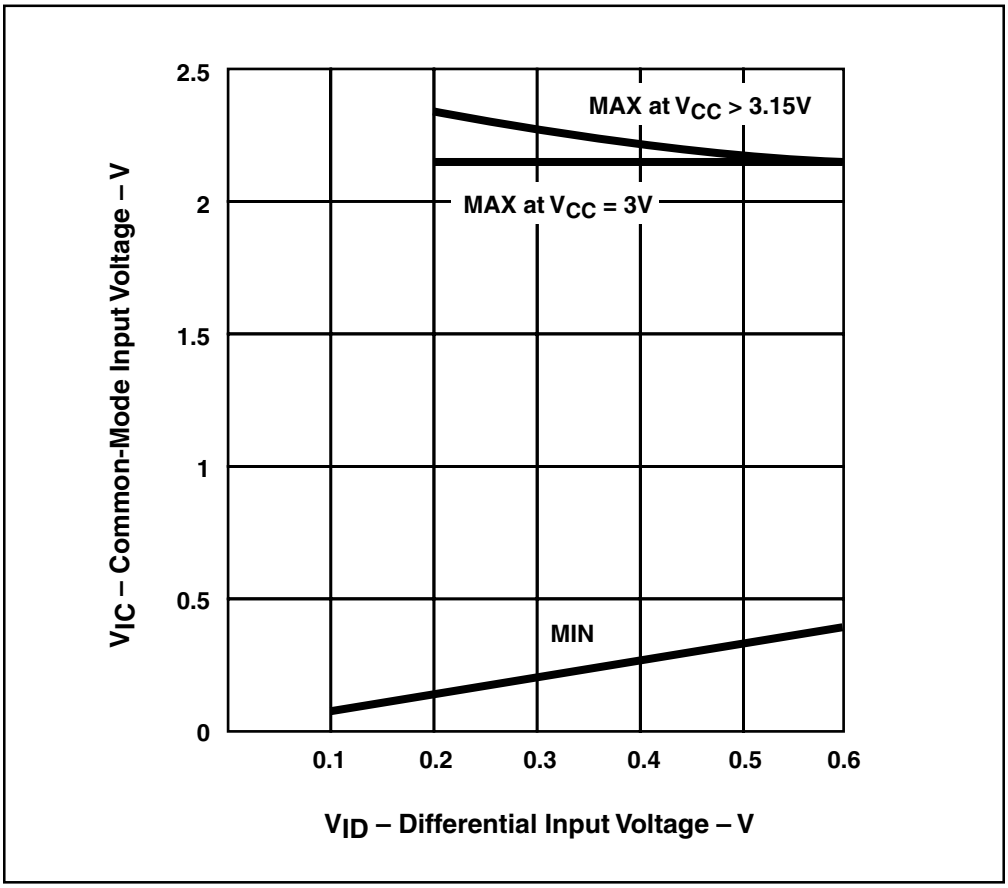


Figure 2. Common-Mode Input Voltage vs. Differential Voltage

Receiver Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Units
V_{ITH+}	Positive-going differential input voltage threshold	V_{CM} = 1.2V			100	mV
$V_{ITH–}$	Negative-going differential input voltage threshold		–100			
I_I	Input current (A or B inputs)	V_I = 0V	–2		–20	µA
		V_I = 2.4V	–1.2			
$I_{I\ (OFF)}$	Power-off input current (A or B inputs)	V_{CC} = 0V			20	

Receiver / Driver Electrical Characteristics Over Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter		Test Conditions		Min.	Typ.(1)	Max.	Units
V_{OD}	Differential output voltage magnitude		R_L = 100 Ohm (LV024)	See Fig. 3	247	440	590	mV
ΔV_{OD}	Change in differential output voltage magnitude between logic states				–50		50	
$V_{OC(SS)}$	Steady-state common-mode output voltage		R_L = 50 Ohm (LVB024)	See Fig. 4	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states				–50	3	50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage						150	
I_{CC}	Supply current		No Load			16	24	mA
			R_L = 100 Ohm (LV024)			26	40	
			R_L = 50 Ohm (LVB024)			42	54	
			Both Channels Disabled			6	12	
I_H	High-level input current	DE	V_{IH} = 5				40	nA
		S1, S2, S3, S4					–3	µA
I_{IL}	Low-level input current	DE	V_{IL} = 0.8V				–20	nA
		S1, S2, S3, S4					10	µA
I_{OS}	Short-circuit output current		V_{OY} or V_{OZ} = 0V, V_{OD} = 0V (LV024)				–10	mA
							–10	
			V_{OY} or V_{OZ} = 0V, V_{OD} = 0V (LVB024)				–10	
							–10	
I_{OZ}	High-Impedence output current		V_{OD} = 600mV			1.5	±25	nA
			V_O = 0V or V_{CC}			1.5	±25	
$I_{O(OFF)}$	Power-off output current		V_{CC} = 0V, V_O = 3.6V			1.5	±40	
C_{IN}	Input capacitance					3		pF
			S0-S3, 1DE-40DE			8		pF

Note:
1. All typical values are at 25°C and with a 3.3 supply

Differential Receiver to Driver Switching Characteristics Over Recommended Operating Conditions

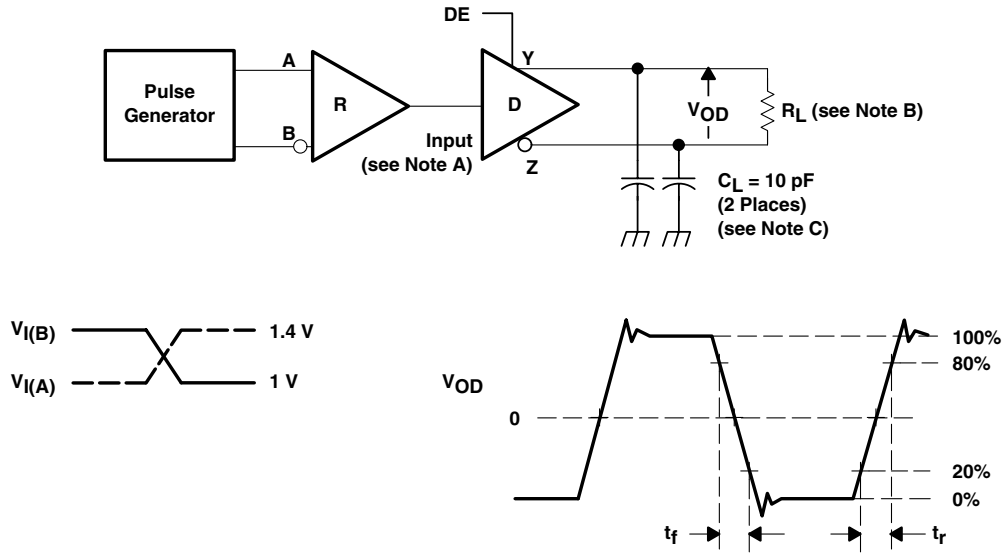
(unless otherwise noted)

Symbol	Parameter		Test Conditions	Min.	Typ.(1)	Max.	Units
t_{PLH}	Differential propagation delay, low-to-high		C_L = 10pF (See Fig. 5)		4.0	6.0	ns
t_{PHL}	Differential propagation delay, high-to-low				4.0	6.0	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				0.5	–	
t_r	Transition, low-to-high	PI90LV024			1.0	1.5	
t_r	Transition, low-to-high	PI90LVB024			0.8	1.3	
t_f	Transition, high-to-low	PI90LV024			1.0	1.5	
t_f	Transition, high-to-low	PI90LVB024			0.8	1.3	
t_{PHZ}	Propagation delay time, high-level-to-high-impedence output		(See Fig. 6)		4.0	10	
t_{PLZ}	Propagation delay time, low-level-to-high-impedence output				4.3	10	
t_{PZH}	Propagation delay time, high-impedence-to-high-level output				3.0	10	
t_{PZL}	Propagation delay time, high-impedence-to-low-level output				2.0	10	
t_{PHL}_R1_Dx	Channel-to-channel skew, receiver to driver(2)				95		ps
t_{PLH}_R1_Dx					95		
t_{PHL}_R2_Dx					95		
t_{PLH}_R2_Dx					95		

Notes:

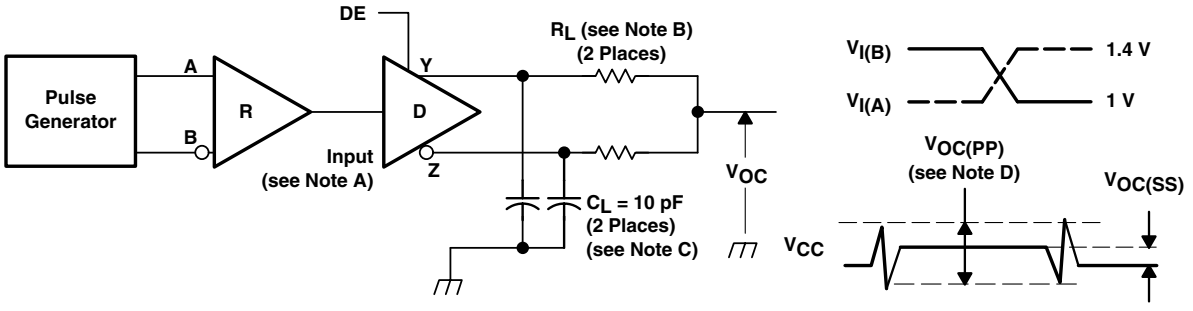
1. All typical values are at 25°C and with a 3.3 supply
2. These parametric values are measured over supply voltage and temperature ranges recommended for the device

Parameter Measurement Information



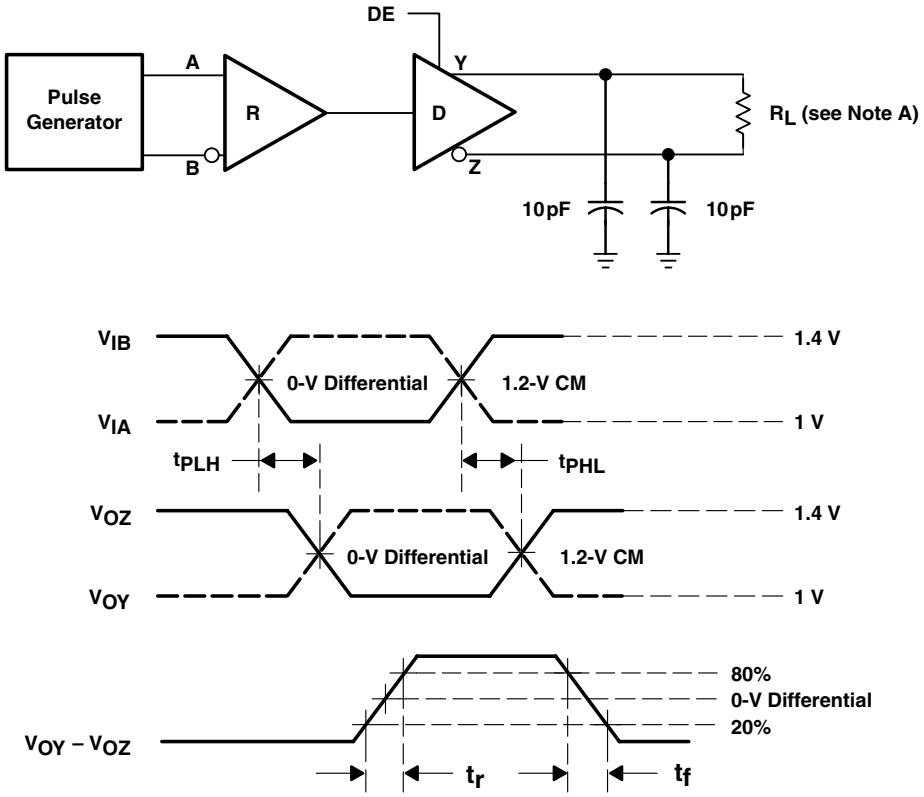
Notes: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, pulse repetition rate (PRR) - 50 Mpps, pulse width = 10 ±0.2ns.
B. R_L = 100Ω or 50Ω ±1%.
C. C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.
D. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3dB bandwidth of at least 300 MHz.

Figure 3. Test Circuit and Voltage Definitions for the Differential Output Signal



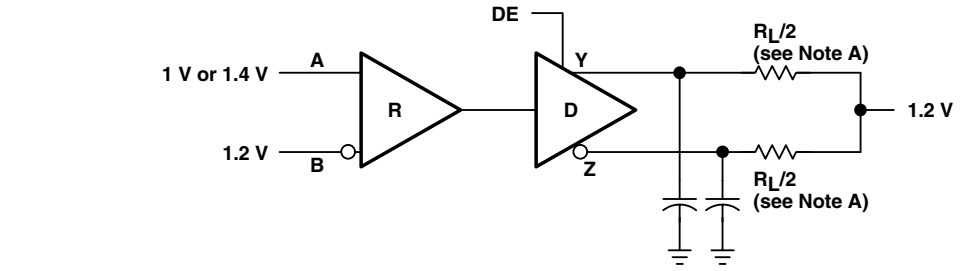
Notes: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1ns, pulse repetition rate (PRR) - 50 Mpps, pulse width = 10 ±0.2ns.
B. R_L = 100Ω or 50Ω ±1%.
C. C_L includes instrumentation and fixture capacitance within 6mm of the D.U.T.
D. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3dB bandwidth of at least 300 MHz.

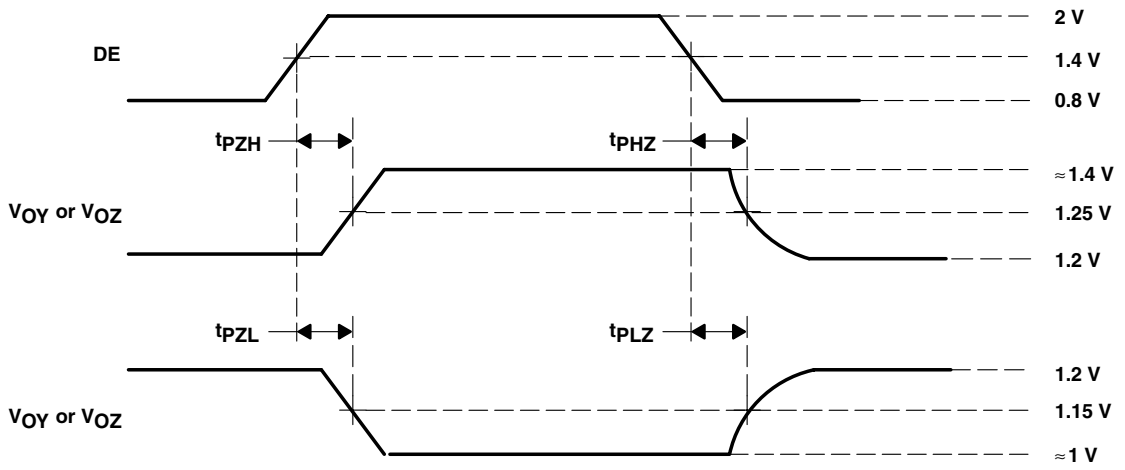
Figure 4. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



Notes: A. R_L = 100Ω or 50Ω ±1%
B. All input pulses are supplies by a generator having the following characteristics: pulse repetition rate (PPR) = 50 Mpps, pulse width = 10 ±0.2ns.

Figure 5. Differential Receiver to Driver Propagation Delay and Driver Transition Time Waveforms





Notes: A. R_L = 100Ω or 50Ω ±1%
B. All input pulses are supplied by a generator having the following characteristics: pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10ns.

Figure 6. Enable and Disable Timing Circuit

Typical Characteristics

PI90LV024
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

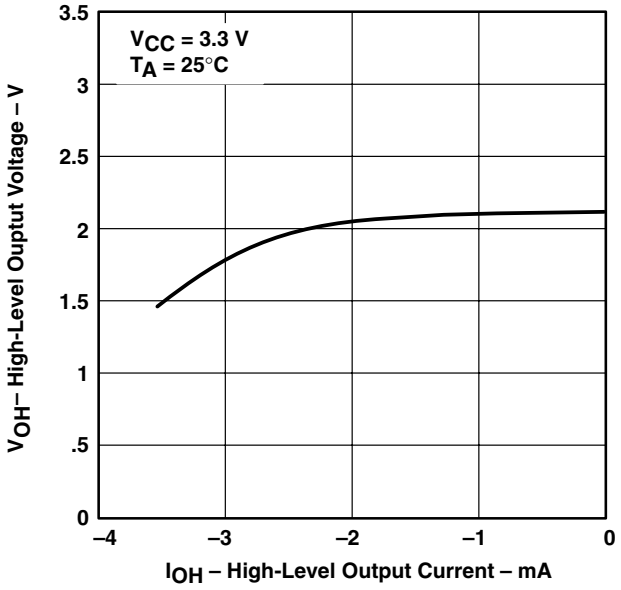


Figure 7

PI90LV024
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

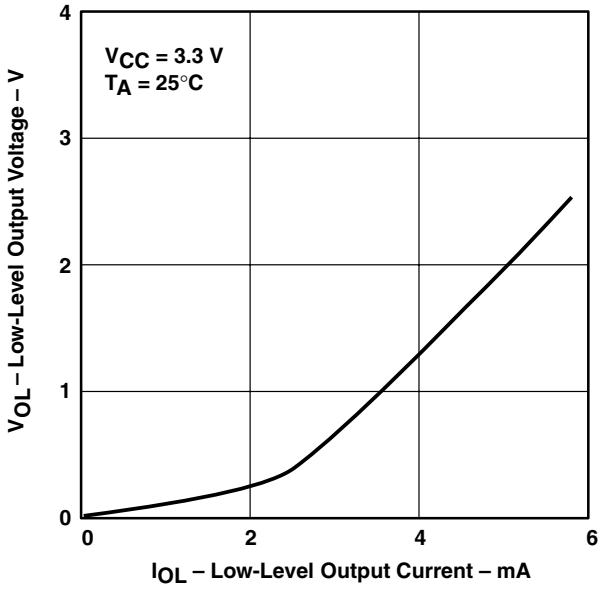


Figure 8

PI90LVB024
HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

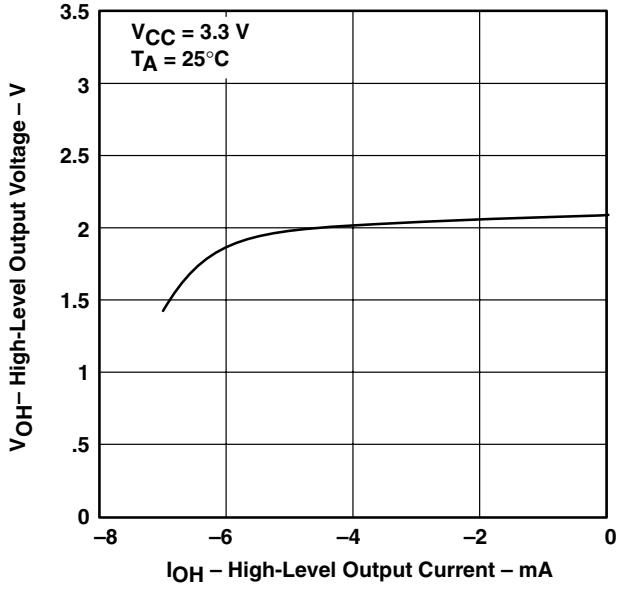


Figure 9

PI90LVB024
LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

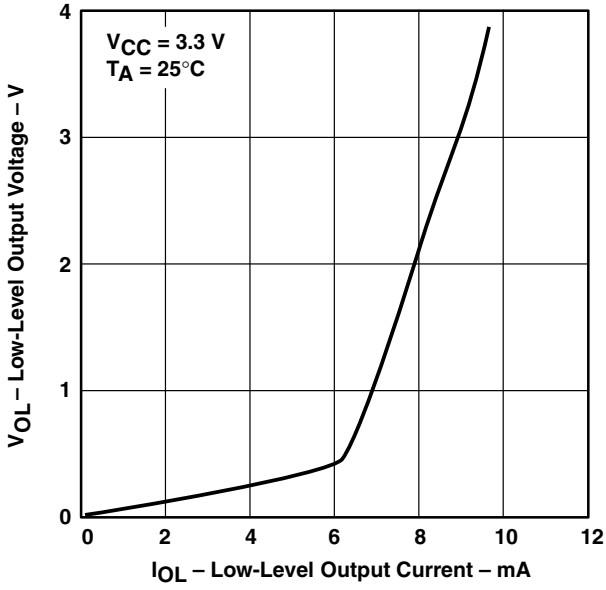
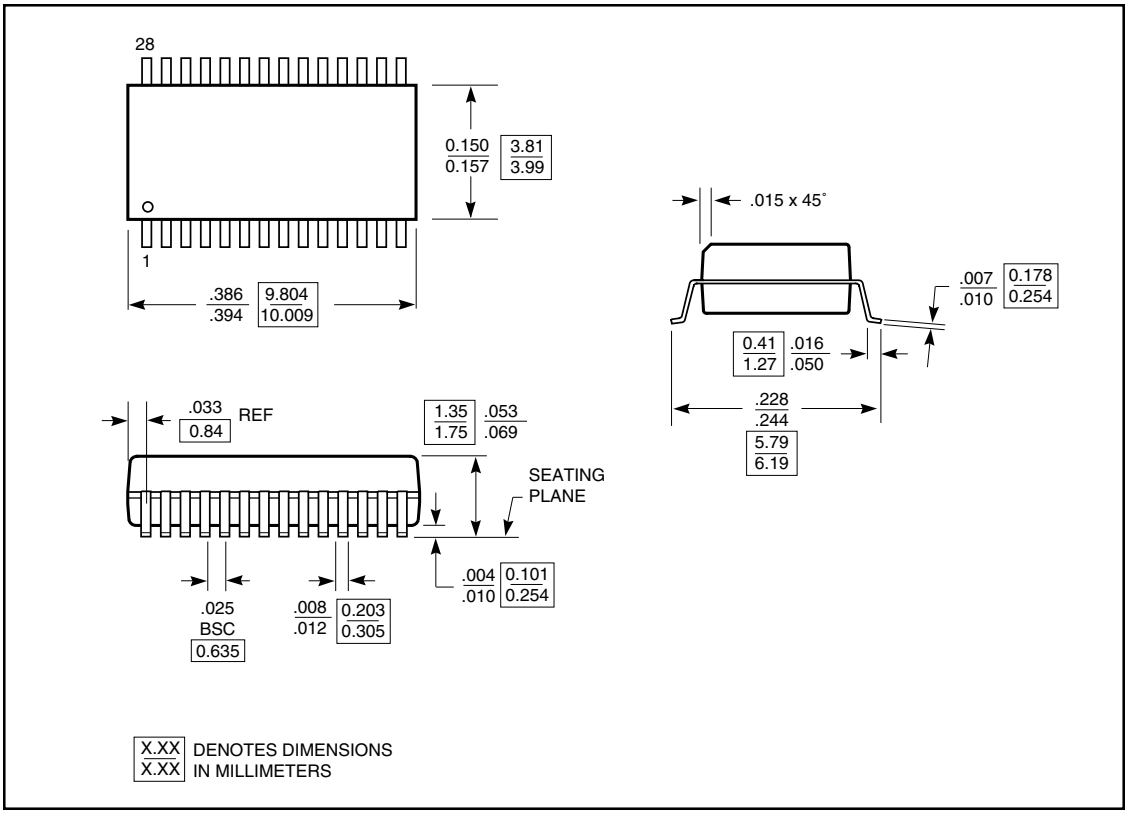
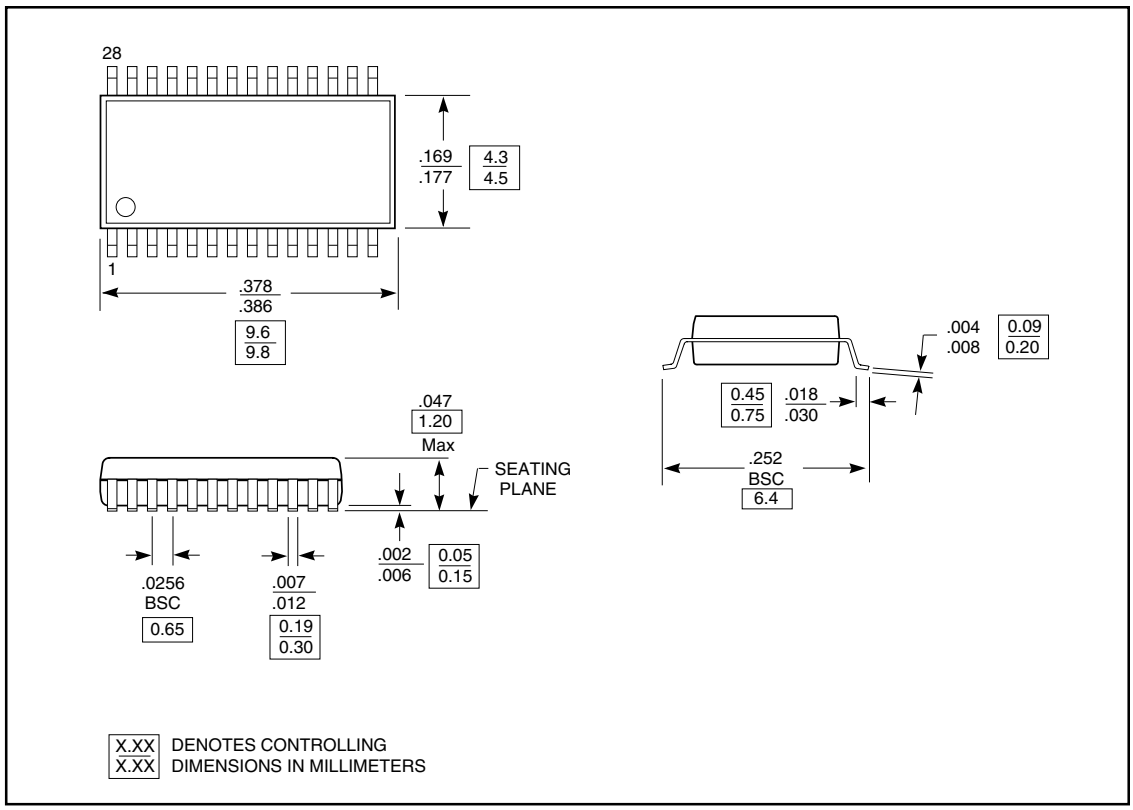


Figure 10

Packaging Mechanical: 28-Pin QSOP



Packaging Mechanical: 28-Pin TSSOP



Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
PI90LV024Q	Q28	28-pin 150-mil SOIC	–40°C to 85°C
PI90LV024L	L28	28-pin 170-mil TSSOP	
PI90LVB024Q	Q28	28-pin 150-mil SOIC	
PI90LVB024L	L28	28-pin 170-mil TSSOP	