PERICOM

PS395

Precision 8-Ch. 17V, SPST Switch w/8-Bit Serial Decoded Control

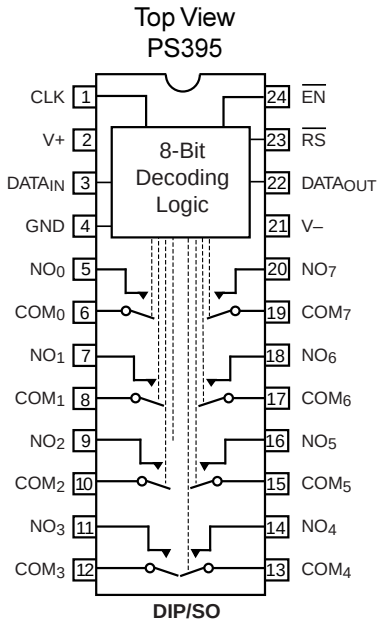
Features

- Low On-Resistance (100Ω typ.) Minimizes Distortion and Error Voltages
- Single Supply Operation (±2.7V to ±8V)
- Improved Second Source for MAX395
- SPI™/QSI™, Microwire™-Compatible Serial Interface
- Split-Supply Operation (+3V to +8V)
- On-Resistance Flatness: 10Ω Max.
- On-Resistance Matching Between Channels: 5Ω Max.
- TTL/CMOS Logic Compatible (w/+5V or ±5V supplies)
- Fast Switching Speed
- Break-Before-Make action eliminates momentary crosstalk
- Rail-to-Rail Analog Signal Range
- Low Power Consumption
- Narrow SOIC and QSOP Packages Minimize Board Area
- Asynchonous Reset ($\overline{RS}$) Input

Applications

- Data Acquisition Systems
- Audio Switching and Routing
- Test Equipment
- PBX, PABX
- Telecommunication Systems
- Battery-Powered Systems

Pin Configurations



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Description

The PS395 eight-channel, serially controlled, single-pole/single-throw (SPST) analog switch offers eight separately controlled switches that conduct equally well in either direction. ON-resistance (100Ω max.) is matched between switches to 5Ω max. and is flat (10Ω max.) over the specified signal range.

These CMOS devices can operate continuously with dual power supplies ranging from ±2.7V to ±8V or a single supply between +2.7V and +16V. Each switch can handle rail-to-rail analog signals. The off leakage current is only 0.1nA at +25°C or 5nA at +85°C.

Upon power-up, all switches are off, and the internal shift registers are reset to zero. The PS395 is electrically equivalent to two PS391 quad switches controlled by a serial interface, and is pin compatible with the PS335.

The serial interface is compatible with SPI™/QSPI™ and Microwire™. Functioning as a shift register, it allows data (at DIN) to be clocked-in synchronously with the rising edge of clock (SCLK). The shift register's output (DOUT) enables several PS395s to be daisy chained.

All digital inputs have 0.8V to 2.4V logic thresholds, ensuring both TTL- and CMOS-logic compatibility when using ±5V supplies or a single +5V supply.

Pin Description

Name	Function
CLK	Serial Clock Digital Input
V+	Positive Analog Supply Voltage Input
$DATA_{IN}$	Serial Data Digital Input
GND	Ground
NO_0–NO_7	Normally Open Analog Switches 0–7
COM_0–COM_7	Common Analog Switches 0–7
V–	Negative Analog Supply Voltage Input
$DATA_{OUT}$	Serial Data Digital Output
$\overline{RS}$	Reset Input ($\overline{RESET}$)
$\overline{CS}$	Chip-Select Digital Input

Note:
$\overline{NO}$ and $\overline{COM}$ pins are identical and interchangeble. Either may be considered as an input or an output; signals pass equally well in either direction.

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Serial-Interface Truth Table

$\overline{RS}$	Data Bits								Function
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	X	X	X	X	X	X	X	Switches 7 open (off)
1	1	X	X	X	X	X	X	X	Switches 7 closed (on)
1	X	0	X	X	X	X	X	X	Switches 6 open (off)
1	X	1	X	X	X	X	X	X	Switches 6 closed (on)
1	0	X	0	X	X	X	X	X	Switches 5 open (off)
1	1	X	1	X	X	X	X	X	Switches 5 closed (on)
1	X	X	X	0	X	X	X	X	Switches 4 open (off)
1	X	X	X	1	X	X	X	X	Switches 4 closed (on)
1	X	X	X	X	0	X	X	X	Switches 3 open (off)
1	X	X	X	X	1	X	X	X	Switches 3 closed (on)
1	X	X	X	X	X	0	X	X	Switches 2 open (off)
1	X	X	X	X	X	1	X	X	Switches 2 closed (on)
1	X	X	X	X	X	X	0	X	Switches 1 open (off)
1	X	X	X	X	X	X	1	X	Switches 1 closed (on)
1	X	X	X	X	X	X	X	0	Switches 0 open (off)
1	X	X	X	X	X	X	X	1	Switches 0 closed (on)

SPDT Truth Table

RS	Data Bits								Function
	D7	D6	D5	D4	D3	D2	D1	D0	
0	X	X	X	X	X	X	X	X	All switches open, D7–D0 = 0
1	0	1	X	X	X	X	X	X	Switch 7 off and 6 on
1	1	0	X	X	X	X	X	X	Switch 6 off and 7 on
1	X	X	0	1	X	X	X	X	Switch 5 off and 4 on
1	X	X	1	0	X	X	X	X	Switch 4 off and 5 on
1	X	X	X	X	0	1	X	X	Switch 3 off and 2 on
1	X	X	X	X	1	0	X	X	Switch 2 off and 3 on
1	X	X	X	X	X	X	0	1	Switch 1 off and 0 on
1	X	X	X	X	X	X	1	0	Switch 0 off and 1 on

Absolute Maximum Ratings

Voltages Referenced to GND

V+ ..... –0.3V, +17V
V– ..... –17V, +0.3V
V+ to V- ..... -0.3V, +17V
SCLK, $\overline{CS}$, DIN, DOUT, $\overline{RESET}$ ..... -0.3V to (V+ + 0.3V)
NO, COM ..... (V- - 2V) to (V+ + 2V)
Continuous Current into Any Terminal ..... ±30mA
Peak Current, NO_ or COM_
(pulsed at 1ms, 10% duty cycle) ..... ±100mA

Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 13.33mW/°C above +70°C) 1067mW
Wide SO (derate 11.76mW/°C above +70°C) 941mW
Operating Temperature Ranges
PS395C_G ..... 0°C to +70°C
PS395E_G ..... -40°C to +85°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Specifications - Dual Supplies

(V± = +4.5V to +5.5V, V– = 4.5V to –5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

Parameter	Symbol	Conditions		Min.(2)	Typ.(1)	Max.(2)	Units
Analog Switch							
Analog Signal Range (3)	V_{COM}, V_{NO}		C,E	V–		V+	V
COM, NO On Resistance	R_{ON}	V+ = 5V, V– = –5V, V_{COM} = ±3V, I_{NO} = 1mA	T_A = +25V		60	100	Ω
			C,E			125	
COM, NO On Resistance Match Between Channels(2)	ΔR_{ON}	V+ = 5V, V– = –5V, V_{COM} = ±3V, I_{NO} = 1mA	T_A = +25V			5	
			C,E			10	
COM, NO On Resistance Flatness(2)	$R_{FLAT(ON)}$	V+ = 5V, V– = –5V, I_{NO} = 1mA, V_{COM} = –3V, 0V, 3V	T_A = +25V			10	
			C,E			15	
NO Off Leakage Current(3)	$I_{NO(OFF)}$	V+ = 5.5V, V– = –5.5V, V_{COM} = –4.5V, V_{NO} = 4.5V	T_A = +25V	–0.1	0.002	0.1	nA
			C,E	–1.0		10	
		V+ = 5.5V, V– = –5.5V, V_{COM} = 4.5V, V_{NO} = –4.5V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–10		10	
COM Off Leakage Current(3)	$I_{COM(OFF)}$	V+ = 5.5V, V– = –5.5V, V_{COM} = –4.5V, V_{NO} = 4.5V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–1.0		10	
		V+ = 5.5V, V– = –5.5V, V_{COM} = 4.5V, V_{NO} = –4.5V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–10		10	
COM On Leakage Current(3)	$I_{COM(ON)}$	V+ = 5.5V, V– = –5.5V, V_{COM} = V_{NO} = ±4.5V	T_A = +25V	–0.2	0.01	0.2	
			C,E	–20		20	
Digital I/O							
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}		C,E	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IL}					0.8	
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V		–1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = 0.8mA		2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = –1.6mA		0		0.4	
SCLK Input Hysteresis	$SCLK_{HYST}$				100		mV

Electrical Specifications - Dual Supplies (continued)

(V± = +4.5V to +5.5V, V– = 4.5V to –5.5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

Parameter	Symbol	Conditions		Min.(2)	Typ.(1)	Max.(2)	Units
Switch Dynamic Characteristics							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25V		200	400	nσ
			C,E			500	
Turn-Off Time	t_{OFF}		T_A = +25V		90	400	
			C,E			500	
Break-Before-Make Delay	t_{BBM}		T_A = +25V	5	15		
Charge Injection(4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25V		2	10	pC
NO Off Capacitance	$C_{NO(OFF)}$	V_{NO} =GND, f = 1MHz	C,E		2		pF
COM Off Capacitance	$C_{COM(OFF)}$	V_{COM} =GND, f = 1MHz	T_A = +25V		2	15	
Switch Off Capacitance	$C_{(ON)}$	V_{COM} =V_{NO} = GND, f = 1MHz	C,E		8		
Off Isolation	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25V		–90		dB
Channel-to-Channel Crosstalk	V_{CT}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	C,E		<–90		
Power Supply							
Power-Supply Range	V+,V–		C,E	±3		±8	V
V+ Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+	T_A = +25V		7	20	µA
			C,E			30	
V– Supply Current	I–	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+	T_A = +25V	–1	0.1	1	
			C,E	–2		2	

Timing Characteristics - Dual Supplies

(V± = ±4.5V to 5.5V, V– = –4/5V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C).

Parameter	Symbol	Conditions		Min.(1)	Typ.(1)	Max.(1)	Units
Serial Digital Interface							
SCLK Frequency	f_{SCLK}		C, E	0		2.1	MHz
Cycle Time	$t_{CH} + t_{CL}$			480			ns
$\overline{CS}$ Lead Time	t_{CSS}			240			
$\overline{CS}$ Lag Time	t_{CSH2}			240			
SCLK High Time	t_{CH}			190			
SCLK Low Time	t_{CL}			190			
Data Setup Time	t_{DS}			200	17		
Data Hold Time	t_{DH}			0	–17		
DIN Data Valid after Falling SCLK(4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25V		85		
			C, E			400	
Rise Time of DOUT(4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF				100	
Allowable Rise Time at DIN, SCLK(4)	t_{SCR}					2	ns
Fall Time of DOUT(4)	t_{DF}					100	µs
Allowable Fall Time at DIN, SCLK(4)	t_{SCF}					2	ns
$\overline{RESET}$ Minimum Pulse Width	t_{RW}				70		

Notes:

1. The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
2. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
3. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.
4. Guaranteed by design.
5. Leakage testing at single supply is guaranteed by testing with dual supplies.
6. See Figure 5. Off isolation = 20log10 V_{COM}/V_{NO}, V_{COM} = output. NO = input to off switch.
7. Between any two switches. See Figure 2.

Electrical Characteristics - Single 5V Supply

(V+ = + 5V ± 10%, V- = 0V, GND = 0V, V_{AH} = V_{ENH} = +2.4, V_{AL} = V_{ENL} = +0.8V)

Parameter	Symbol	Conditions		Min.(2)	Typ.(1)	Max.(2)	Units
Analog Switch							
Analog Signal Range (3)	V_{COM},V_{NO}		C,E	V–		V+	V
COM, NO On Resistance	R_{ON}	V+ = 5V, V_{COM} = 3.5V, I_{NO} = 1mA	T_A = +25V		125	175	Ω
			C,E			225	
NO Off Leakage Current(4,5)	$I_{NO(OFF)}$	V+ = 5.5V, V_{COM} = –4.5V, V_{NO} = 0V	T_A = +25V	–0.1	0.002	0.1	nA
			C,E	–10		10	
		V+ = 5.5V, V– = –5.5V, V_{COM} = 4.5V, V_{NO} = –4.5V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–10		10	
COM Off Leakage Current(4,5	$I_{COM(OFF)}$	V+ = 5.5V, V_{COM} = –4.5V, V_{NO} = 0V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–10		10	
		V+ = 5.5V, V– = –5.5V, V_{COM} = 4.5V, V_{NO} = –4.5V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–10		10	
COM On Leakage Current(4,5)	$I_{COM(ON)}$	V+ = 5.5V, V_{COM} = V_{NO} = 4.5V	T_A = +25V	–0.2	0.02	0.2	
			C,E	–20		20	
Digital I/O							
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}		C,E	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}					0.8	
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V		–1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = –0.8mA		2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = –1.6mA		0		0.4	
SCLK Input Hysteresis	$SCLK_{HYST}$				100		mV
Switch Dynamic Characteristics							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25V		200	400	ns
			C,E			500	
Turn-Off Time	t_{OFF}		T_A = +25V		90	400	
			C,E			500	
Break-Before-Make Delay	t_{BBM}		T_A = +25V		15		
Charge Injection(4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25V		2	10	pC
Off Isolation(6)	V_{ISO}	R_L = 1nF, C_L = 15pF, V_{NO} = $1V_{RMS}$, f= 100kHz	T_A = +25V		–90		dB
Channel-to-Channel Crosstalk(6)	V_{CT}		T_A = +25V		<–90		
Power Supply							
V+, V– Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or V+	T_A = +25V		7	20	µA
			C,E			30	

Timing Characteristics - Single +5V Supply

(V+ = ±4.5V to 5.5V, V– = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C).

Parameter	Symbol	Conditions		Min.(1)	Typ.(1)	Max.(1)	Units
Serial Digital Interface							
SCLK Frequency	f_{SCLK}		C, E	0		2.1	MHz
Cycle Time(4)	$t_{CH} + t_{CL}$			480			ns
$\overline{CS}$ Lead Time(4)	t_{CSS}			240			
$\overline{CS}$ Lag Time(4)	t_{CSH2}			240			
SCLK High Time(4)	t_{CH}			190			
SCLK Low Time(4)	t_{CL}			190			
Data Setup Time(4)	t_{DS}			200	17		
Data Hold Time(4)	t_{DH}			0	–17		
DIN Data Valid after Falling SCLK(4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25V		85		
			C, E			400	
Rise Time of DOUT(4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF				100	
Allowable Rise Time at DIN, SCLK(4)	t_{SCR}					2	ns
Fall Time of DOUT(4)	t_{DF}					100	µs
Allowable Fall Time at DIN, SCLK(4)	t_{SCF}					2	ns
$\overline{RESET}$ Minimum Pulse Width	t_{RW}				70		

Notes:

1. The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
2. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
3. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.
4. Guaranteed by design.
5. Leakage testing at single supply is guaranteed by testing with dual supplies.
6. See Figure 5. Off isolation = 20log10 V_{COM}/V_{NO}, V_{COM} = output. NO = input to off switch.
7. Between any two switches. See Figure 2.

Electrical Characteristics - Single +3V Supply

(V+ = +3.0V + 3.6V, V– = 0V, T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C)

Parameter	Symbol	Conditions		Min.(2)	Typ.(1)	Max.(2)	Units
Analog Switch							
Analog Signal Range (3)	V_{COM},V_{NO}		C,E	V–		V+	V
COM, NO On Resistance	R_{ON}	V+ = 3.0, V_{COM} = 1.5V, I_{NO} = 1mA	T_A = +25V		270	500	Ω
			C,E			600	
NO Off Leakage Current(4,5)	$I_{NO(OFF)}$	V+ = 3.0V, V_{COM} = 3V, V_{NO} = 0V	T_A = +25V	–0.1	0.002	0.1	nA
			C,E	–5		5	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–5		5	
COM Off Leakage Current(4,5	$I_{COM(OFF)}$	V+ = 3.6V, V_{COM} = 3V, V_{NO} = 0V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–5		5	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–5		5	
COM On Leakage Current(4,5)	$I_{COM(ON)}$	V+ = 3.6V, V_{COM} = 3V, V_{NO} = 0V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–10		10	
		V+ = 3.6V, V_{COM} = 0V, V_{NO} = 3V	T_A = +25V	–0.1	0.002	0.1	
			C,E	–10		10	
Digital I/O							
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold High	V_{IH}		C,E	2.4			V
DIN, SCLK, $\overline{CS}$, $\overline{RESET}$ Input Voltage Logic Threshold Low	V_{IL}					0.8	
DIN, SCLK, $\overline{CS}$, Input Current Logic High or Low	I_{IH}, I_{IL}	V_{DIN}, V_{SCLK}, $V_{\overline{CS}}$ = 0.8V or 2.4V		–1	0.03	1	µA
DOUT Output Voltage Logic High	V_{DOUT}	I_{DOUT} = –0.1mA		2.8		V+	V
DOUT Output Voltage Logic Low	V_{DOUT}	I_{DOUT} = –1.6mA		0		0.4	
SCLK Input Hysteresis	$SCLK_{HYST}$				100		mV
Switch Dynamic Characteristics							
Turn-On Time	t_{ON}	From rising edge of $\overline{CS}$	T_A = +25V		260	600	ns
			C,E			800	
Turn-Off Time	t_{OFF}		T_A = +25V		90	300	
			C,E			400	
Break-Before-Make Delay	t_{BBM}		T_A = +25V		15		
Charge Injection(4)	V_{CTE}	C_L = 1nF, V_{NO} = 0V, R_S = 0Ω	T_A = +25V		2	10	pC
Off Isolation(6)	V_{ISO}	R_L = 50Ω, C_L = 15pF, V_{NO} = $1V_{RMS}$, f = 100kHz	T_A = +25V		–90		dB
Channel-to-Channel Crosstalk(7)	V_{CT}		T_A = +25V		<–90		
Power Supply							
V+, V– Supply Current	I+	DIN = $\overline{CS}$ = SCLK = 0V or V+, $\overline{RESET}$ = 0V or 5V	T_A = +25V		6	20	µA
			C,E			30	

Timing Characteristics - Single +3V Supply

(V+ = ±3.0V to +3.6V, V– = 0V, $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted. Typical values are T_A = +25°C).

Parameter	Symbol	Conditions		Min.(1)	Typ.(1)	Max.(1)	Units
Serial Digital Interface							
SCLK Frequency	f_{SCLK}		C, E	0		2.1	MHz
Cycle Time(4)	$t_{CH} + t_{CL}$			480			ns
$\overline{CS}$ Lead Time(4)	t_{CSS}			240			
$\overline{CS}$ Lag Time(4)	t_{CSH2}			240			
SCLK High Time(4)	t_{CH}			190			
SCLK Low Time(4)	t_{CL}			190			
Data Setup Time(4)	t_{DS}			200	38		
Data Hold Time(4)	t_{DH}			0	–38		
DIN Data Valid after Falling SCLK(4)	t_{DO}	50% of SCLK to 10% of DOUT, C_L = 10pF	T_A = +25V		150		
			C, E			400	
Rise Time of DOUT(4)	t_{DR}	20% of V+ to 70% of V+, C_L = 10pF				100	
Allowable Rise Time at DIN, SCLK(4)	t_{SCR}					2	ns
Fall Time of DOUT(4)	t_{DF}					300	µs
Allowable Fall Time at DIN, SCLK(4)	t_{SCF}					2	ns
$\overline{RESET}$ Minimum Pulse Width	t_{RW}		T_A = +25V		105		

Notes:

1. The algebraic convention is used in this data sheet; the most negative value is shown in the minimum column.
2. $\Delta R_{ON} = R_{ON(MAX)} - R_{ON(MIN)}$. On-resistance match between channels and on-resistance flatness are guaranteed only with specified voltages. Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
3. Leakage parameters are 100% tested at maximum rated hot temperature and guaranteed by correlation at room temp.
4. Guaranteed by design.
5. Leakage testing at single supply is guaranteed by testing with dual supplies.
6. See Figure 5. Off isolation = 20log10 V_{COM}/V_{NO}, V_{COM} = output. NO = input to off switch.
7. Between any two switches. See Figure 2.

Detailed Description

Basic Operation

The PS395's interface can be thought of as an 8-bit shift register controlled by $\overline{CS}$ (Figure 7). While $\overline{CS}$ is low, input data appearing at DIN is clocked into the shift register synchronously with SCLK's rising edge. The data is an 8-bit word, each bit controlling one of eight switches in the PS395. DOUT is the shift register's output, with data appearing synchronously with SCLK's falling edge. Data at DOUT is simply the input data delayed by eight clock cycles.

When shifting the input data, D7 is the first bit in and out of the shift register. While shifting data, the switches remain in their previous configuration. When the eight bits of data have been shifted in, $\overline{CS}$ is driven high. This updates the new switch configuration and inhibits further data from entering the shift register. Transitions at DIN and SCLK have no effect when $\overline{CS}$ is high, and DOUT holds the first input bit (D7) at its output.

More or less than eight clock cycles can be entered during the $\overline{CS}$ low period. When this happens, the shift register will contain only the last eight serial data bits, regardless of when they were entered. On the rising edge of $\overline{CS}$, all the switches will be set to the corresponding states.

The PS395's three-wire serial interface is compatible with SPI™, QSPI™, and Microwire™ standards. If inter-facing with a Motorola processor serial interface, set CPOL = 0. The PS395 is considered a slave device (Figures 2 and 7). Upon power-up, the shift register contains all zeros, and all switches are off.

The latch that drives the analog switch is updated on the rising edge of $\overline{CS}$, regardless of SCLK's state. This meets all the SPI and QSPI requirements.

Daisy Chaining

For a simple interface using several PS395s, "daisy chain" the shift registers as shown in Figure 5. The $\overline{CS}$ pins of all devices are connected together, and a stream of data is shifted through the PS395s in series. When $\overline{CS}$ is brought high, all switches are updated simultaneously. Additional shift registers may be included anywhere in series with the PS395 data chain.

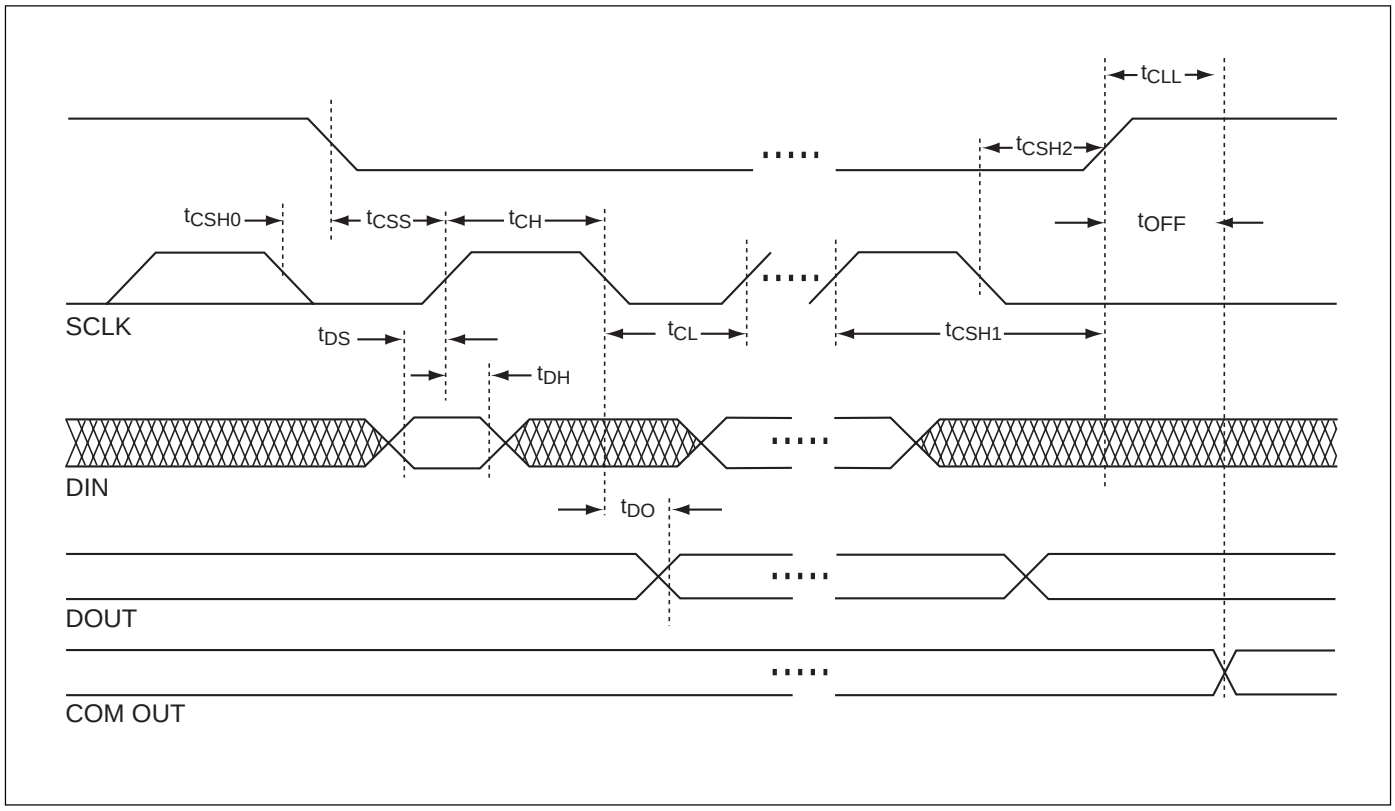

Figure 1. Timing Diagram

8x1 Multiplexer

To use the PS395 as an 8x1 multiplexer, connect all common pins together (COM0–COM7) to form the mux output; the mux inputs are NO0–NO7.

The mux can be programmed normally, with only one channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse. In this mode, the channels are selected by sending a single high pulse (corresponding to the selected channel) at DIN, and a corresponding $\overline{CS}$ low pulse for every eight clock pulses. As this is clocked through the register by SCLK, each switch sequences one channel at a time, starting with Channel 7.

Dual, Differential 4-Channel Multiplexer

To use the PS395 as a dual (4x2) mux, connect COM0–COM3 together and connect COM4–COM7 together, forming the two outputs. The mux input pairs become NO0/NO4, NO1/NO5, NO2/NO6, and NO3/NO7.

The mux can be programmed normally, with only one differential channel selected for every eight clock pulses, or it can be programmed in a fast mode, where channel changing occurs on each clock pulse.

In fast mode, the channels are selected by sending two high pulses spaced four clock pulses apart (corresponding to the two selected channels) at DIN, and a corresponding $\overline{CS}$ low pulse for each of the first eight clock pulses. As this is clocked through the register by SCLK, each switch sequences one differential channel at a time, starting with channel 7/0. After the first eight bits have been sent, subsequent channel sequencing can occur by repeating this sequence or, even faster, by sending only one DIN high pulse and one $\overline{CS}$ low pulse for each four clock pulses.

SPDT Switches

To use the PS395 as a quad, single-pole/double-throw (SPDT) switch, connect COM0 to NO1, COM2 to NO3, COM4 to NO5, and COM6 to NO7, forming the four "common" pins. Program these four switches with pairs of instructions, as shown in SPST Truth Table.

Reset Function

$\overline{RESET}$ is the internal reset pin. It is usually connected to a logic signal or V+. Drive $\overline{RESET}$ low to open all switches and set the contents of the internal shift register to zero simultaneously. When $\overline{RESET}$ is high, the part functions normally and DOUT is sourced from V+. $\overline{RESET}$ must not be driven beyond V+ or GND.

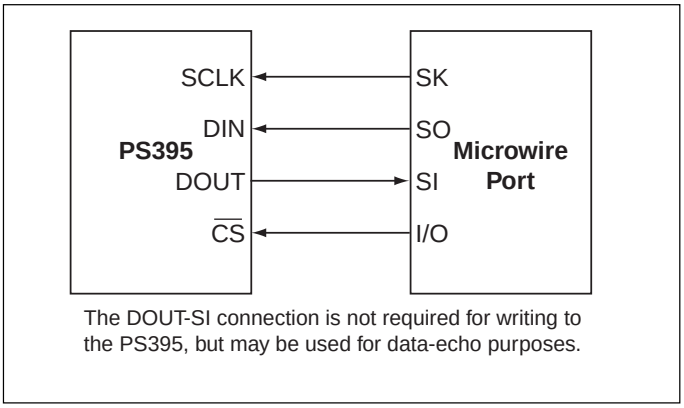

Figure 2. Connections for Microwire

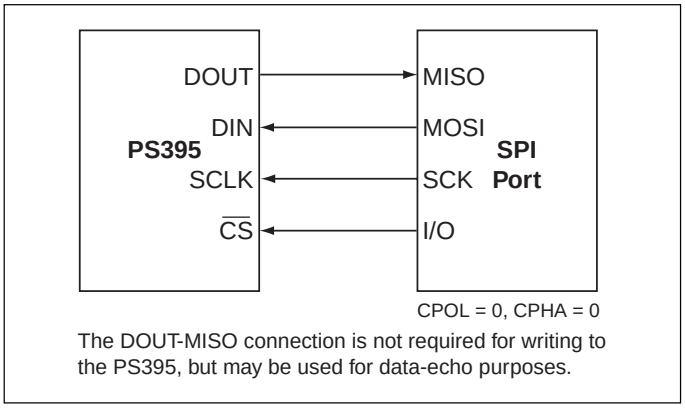

Figure 3. Connections for SPI and QSPI

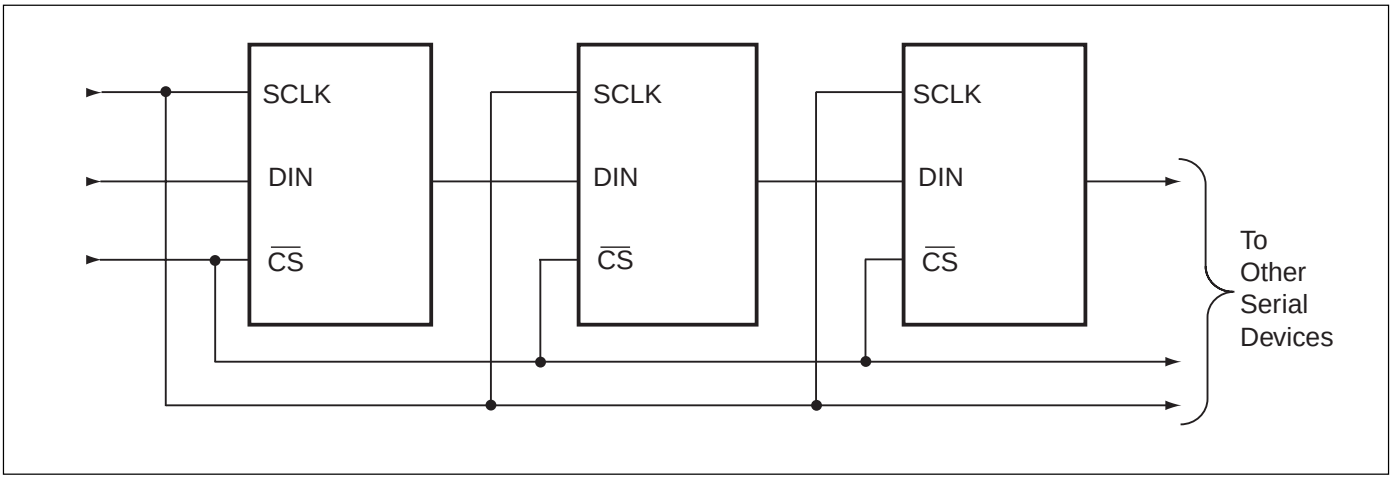

Figure 4. Daisy-Chained Connection

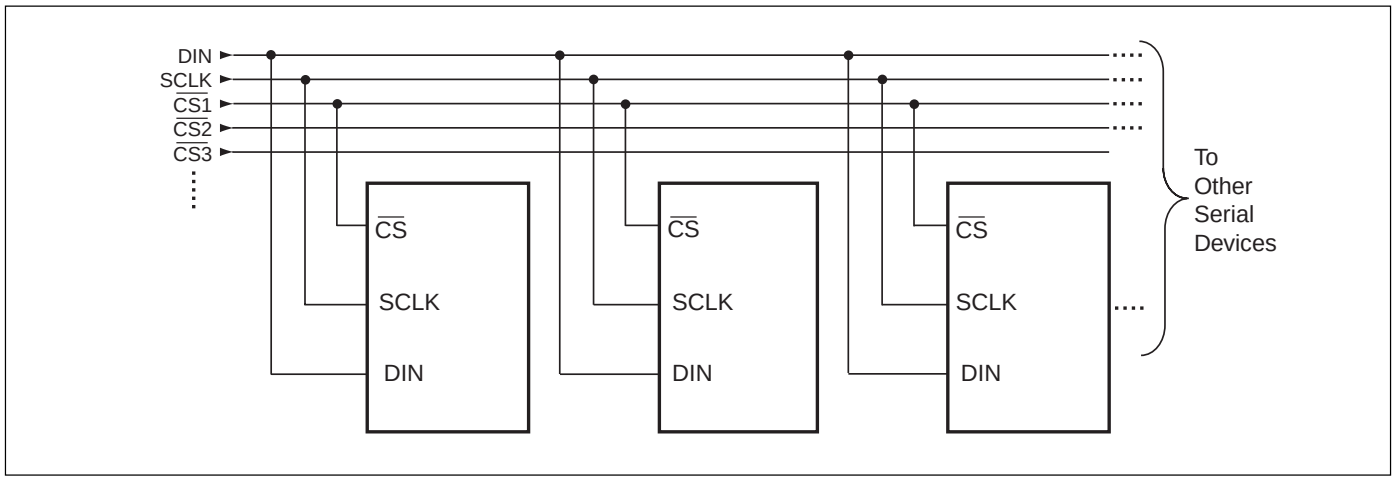

Figure 5. Addressable Serial Interface

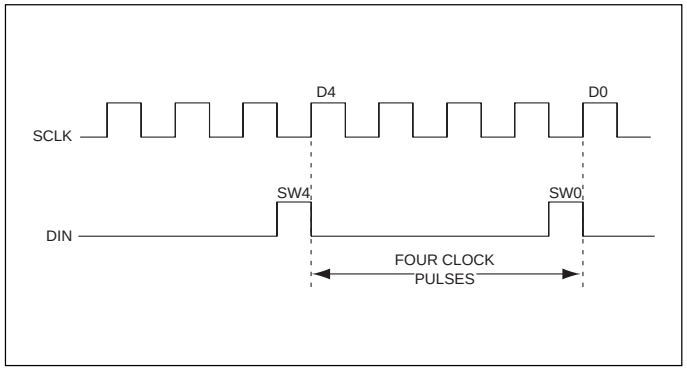

Figure 6. Differential Multiplexer Input Control

Power-Supply Considerations

Overview

The PS395 construction is typical of most CMOS analog switches. It has three supply pins: V+, V-, and GND. V+ and V- are used to drive the internal CMOS switches and to set the limits of the analog voltage on any switch. Reverse ESD-protection diodes are internally connected between each analog signal pin and both V+ and V-. If any analog signal exceeds V+ or V-, one of these diodes will conduct. During normal operation, these (and other) reverse-biased ESD diodes leak, forming the only current drawn from V+ or V-.

Virtually all the analog leakage current is through the ESD diodes. Although the ESD diodes on a given signal pin are identical, and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or V- and the analog signal. This means their leakages vary as the signal varies. The difference in the two diode leakages to the V+ and V- pins constitutes the analog signal-path leakage current. All analog leakage current flows to the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of either the same or opposite polarity.

There is no connection between the analog signal paths and GND.

V+ and GND power the internal logic and logic-level translators, and set both the input and output logic limits. The logic-level translators convert the logic levels to switched V+ and V- signals to drive the analog signal gates. This drive signal is the only connection between logic supplies (and signals) and the analog supplies. V+, and V- have ESD-protection diodes to GND. The logic-level inputs and output have ESD protection to V+ and to GND.

The logic-level thresholds are CMOS and TTL compatible when V+ is +5V. As V+ is raised, the threshold increases slightly. So when V+ reaches +12V, the threshold is about 3.1V; slightly above the TTL guaranteed high-level minimum of 2.8V, but still compatible with CMOS outputs.

Bipolar Supplies

The PS395 operates with bipolar supplies between ±3.0V and ±8V. The V+ and V- supplies need not be symmetrical, but their sum cannot exceed the absolute maximum rating of 17V. **Do not connect the PS395 V+ to +3V and connect the logic-level pins to TTL logic-level signals. This exceeds the absolute maximum ratings and can damage the part and/or external circuits.**

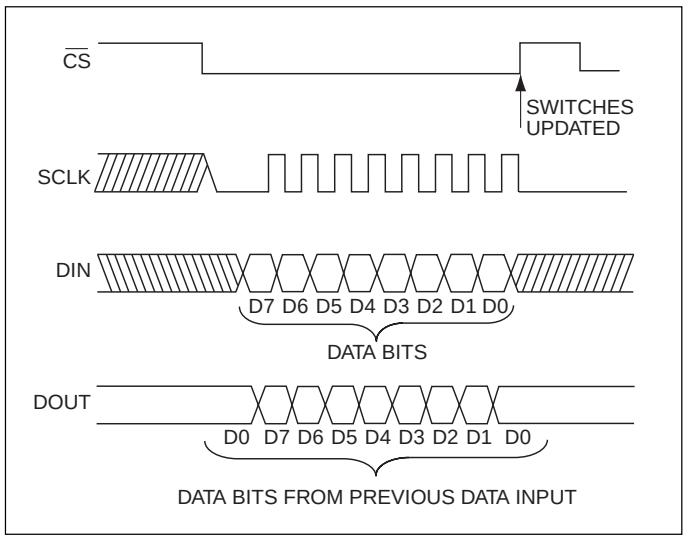

Figure 7. Three-Wire Interface Timing

Addressable Serial Interface

When several serial devices are configured as slaves, addressable by the processor, DIN pins of each decode logic individually control $\overline{CS}$ of each slave device. When a slave is selected, its $\overline{CS}$ pin is driven low, data is shifted in, and $\overline{CS}$ is driven high to latch the data. Typically, only on slave is addressed at a time. DOUT is not used.

Applications Information

Multiplexers

The PS395 can be used as a multiplexer.

Single Supply

The PS395 operates from a single supply between +3V and +16V when V- is connected to GND. All of the bipolar precautions must be observed.

High-Frequency Performance

In 50Ω systems, signal response is reasonably flat up to 50MHz (see Typical Operating Characteristics). Above 20MHz, the on-response has several minor peaks that are highly layout dependent. The problem is not turning the switch on, but turning it off. The off-state switch acts like a capacitor and passes higher frequencies with less attenuation. At 10MHz, off isolation is about -45dB in 50Ω systems, becoming worse (approximately 20dB per decade) as frequency increases. Higher circuit impedances also make off isolation worse. Adjacent channel attenuation is about 3dB above that of a bare IC socket, and is due entirely to capacitive coupling.

Part	Temperature Range	Pin-Package
PS395CNB	0°C to +70°C	24 Narrow Plastic Dip
PS395CWG	0°C to +70°C	24 Wide SO
PS395ENG	–40°C to +850°C	24 Narrow Plastic Dip
PS395EWG	–40°C to +850°C	24 Wide SO