DATA SHEET

PCF8578
LCD row/column driver for dot matrix graphic displays

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PHILIPS

CONTENTS

LCD row/column driver for dot matrix graphic displays

PCF8578

1 FEATURES

- Single chip LCD controller/driver
- Stand-alone or may be used with up to 32 PCF8579s (40960 dots possible)
- 40 driver outputs, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns
- Selectable multiplex rates; 1 : 8, 1 : 16, 1 : 24 or 1 : 32
- Externally selectable bias configuration, 5 or 6 levels
- 1280-bit RAM for display data storage and scratch pad
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8579)
- Provides display synchronization for PCF8579
- On-chip oscillator, requires only 1 external resistor
- Power-on reset blanks display
- Logic voltage supply range 2.5 to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I^2C-bus interface
- TTL/CMOS compatible
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8579)
- Space saving 56-lead plastic mini-pack and 64 pin quad flat pack
- Compatible with chip-on-glass technology.

2 APPLICATIONS

- Automotive information systems
- Telecommunication systems
- Point-of-sale terminals
- Computer terminals
- Instrumentation.

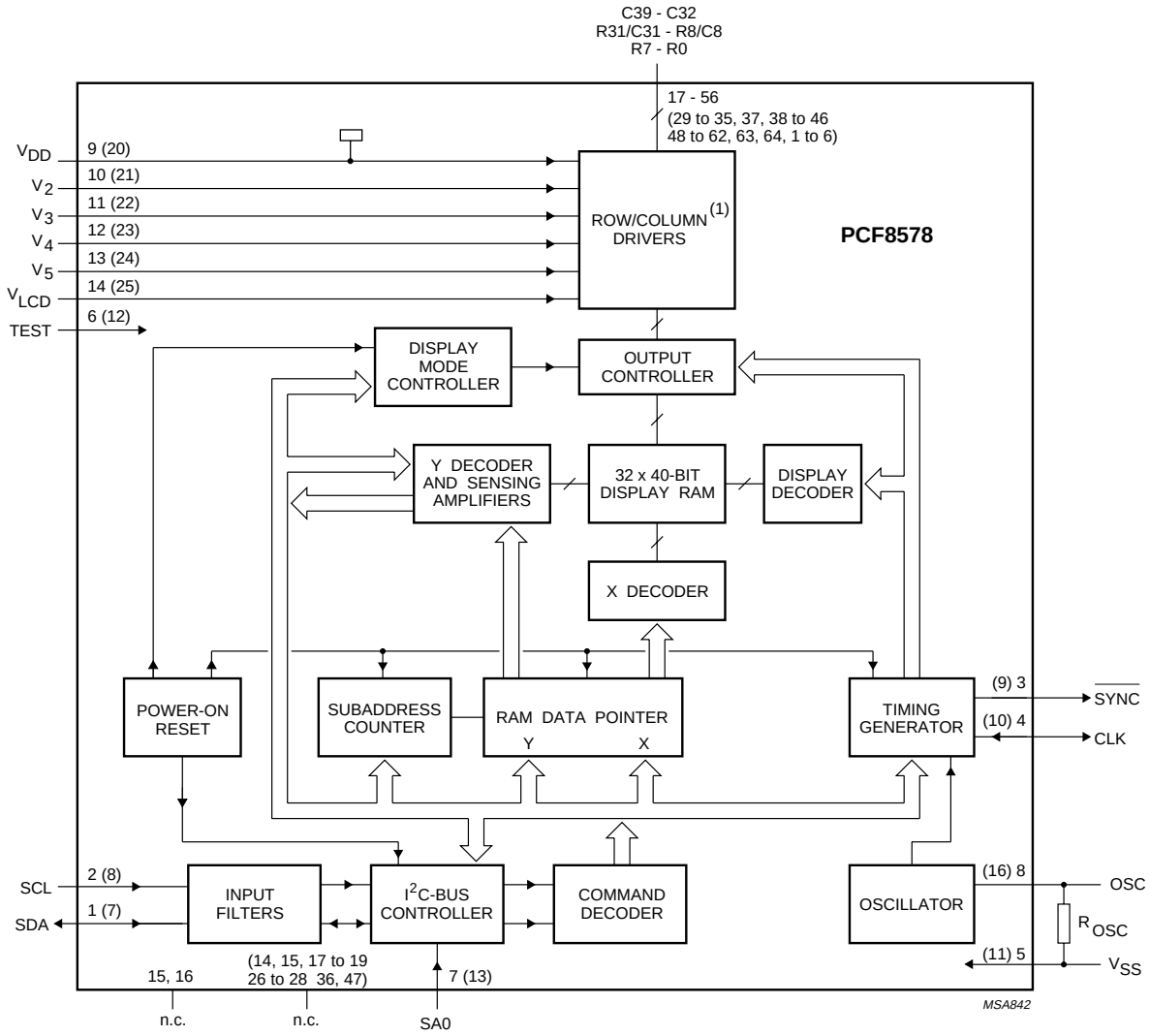
3 GENERAL DESCRIPTION

The PCF8578 is a low power CMOS LCD row/column driver, designed to drive dot matrix graphic displays at multiplex rates of 1 : 8, 1 : 16, 1 : 24 or 1 : 32. The device has 40 outputs, of which 24 are programmable, configurable as $^{32}/_{8}$, $^{24}/_{16}$, $^{16}/_{24}$ or $^{8}/_{32}$ rows/columns. The PCF8578 can function as a stand-alone LCD controller/driver for use in small systems, or for larger systems can be used in conjunction with up to 32 PCF8579s for which it has been optimized. Together these two devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8578 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I^2C-bus). Communication overheads are minimized by a display RAM with auto-incremented addressing and display bank switching.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCF8578T	VSO56	plastic very small outline package; 56 leads	SOT190-1
PCF8578U/2	–	chip with bumps in tray	–
PCF8578H	LQFP64	plastic low profile quad flat package; 64 leads; body $10 \times 10 \times 1.4$ mm	SOT314-2

5 BLOCK DIAGRAM



(1) Operates at LCD voltage levels, all other blocks operate at logic levels.
The pin numbers given in parenthesis refer to the LQFP64 package.

Fig.1 Block diagram.

6 PINNING

SYMBOL	PIN		DESCRIPTION
	VSO56	LQFP64	
SDA	1	7	I^2C-bus serial data input/output
SCL	2	8	I^2C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization output
CLK	4	10	external clock input/output
V_{SS}	5	11	ground (logic)
TEST	6	12	test pin (connect to V_{SS})
SA0	7	13	I^2C-bus slave address input (bit 0)
OSC	8	16	oscillator input
V_{DD}	9	20	positive supply voltage
V_2 to V_5	10 to 13	21 to 24	LCD bias voltage inputs
V_{LCD}	14	25	LCD supply voltage
n.c.	15, 16	14, 15, 17 to 19, 26 to 28, 36, 47	not connected
C39 to C32	17 to 24	29 to 35, 37	LCD column driver outputs
R31/C31 to R8/C8	25 to 48	38 to 46, 48 to 62	LCD row/column driver outputs
R7 to R0	49 to 56	63, 64, 1 to 6	LCD row driver outputs

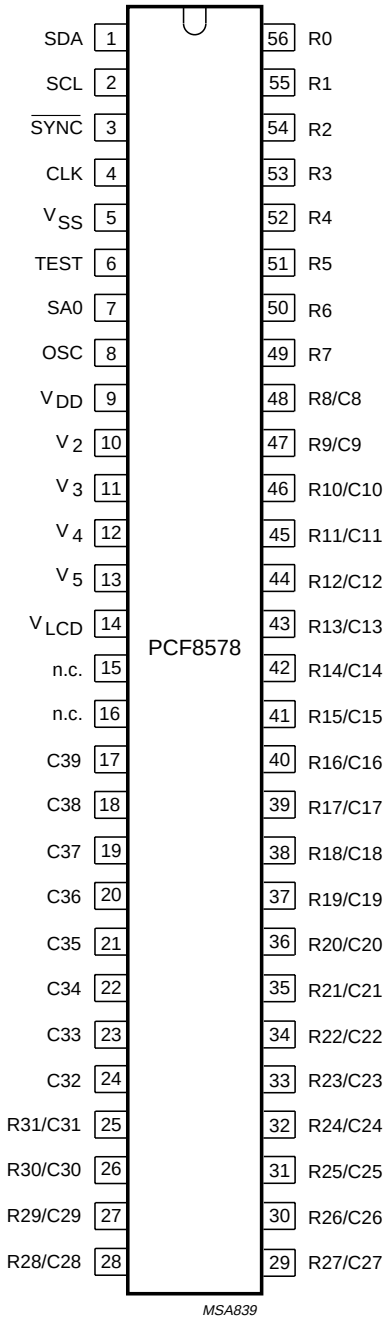


Fig.2 Pin configuration (VSO56).

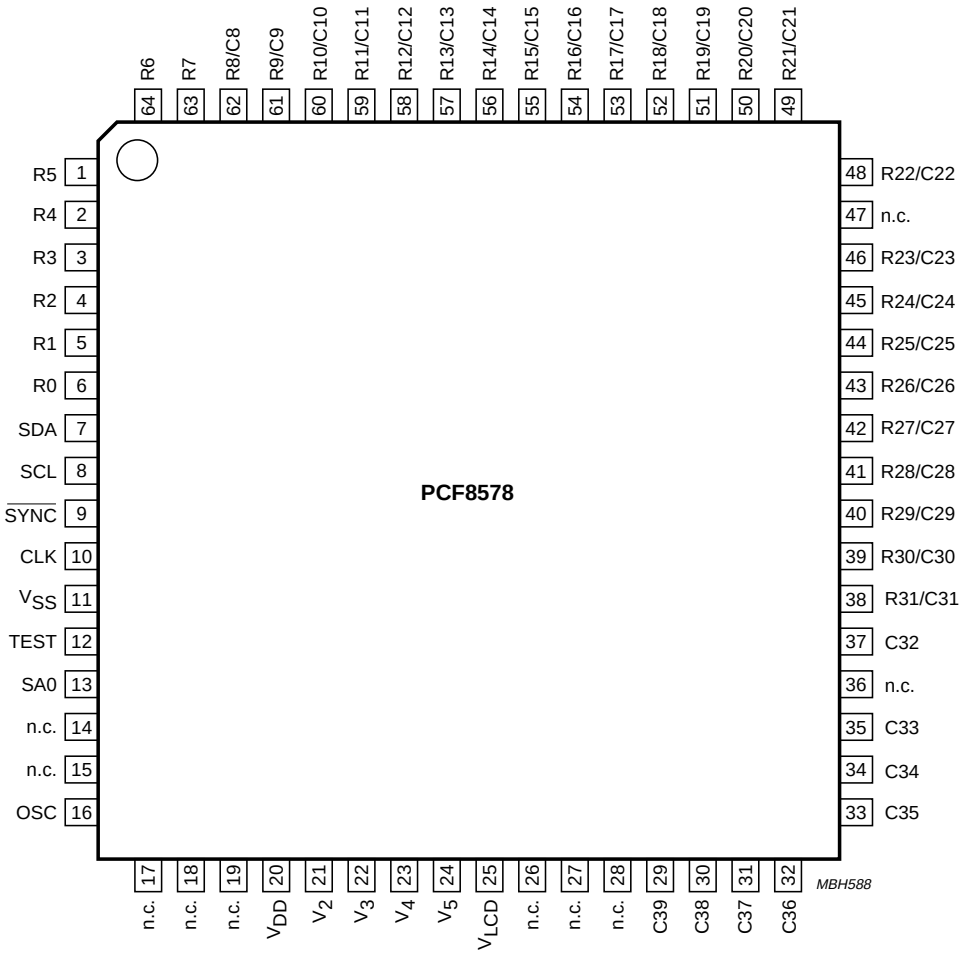


Fig.3 Pin configuration (LQFP64).

7 FUNCTIONAL DESCRIPTION

The PCF8578 row/column driver is designed for use in one of three ways:

- Stand-alone row/column driver for small displays (mixed mode)
- Row/column driver with cascaded PCF8579s (mixed mode)
- Row driver with cascaded PCF8579s (mixed mode).

7.1 Mixed mode

In mixed mode, the device functions as both a row and column driver. It can be used in small stand-alone applications, or for larger displays with up to 15 PCF8579s (31 PCF8579s when two slave addresses are used). See Table 1 for common display configurations.

7.2 Row mode

In row mode, the device functions as a row driver with up to 32 row outputs and provides the clock and synchronization signals for the PCF8579. Up to 16 PCF8579s can normally be cascaded (32 when two slave addresses are used).

Timing signals are derived from the on-chip oscillator, whose frequency is determined by the value of the resistor connected between OSC and V_{SS}.

Commands sent on the I^2C-bus from the host microcontroller set the mode (row or mixed), configuration (multiplex rate and number of rows and columns) and control the operation of the device. The device may have one of two slave addresses. The only difference between these slave addresses is the least significant bit, which is set by the logic level applied to SA0. The PCF8578 and PCF8579 also have subaddresses. The subaddress of the PCF8578 is only defined in mixed mode and is fixed at 0. The RAM may only be accessed in mixed mode and data is loaded as described for the PCF8579.

Bias levels may be generated by an external potential divider with appropriate decoupling capacitors. For large displays, bias sources with high drive capability should be used. A typical mixed mode system operating with up to 15 PCF8579s is shown in Fig.5 (a stand-alone system would be identical but without the PCF8579s).

Table 1 Possible displays configurations

APPLICATION	MULTIPLEX RATE	MIXED MODE		ROW MODE		TYPICAL APPLICATIONS
		ROWS	COLUMNS	ROWS	COLUMNS	
Stand alone	1 : 8	8	32	–	–	small digital or alphanumerical displays
	1 : 16	16	24	–	–	
	1 : 24	24	16	–	–	
	1 : 32	32	8	–	–	
With PCF8579	1 : 8	8[1]	632[1]	8×4 4[2]	640[2]	alphanumeric displays and dot matrix graphic displays
	1 : 16	16[1]	624[1]	16×2[2]	640[2]	
	1 : 24	24[1]	616[1]	24[2]	640[2]	
	1 : 32	32[1]	608[1]	24[2]	640[2]	

Notes

1. Using 15 PCF8579s.
2. Using 16 PCF8579s.

7.3 Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10% contrast. Table 2 shows the optimum voltage bias levels for the PCF8578 as functions of V_{op} ($V_{op} = V_{DD} - V_{LCD}$), together with the discrimination ratios (D) for the different multiplex rates. A practical value for V_{op} is obtained by equating $V_{off(rms)}$ with V_{th}. Figure 4 shows the first 4 rows of Table 2 as graphs. Table 3 shows the relative values of the resistors required in the configuration of Fig.5 to produce the standard multiplex rates.

Table 2 Optimum LCD voltages

PARAMETER	MULTIPLEX RATE			
	1 : 8	1 : 16	1 : 24	1 : 32
$\frac{V_2}{V_{op}}$	0.739	0.800	0.830	0.850
$\frac{V_3}{V_{op}}$	0.522	0.600	0.661	0.700
$\frac{V_4}{V_{op}}$	0.478	0.400	0.339	0.300
$\frac{V_5}{V_{op}}$	0.261	0.200	0.170	0.150
$\frac{V_{off(rms)}}{V_{op}}$	0.297	0.245	0.214	0.193
$\frac{V_{on(rms)}}{V_{op}}$	0.430	0.316	0.263	0.230
$D = \frac{V_{on(rms)}}{V_{off(rms)}}$	1.447	1.291	1.230	1.196
$\frac{V_{op}}{V_{th}}$	3.370	4.080	4.680	5.190

Table 3 Multiplex rates and resistor values for Fig.5

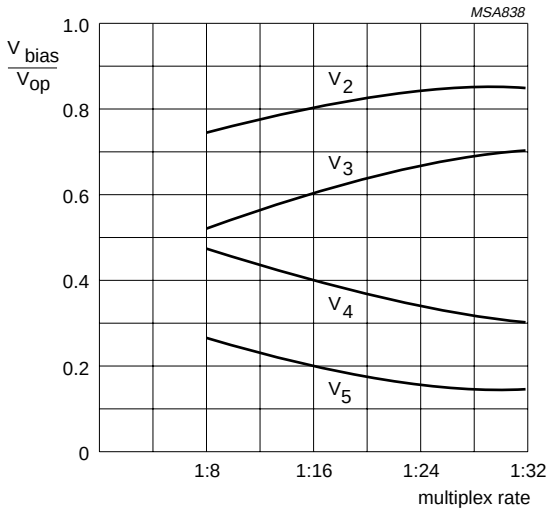
RESISTORS	MULTIPLEX RATE (n)	
	n = 8	n = 16, 24, 32
R1	R	R
R2	$(\sqrt{n-2})$ R	R
R3	$(3-\sqrt{n})$ R	$(\sqrt{n-3})$ R

7.4 Power-on reset

At power-on the PCF8578 resets to a defined starting condition as follows:

1. Display blank
2. 1 : 32 multiplex rate, row mode
3. Start bank, 0 selected
4. Data pointer is set to X, Y address 0, 0
5. Character mode
6. Subaddress counter is set to 0
7. I^2C-bus interface is initialized.

Data transfers on the I^2C-bus should be avoided for 1 ms following power-on, to allow completion of the reset action.



$V_{bias} = V_2, V_3, V_4, V_5$. See Table 2.

Fig.4 V_{bias}/V_{op} as a function of the multiplex rate.

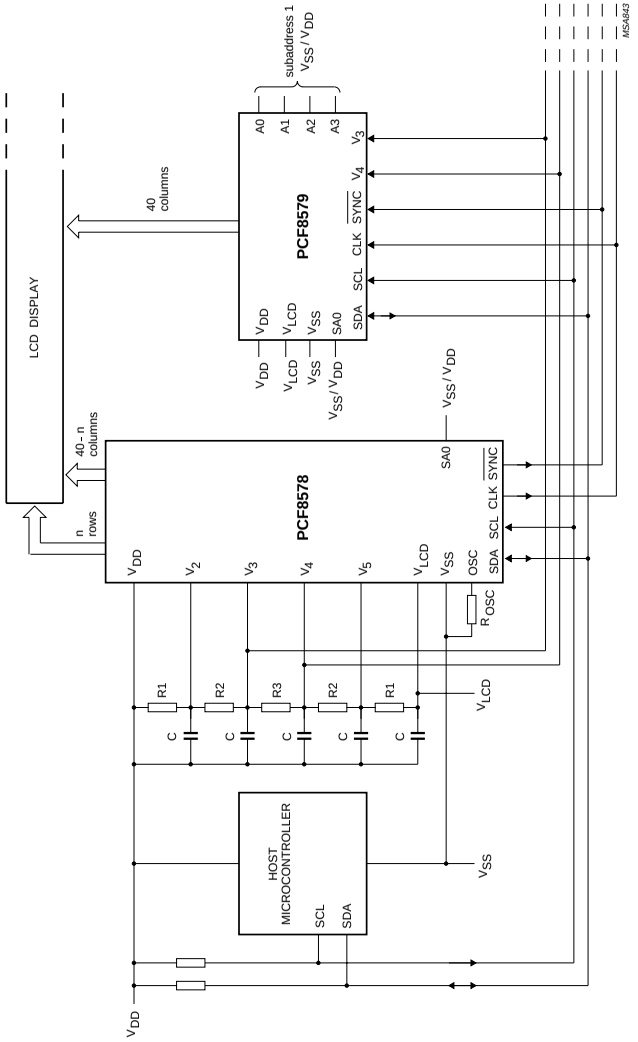


Fig.5 Typical mixed mode configuration.

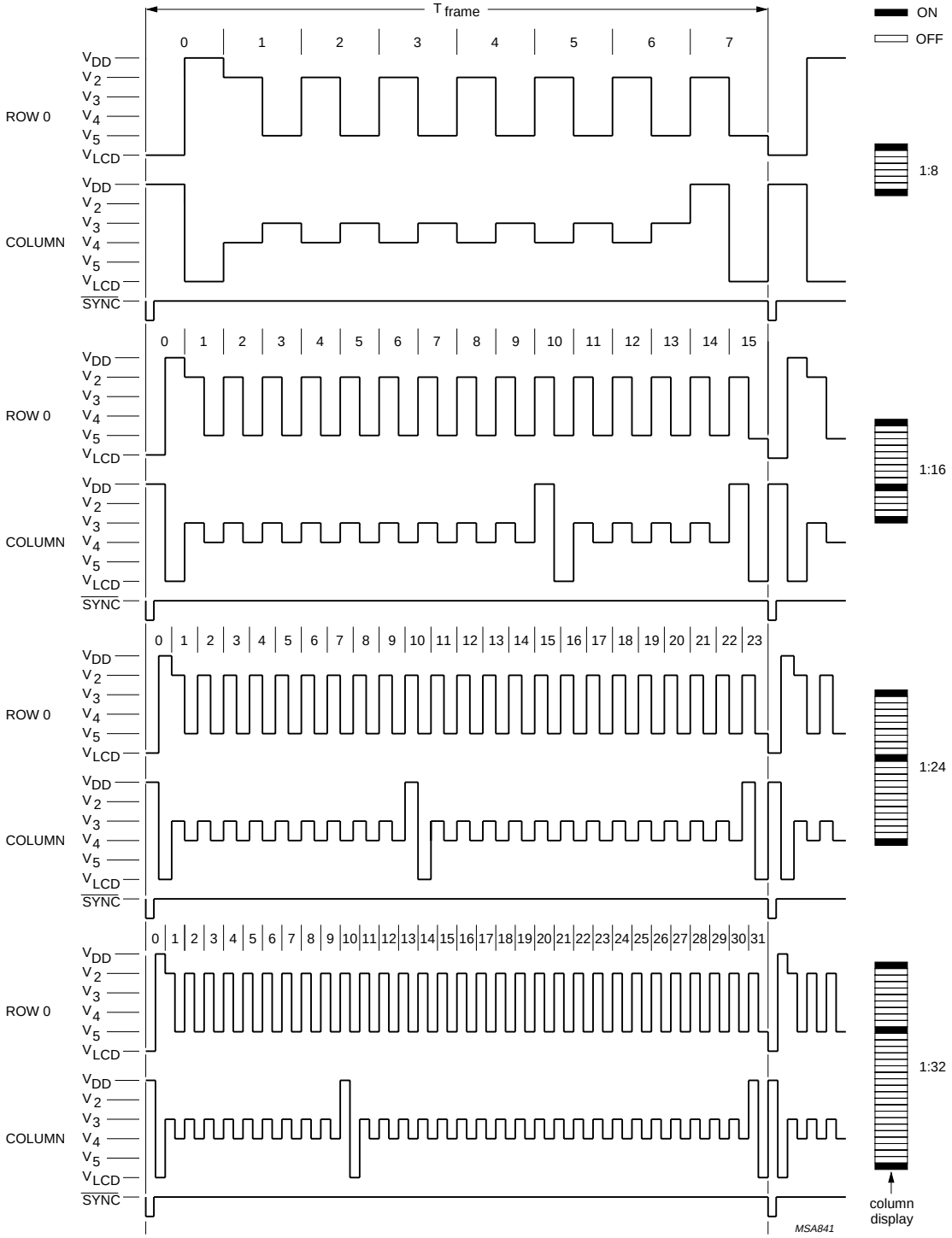
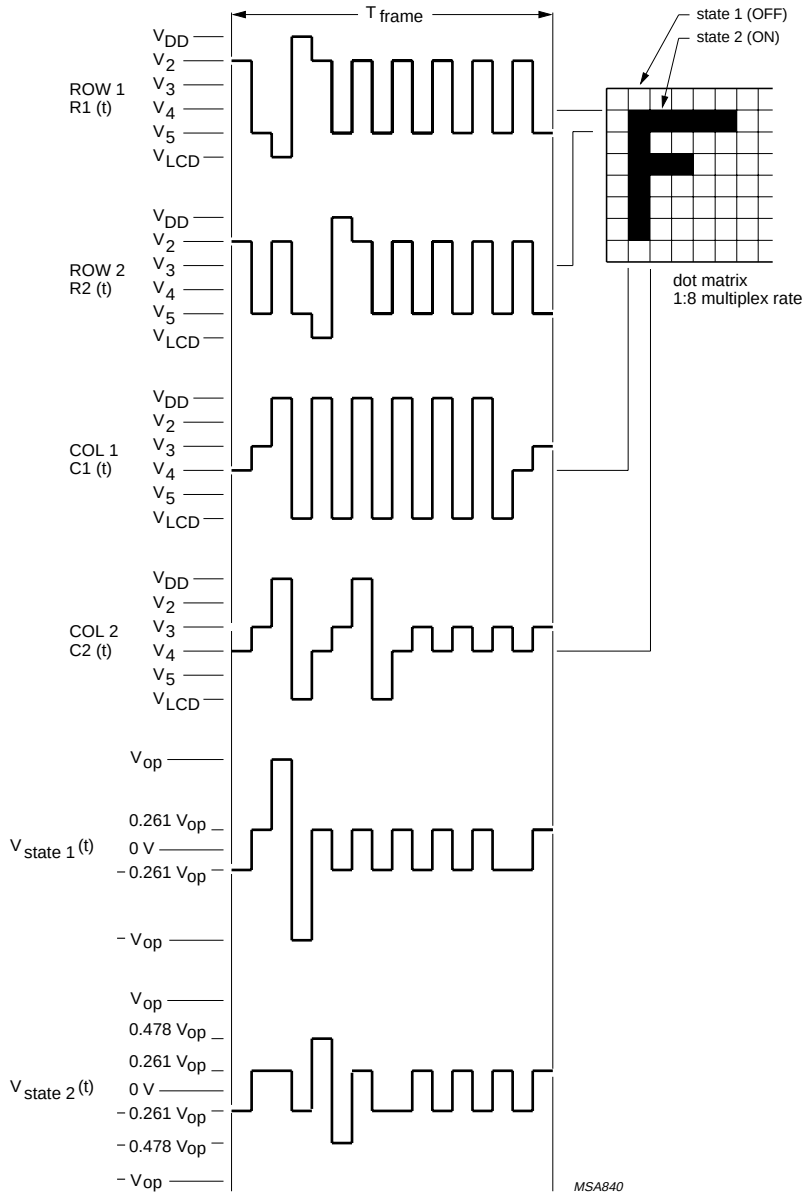


Fig.6 LCD row/column waveforms.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

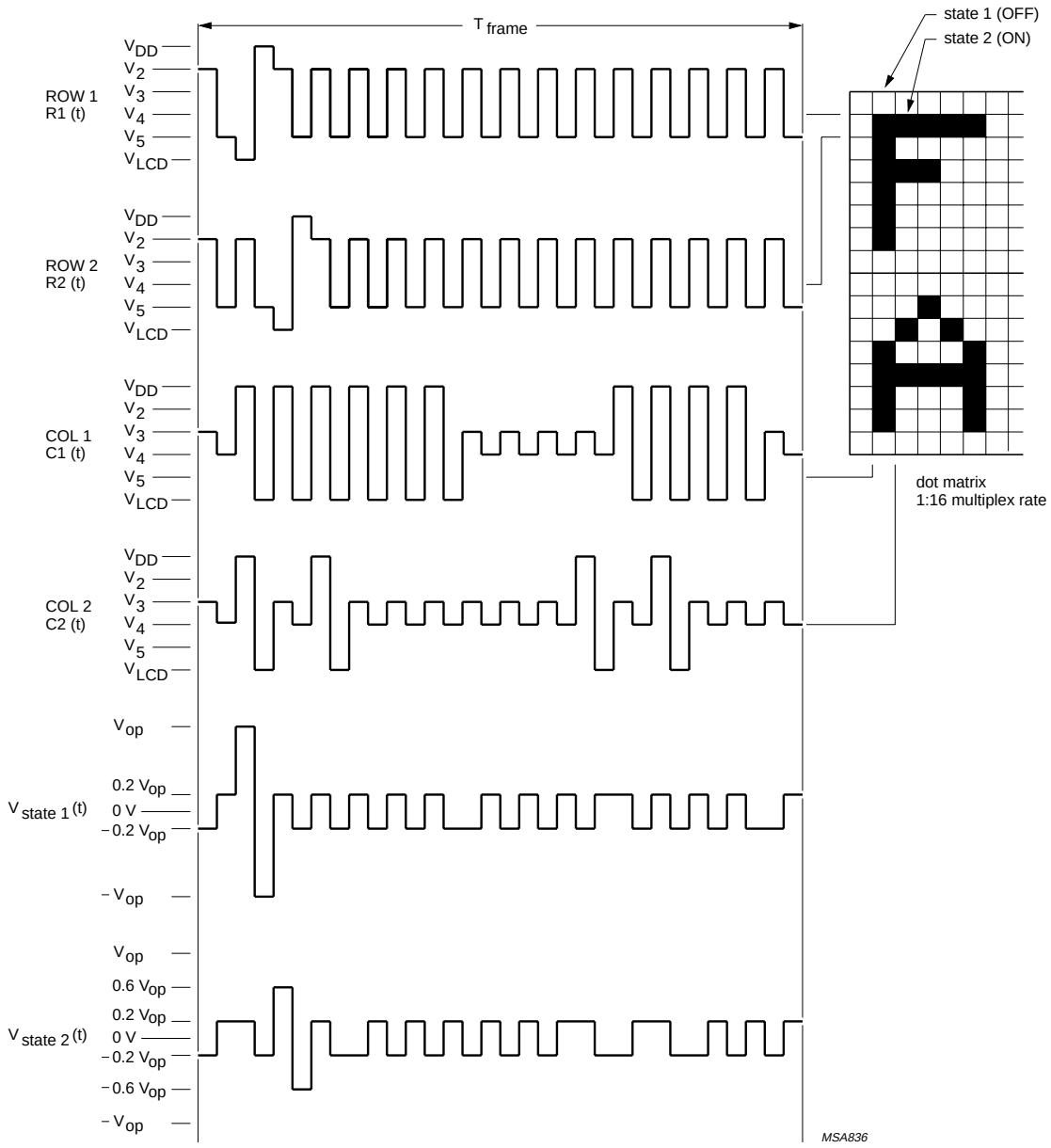
$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

general relationship (n = multiplex rate)

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.7 LCD drive mode waveforms for 1 : 8 multiplex rate.



$V_{state\ 1}(t) = C1(t) - R1(t)$:

$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16}-1}{16(\sqrt{16}+1)}} = 0.316$$

$V_{state\ 2}(t) = C2(t) - R2(t)$:

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{16}-1)}{\sqrt{16}(\sqrt{16}+1)^2}} = 0.254$$

general relationship (n = multiplex rate)

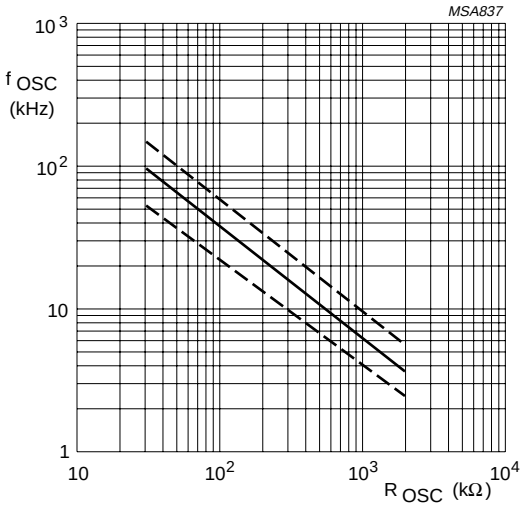
$$\frac{V_{on(rms)}}{V_{op}} = \sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}}$$

$$\frac{V_{off(rms)}}{V_{op}} = \sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}}$$

Fig.8 LCD drive mode waveforms for 1 : 16 multiplex rate.

7.5 Internal clock

The clock signal for the system may be generated by the internal oscillator and prescaler. The frequency is determined by the value of the resistor R_{OSC}, see Fig.9. For normal use a value of 330 kΩ is recommended. The clock signal, for cascaded PCF8579s, is output at CLK and has a frequency $\frac{1}{6}$ (multiplex rate 1 : 8, 1 : 16 and 1 : 32) or $\frac{1}{8}$ (multiplex rate 1 : 24) of the oscillator frequency.



To avoid capacitive coupling, which could adversely affect oscillator stability, R_{OSC} should be placed as closely as possible to the OSC pin. If this proves to be a problem, a filtering capacitor may be connected in parallel to R_{OSC}.

Fig.9 Oscillator frequency as a function of external oscillator resistor, R_{OSC}.

7.6 External clock

If an external clock is used, OSC must be connected to V_{DD} and the external clock signal to CLK. Table 4 summarizes the nominal CLK and $\overline{SYNC}$ frequencies.

7.7 Timing generator

The timing generator of the PCF8578 organizes the internal data flow of the device and generates the LCD frame synchronization pulse $\overline{SYNC}$, whose period is an integer multiple of the clock period. In cascaded applications, this signal maintains the correct timing relationship between the PCF8578 and PCF8579s in the system.

7.8 Row/column drivers

Outputs R0 to R7 and C32 to C39 are fixed as row and column drivers respectively. The remaining 24 outputs R8/C8 to R31/C31 are programmable and may be configured (in blocks of 8) to be either row or column drivers. The row select signal is produced sequentially at each output from R0 up to the number defined by the multiplex rate (see Table 1). In mixed mode the remaining outputs are configured as columns. In row mode all programmable outputs (R8/C8 to R31/C31) are defined as row drivers and the outputs C32 to C39 should be left open-circuit.

Using a 1 : 16 multiplex rate, two sets of row outputs are driven, thus facilitating split-screen configurations, i.e. a row select pulse appears simultaneously at R0 and R16/C16, R1 and R17/C17 etc. Similarly, using a multiplex rate of 1 : 8, four sets of row outputs are driven simultaneously. Driver outputs must be connected directly to the LCD. Unused outputs should be left open-circuit. In 1 : 8 R0 to R7 are rows; in 1 : 16 R0 to R15/C15 are rows; in 1 : 24 R0 to R23/C23 are rows; in 1 : 32 R0 to R31/C31 are rows.

Table 4 Signal frequencies required for nominal 64 Hz frame frequency; note 1.

OSCILLATOR FREQUENCY f_{OSC}(2) (Hz)	FRAME FREQUENCY $f_{\overline{SYNC}}$ (Hz)	MULTIPLEX RATE (n)	DIVISION RATIO	CLOCK FREQUENCY f_{CLK} (Hz)
12288	64	1 : 8, 1 : 16, 1 : 32	6	2048
12288	64	1 : 24	8	1536

Notes

1. A clock signal must always be present, otherwise the LCD may be frozen in a DC state.
2. R_{OSC} = 330 kΩ.

7.9 Display mode controller

The configuration of the outputs (row or column) and the selection of the appropriate driver waveforms are controlled by the display mode controller.

7.10 Display RAM

The PCF8578 contains a 32 x 40-bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes (4 x 8 x 40 bits). During RAM access, data is transferred to/from the RAM via the I^2C-bus. The first eight columns of data (0 to 7) cannot be displayed but are available for general data storage and provide compatibility with the PCF8579. There is a direct correspondence between X-address and column output number.

7.11 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^2C-bus.

7.12 Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage takes place only when the contents of the subaddress counter agree with the hardware subaddress. The hardware subaddress of the PCF8578, valid in mixed mode only, is fixed at 0000.

7.13 I^2C-bus controller

The I^2C-bus controller detects the I^2C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8578 acts as an I^2C-bus slave transmitter/receiver in mixed mode, and as a slave receiver in row mode. A slave device cannot control bus communication.

7.14 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.15 RAM access

RAM operations are only possible when the PCF8578 is in mixed mode.

In this event its hardware subaddress is internally fixed at 0000 and the hardware subaddresses of any PCF8579 used in conjunction with the PCF8578 must start at 0001.

There are three RAM ACCESS modes:

- Character
- Half-graphic
- Full-graphic.

These modes are specified by bits G1 to G0 of the RAM ACCESS command. The RAM ACCESS command controls the order in which data is written to or read from the RAM (see Fig.10).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Fig.11):

- Device subaddress (specified by the DEVICE SELECT command)
- RAM X-address (specified by the LOAD X-ADDRESS command)
- RAM bank (specified by bits Y1 and Y0 of the RAM ACCESS command).

Subsequent data bytes will be written or read according to the chosen RAM ACCESS mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.

7.16 Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M1 and M0 of the SET MODE command.

The display status (all dots on/off and normal/inverse video) is set by bits E1 and E0 of the SET MODE command. For bank switching, the RAM bank corresponding to the top of the display is set by bits B1 and B0 of the SET START BANK command. This is shown in Fig.12. This feature is useful when scrolling in alphanumeric applications.

7.17 TEST pin

The TEST pin must be connected to V_{SS}.

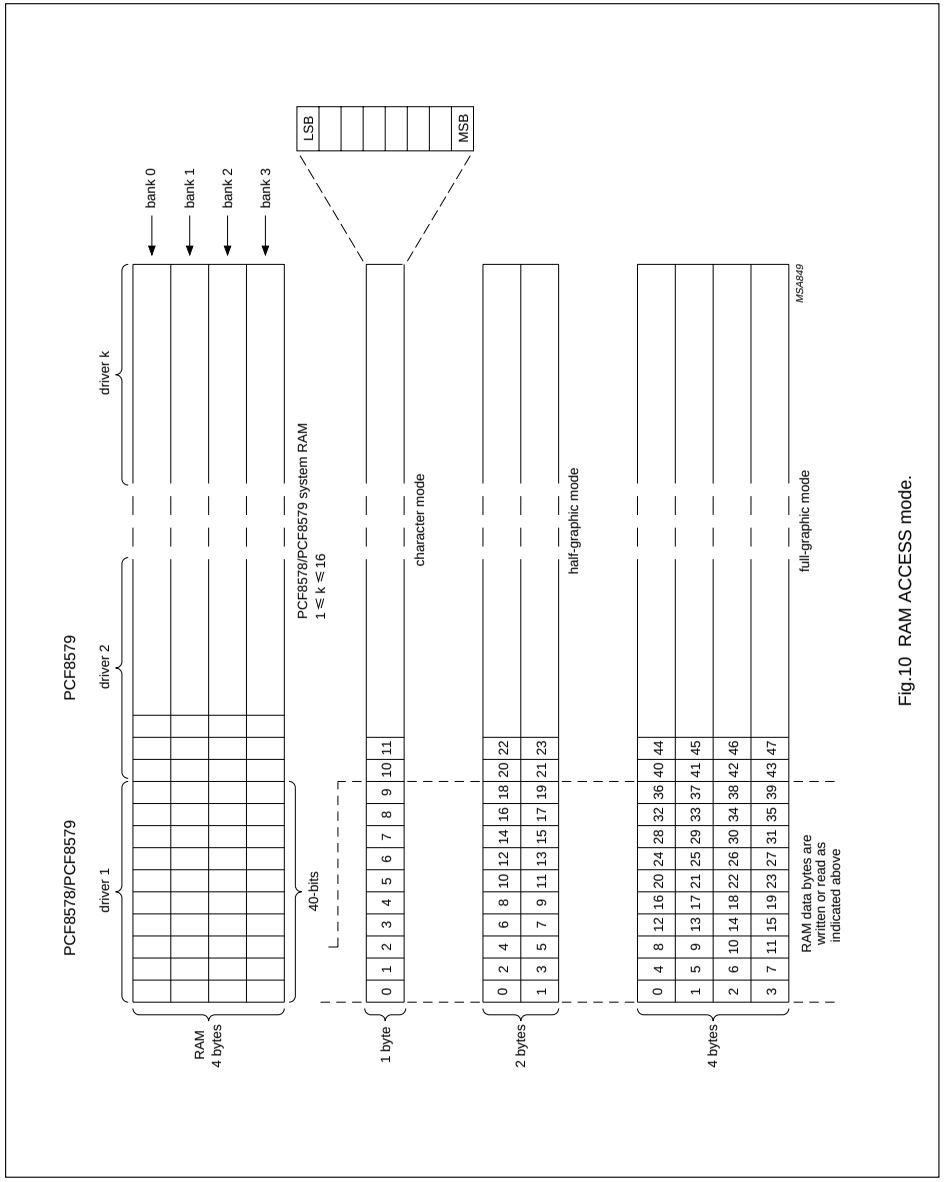


Fig.10 RAM ACCESS mode.

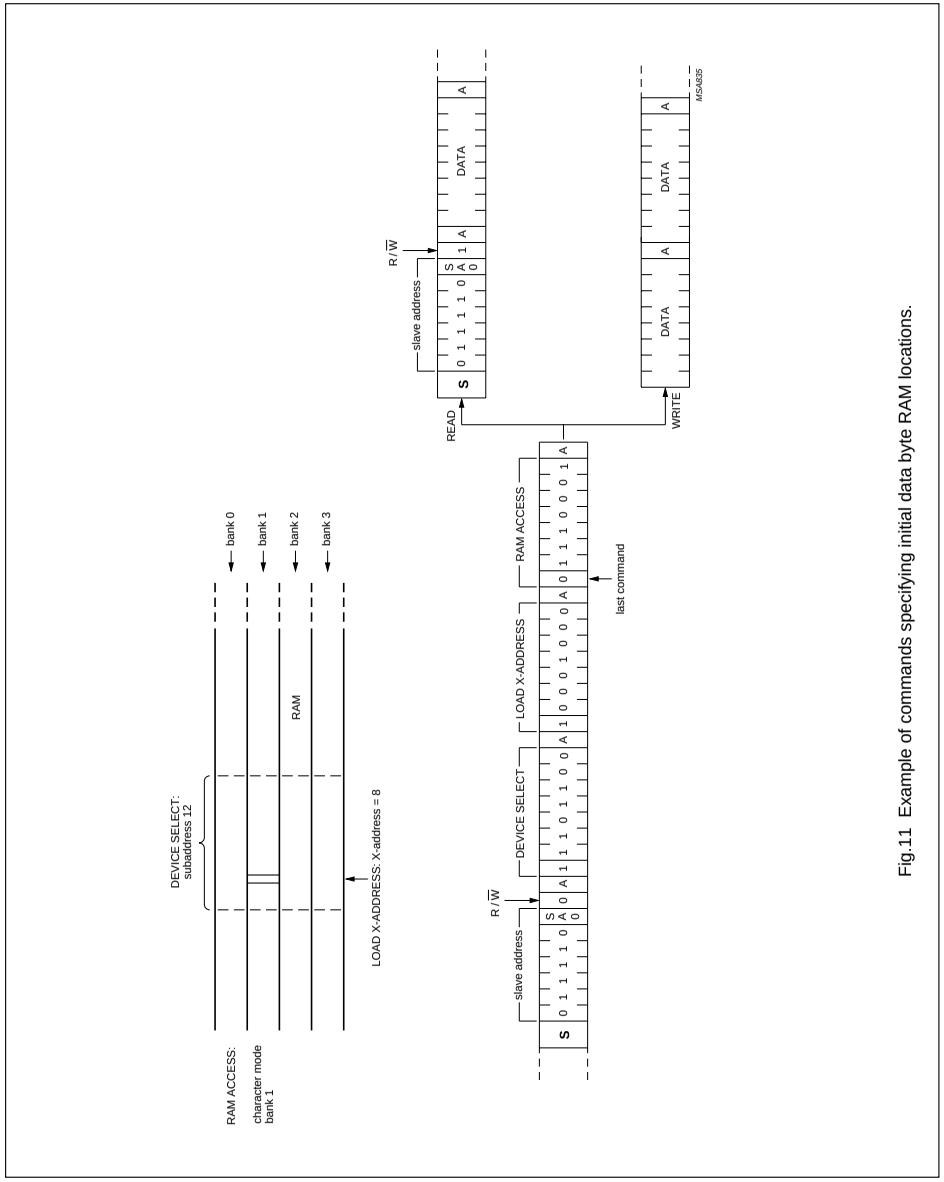


Fig.11 Example of commands specifying initial data byte RAM locations.

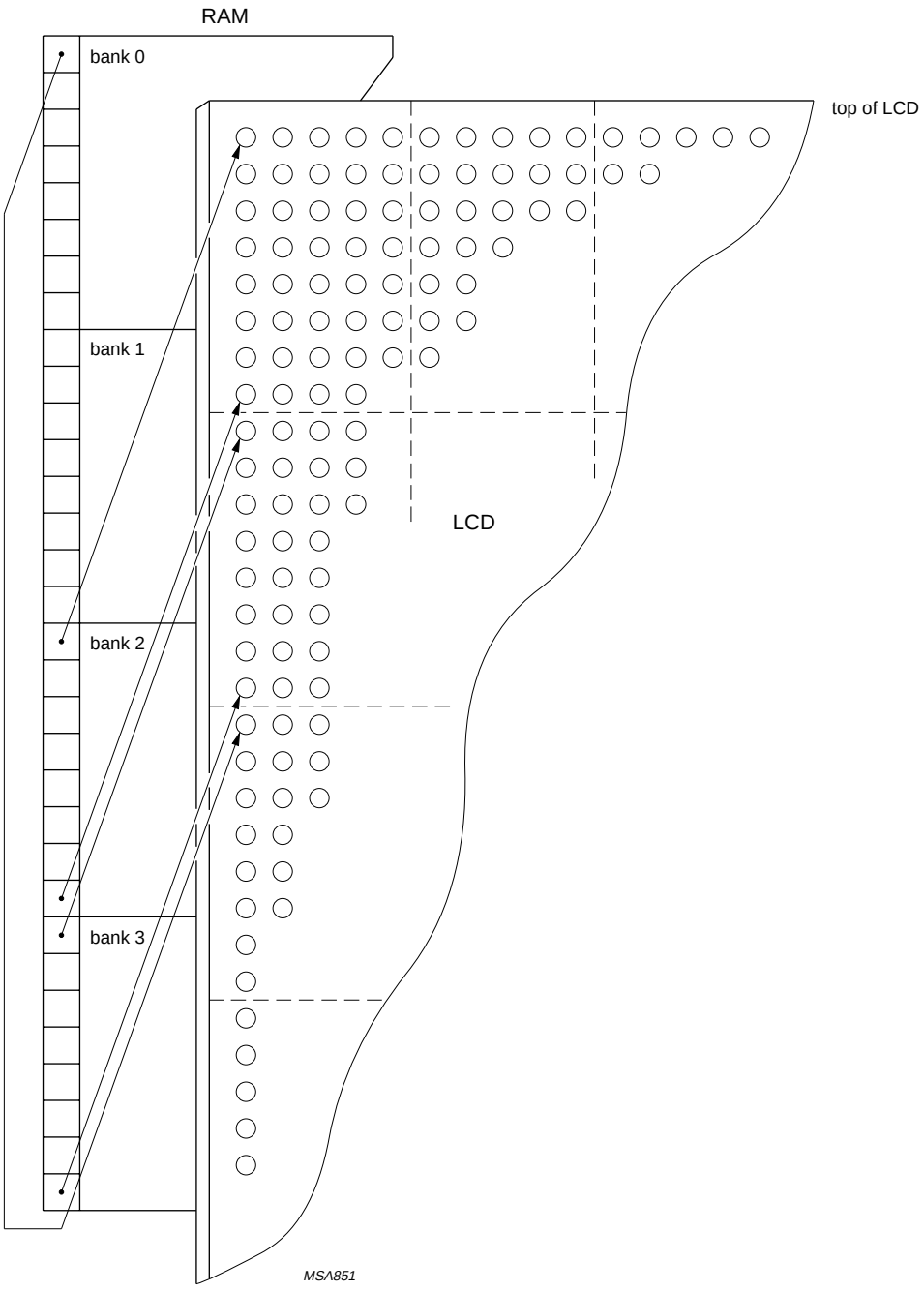


Fig.12 Relationship between display and SET START BANK; 1 : 32 multiplex rate and start bank = 2.

8 I²C-BUS PROTOCOL

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least significant bit of the slave address is set by connecting input SA0 to either 0 (V_{SS}) or 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I²C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I²C-bus for very large applications
2. The use of two types of LCD multiplex schemes on the same I²C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

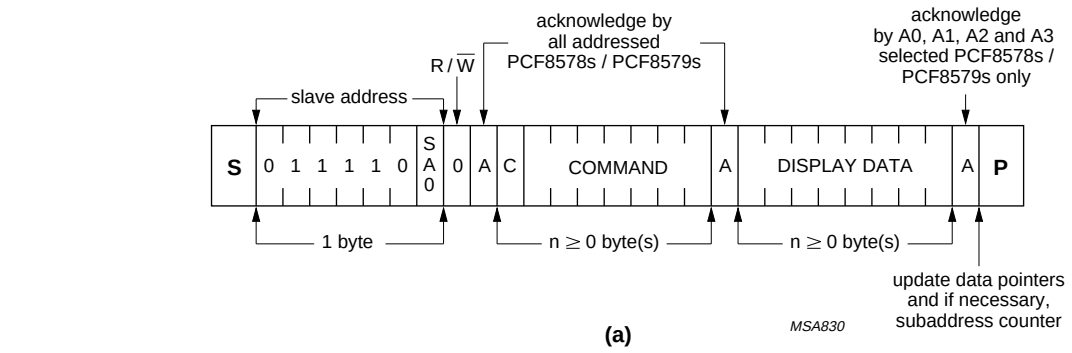
The I²C-bus protocol is shown in Fig.13.
All communications are initiated with a start condition (S) from the I²C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus.
The last command must clear the continuation bit C.
After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I²C-bus master issues a stop condition (P).

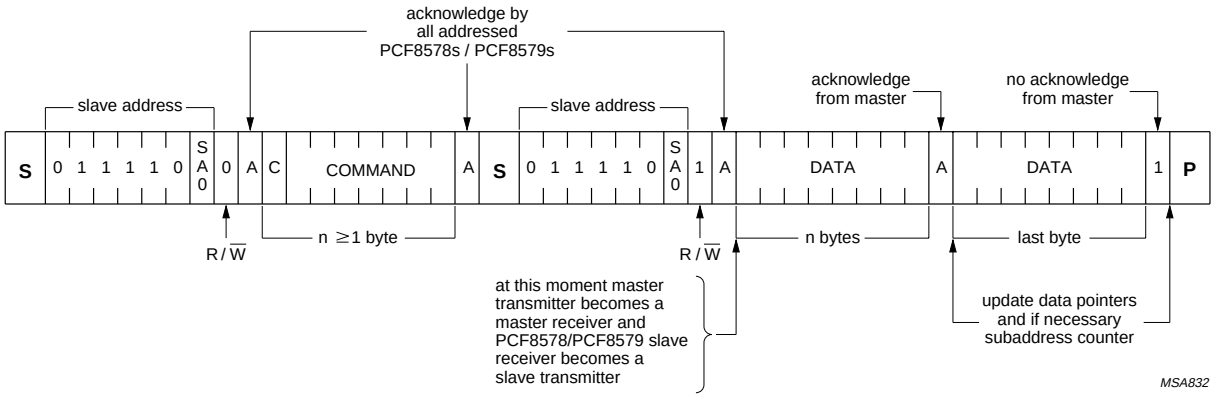
In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8578 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by not generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a stop condition (P).

Display bytes are written into, or read from, the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from, the intended devices.

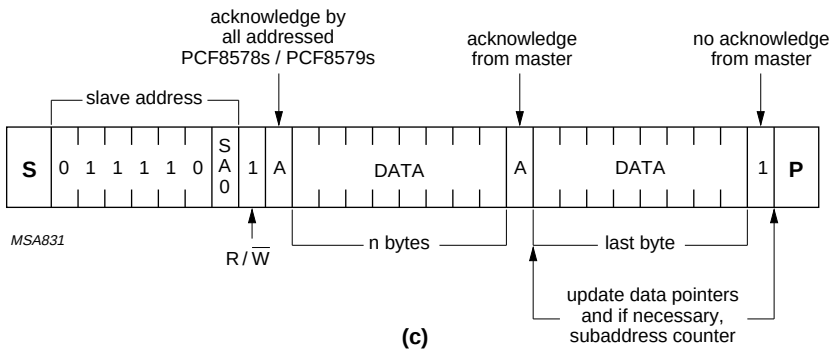
In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.



(a)



(b)



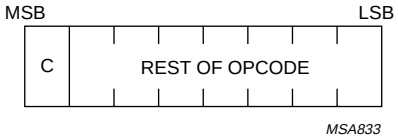
(c)

Fig.13 (a) Master transmits to slave receiver (WRITE mode); (b) Master reads after sending command string (WRITE commands; READ data); (c) Master reads slave immediately after sending slave address (READ mode).

8.1 Command decoder

The command decoder identifies command bytes that arrive on the I^2C-bus. The most-significant bit of a command is the continuation bit C (see Fig.14). When this bit is set, it indicates that the next byte to be transferred will also be a command. If the bit is reset, it indicates the conclusion of the command transfer. Further bytes will be regarded as display data. Commands are transferred in WRITE mode only.

The five commands available to the PCF8578 are defined in Tables 5 and 6.



C = 0; last command.
C = 1; commands continue.

Fig.14 General information of command byte.

Table 5 Summary of commands

COMMAND	OPCODE(1)								DESCRIPTION
SET MODE	C	1	0	D	D	D	D	D	multiplex rate, display status, system type
SET START BANK	C	1	1	1	1	1	D	D	defines bank at top of LCD
DEVICE SELECT	C	1	1	0	D	D	D	D	defines device subaddress
RAM ACCESS	C	1	1	1	D	D	D	D	graphic mode, bank select (D D D D ≥ 12 is not allowed; see SET START BANK opcode)
LOAD X-ADDRESS	C	0	D	D	D	D	D	D	0 to 39

Note

1. C = command continuation bit. D = may be a logic 1 or 0.

Table 6 Definition of PCF8578/PCF8579 commands

COMMAND	OPCODE								OPTIONS	DESCRIPTION
SET MODE	C	1	0	T	E1	E0	M1	M0	see Table 7	defines LCD drive mode
									see Table 8	defines display status
									see Table 9	defines system type
SET START BANK	C	1	1	1	1	1	B1	B0	see Table 10	defines pointer to RAM bank corresponding to the top of the LCD; useful for scrolling, pseudo-motion and background preparation of new display
DEVICE SELECT	C	1	1	0	A3	A2	A1	A0	see Table 11	four bits of immediate data, bits A0 to A3, are transferred to the subaddress counter to define one of sixteen hardware subaddresses
RAM ACCESS	C	1	1	1	G1	G0	Y1	Y0	see Table 12	defines the auto-increment behaviour of the address for RAM access
									see Table 13	two bits of immediate data, bits Y0 to Y1, are transferred to the X-address pointer to define one of forty display RAM columns
LOAD X-ADDRESS	C	0	X5	X4	X3	X2	X1	X0	see Table 14	six bits of immediate data, bits X0 to X5, are transferred to the X-address pointer to define one of forty display RAM columns

Table 7 Set mode option 1

LCD DRIVE MODE		BITS	
		M1	M0
1 : 8	MUX (8 rows)	0	1
1 : 16	MUX (16 rows)	1	0
1 : 24	MUX (24 rows)	1	1
1 : 32	MUX (32 rows)	0	0

Table 8 Set mode option 2

DISPLAY STATUS	BITS	
	E1	E0
Blank	0	0
Normal	0	1
All segments on	1	0
Inverse video	1	1

Table 9 Set mode option 3

SYSTEM TYPE	BIT T
PCF8578 row only	0
PCF8578 mixed mode	1

Table 10 Set start bank option 1

START BANK POINTER	BITS	
	B1	B0
Bank 0	0	0
Bank 1	0	1
Bank 2	1	0
Bank 3	1	1

Table 11 Device select option 1

DESCRIPTION	BITS			
Decimal value 0 to 15	A3	A2	A1	A0

Table 12 RAM access option 1

RAM ACCESS MODE	BITS	
	G1	G0
Character	0	0
Half-graphic	0	1
Full-graphic	1	0
Not allowed (note 1)	1	1

Note

1. See opcode for SET START BANK in Table 6.

Table 13 Device select option 1

DESCRIPTION	BITS	
Decimal value 0 to 3	Y1	Y0

Table 14 Device select option 1

DESCRIPTION	BITS					
Decimal value 0 to 39	X5	X4	X3	X2	X1	X0

9 CHARACTERISTICS OF THE I²C-BUS

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a serial data line (SDA) and a serial clock line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

9.1 Bit transfer

One data bit is transferred during each clock pulse.
The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

9.2 Start and stop conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S).
A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the STOP condition (P).

9.3 System configuration

A device transmitting a message is a 'transmitter', a device receiving a message is the 'receiver'. The device that controls the message flow is the 'master' and the devices which are controlled by the master are the 'slaves'.

9.4 Acknowledge

The number of data bytes transferred between the start and stop conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse.
A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a stop condition.

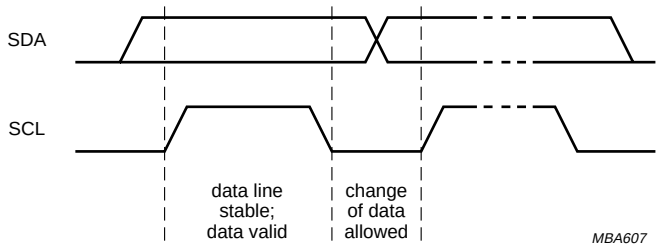


Fig.15 Bit transfer.

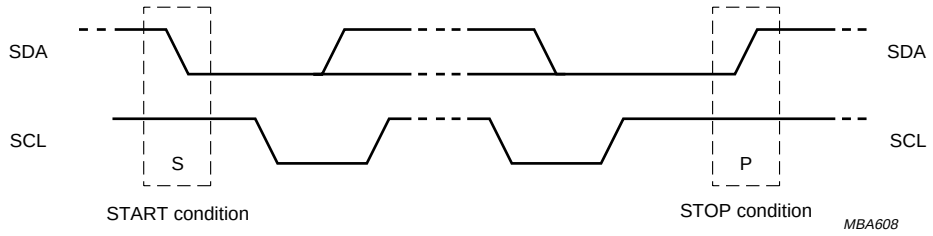


Fig.16 Definition of start and stop condition.

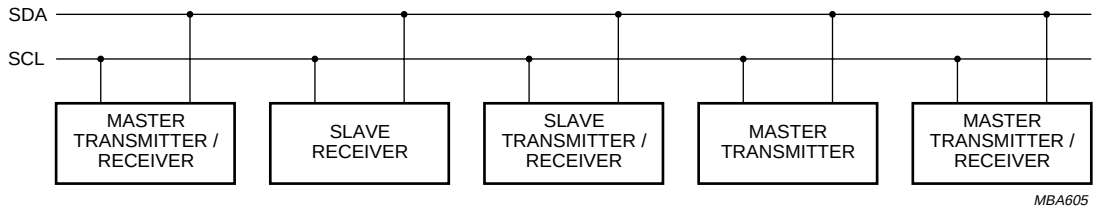
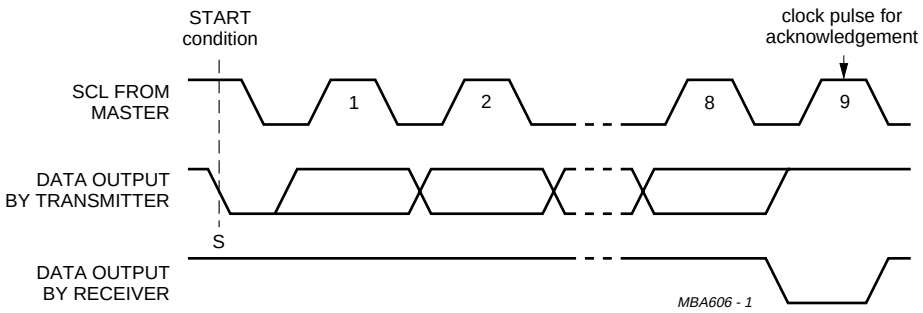


Fig.17 System configuration.



The general characteristics and detailed specification of the I^2C-bus are available on request.

Fig.18 Acknowledgement on the I^2C-bus.

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+8.0	V
V_{LCD}	LCD supply voltage	V_{DD} − 11	V_{DD}	V
V_{I1}	input voltage SDA, SCL, CLK, TEST, SA0 and OSC	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{I2}	input voltage V_2 to V_5	V_{LCD} − 0.5	V_{DD} + 0.5	V
V_{o1}	output voltage $\overline{SYNC}$ and CLK	V_{SS} − 0.5	V_{DD} + 0.5	V
V_{o2}	output voltage R0 to R7, R8/C8 to R31/C31 and C32 to C39	V_{LCD} − 0.5	V_{DD} + 0.5	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
I_{DD}, I_{SS}, I_{LCD}	V_{DD}, V_{SS} or V_{LCD} current	–50	+50	mA
P_{tot}	total power dissipation per package	–	400	mW
P_o	power dissipation per output	–	100	mW
T_{stg}	storage temperature	–65	+150	°C

11 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe it is desirable to take normal precautions appropriate to handling MOS devices. Advice can be found in Data Handbook IC12 under *“Handling MOS Devices”*.

12 DC CHARACTERISTICS

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage		2.5	–	6.0	V
V_{LCD}	LCD supply voltage		V_{DD} − 9	–	V_{DD} − 3.5	V
I_{DD1}	supply current external clock	f_{CLK} = 2 kHz; note 1	–	6	15	µA
I_{DD2}	supply current internal clock	R_{OSC} = 330 kΩ	–	20	50	µA
V_{POR}	power-on reset level	note 2	0.8	1.3	1.8	V
Logic						
V_{IL}	LOW level input voltage		V_{SS}	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{OL1}	LOW level output current at $\overline{SYNC}$ and CLK	V_{OL} = 1 V; V_{DD} = 5 V	1	–	–	mA
I_{OH1}	HIGH level output current at $\overline{SYNC}$ and CLK	V_{OH} = 4 V; V_{DD} = 5 V	–	–	−1	mA
I_{OL2}	LOW level output current at SDA	V_{OL} = 0.4 V; V_{DD} = 5 V	3	–	–	mA
I_{L1}	leakage current at SDA, SCL, $\overline{SYNC}$, CLK, TEST and SA0	V_i = V_{DD} or V_{SS}	–	–	+1	mA
I_{L2}	leakage current at OSC	V_i = V_{DD}	–	–	+1	µA
C_i	input capacitance at SCL and SDA	note 3	–	–	5	pF
LCD outputs						
I_{L3}	leakage current at V_2 to V_5	V_i = V_{DD} or V_{LCD}	−2	–	+2	µA
V_{DC}	DC component of LCD drivers R0 to R7, R8/C8 to R31/C31 and C32 to C39		–	±20	–	mV
R_{ROW}	output resistance R0 to R7 and R8/C8 to R31/C31	row mode; note 4	–	1.5	3	kΩ
R_{COL}	output resistance R8/C8 to R31/C31 and C32 to C39	column mode; note 4	–	3	6	kΩ

Notes

1. Outputs are open; inputs at V_{DD} or V_{SS}; I^2C-bus inactive; external clock with 50% duty factor.
2. Resets all logic when $V_{DD} < V_{POR}$.
3. Periodically sampled; not 100% tested.
4. Resistance measured between output terminal (R0 to R7, R8/C8 to R31/C31 and C32 to C39) and bias input (V_2 to V_5, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 2):
   a) V_{op} = V_{DD} − V_{LCD} = 9 V.
   b) Row mode, R0 to R7 and R8/C8 to R31/C31: $V_2 - V_{LCD} \geq 6.65$ V; $V_5 - V_{LCD} \leq 2.35$ V; I_{LOAD} = 150 µA.
   c) Column mode, R8/C8 to R31/C31 and C32 to C39: $V_3 - V_{LCD} \geq 4.70$ V; $V_4 - V_{LCD} \leq 4.30$ V; I_{LOAD} = 100 µA.

13 AC CHARACTERISTICS

All timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}.

V_{DD} = 2.5 to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 to +85 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{CLK1}	clock frequency at multiplex rates of 1 : 8, 1 : 16 and 1 : 32	R_{OSC} = 330 kΩ; V_{DD} = 6 V	1.2	2.1	3.3	kHz
f_{CLK2}	clock frequency at multiplex rates of 1 : 24	R_{OSC} = 330 kΩ; V_{DD} = 6 V	0.9	1.6	2.5	kHz
t_{PSYNC}	$\overline{SYNC}$ propagation delay		–	–	500	ns
t_{PLCD}	driver delays	V_{DD} − V_{LCD} = 9 V; with test loads	–	–	100	µs
I²C-bus						
f_{SCL}	SCL clock frequency		–	–	100	kHz
t_{SW}	tolerable spike width on bus		–	–	100	ns
t_{BUF}	bus free time		4.7	–	–	µs
$t_{SU;STA}$	start condition set-up time	repeated start codes only	4.7	–	–	µs
$t_{HD;STA}$	start condition hold time		4.0	4.0	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
t_r	SCL and SDA rise time		–	–	1	µs
t_f	SCL and SDA fall time		–	–	0.3	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
$t_{HD;DAT}$	data hold time		0	–	–	ns
$t_{SU;STO}$	stop condition set-up time		4.0	–	–	µs

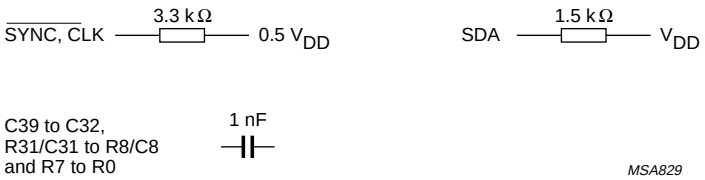


Fig.19 AC test loads.

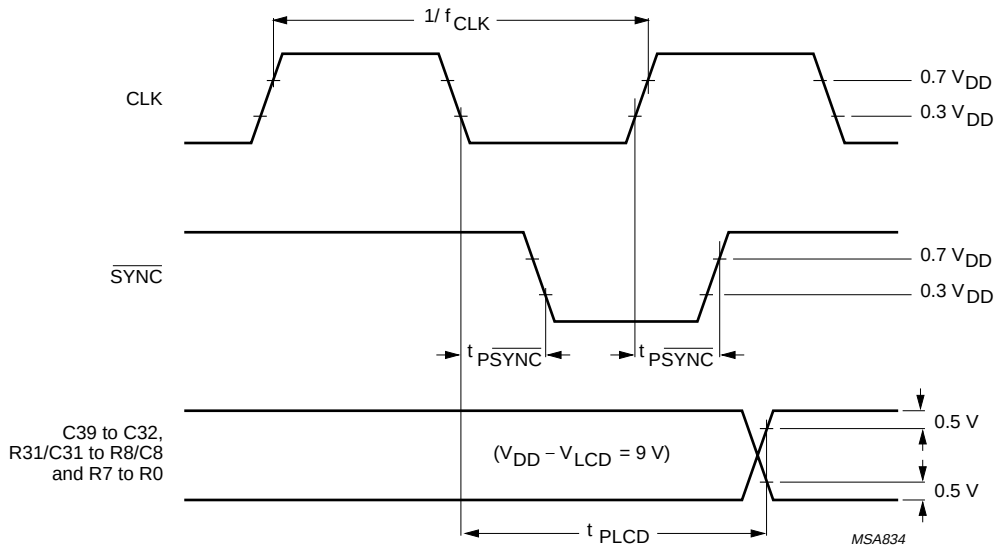


Fig.20 Driver timing waveforms.

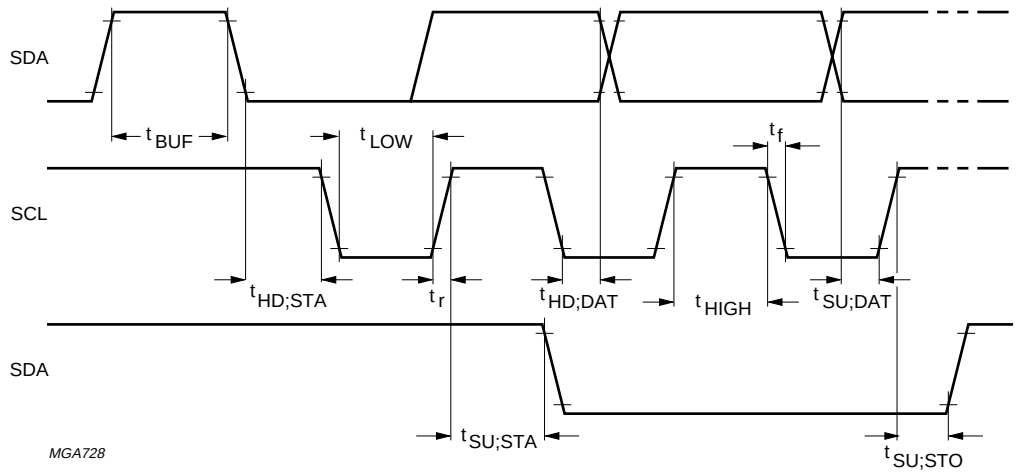


Fig.21 I²C-bus timing waveforms.

14 APPLICATION INFORMATION

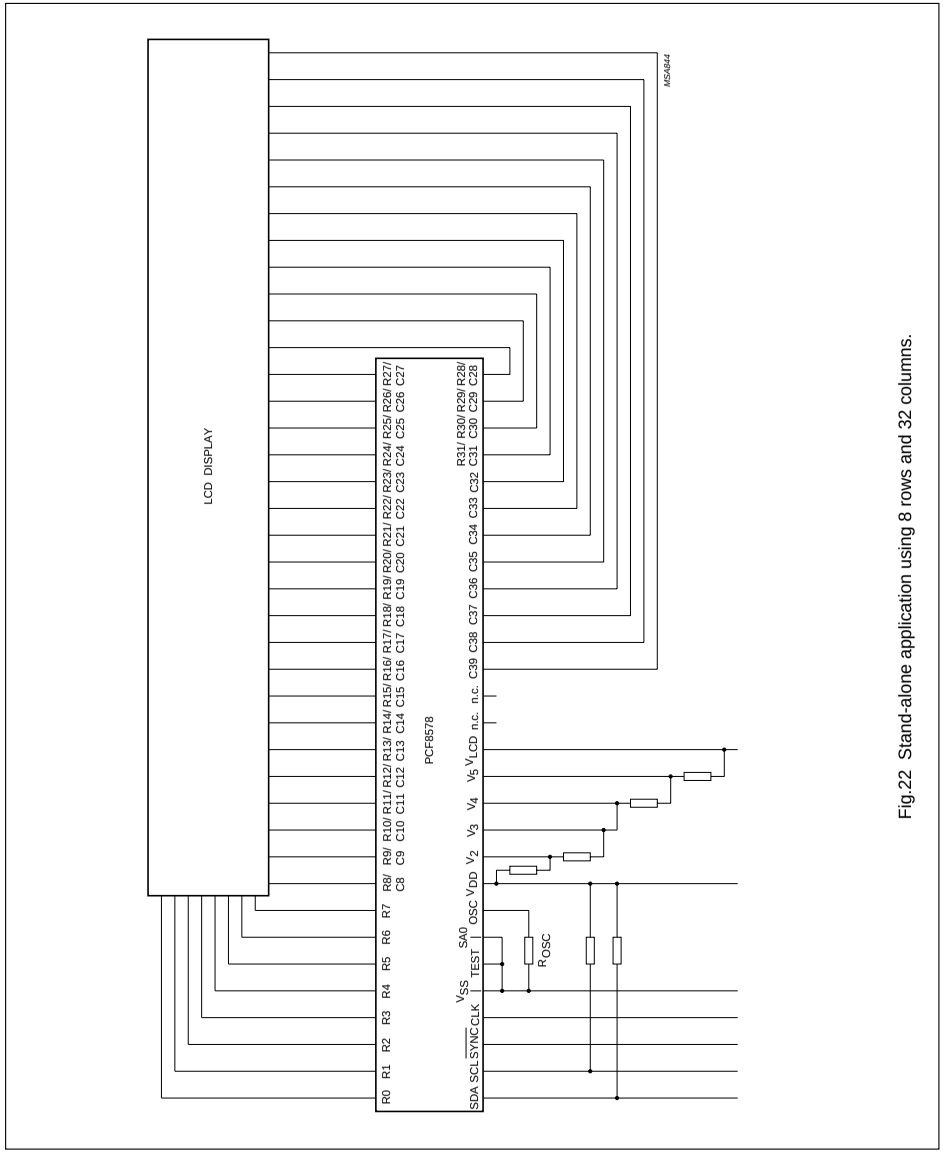


Fig.22 Stand-alone application using 8 rows and 32 columns.

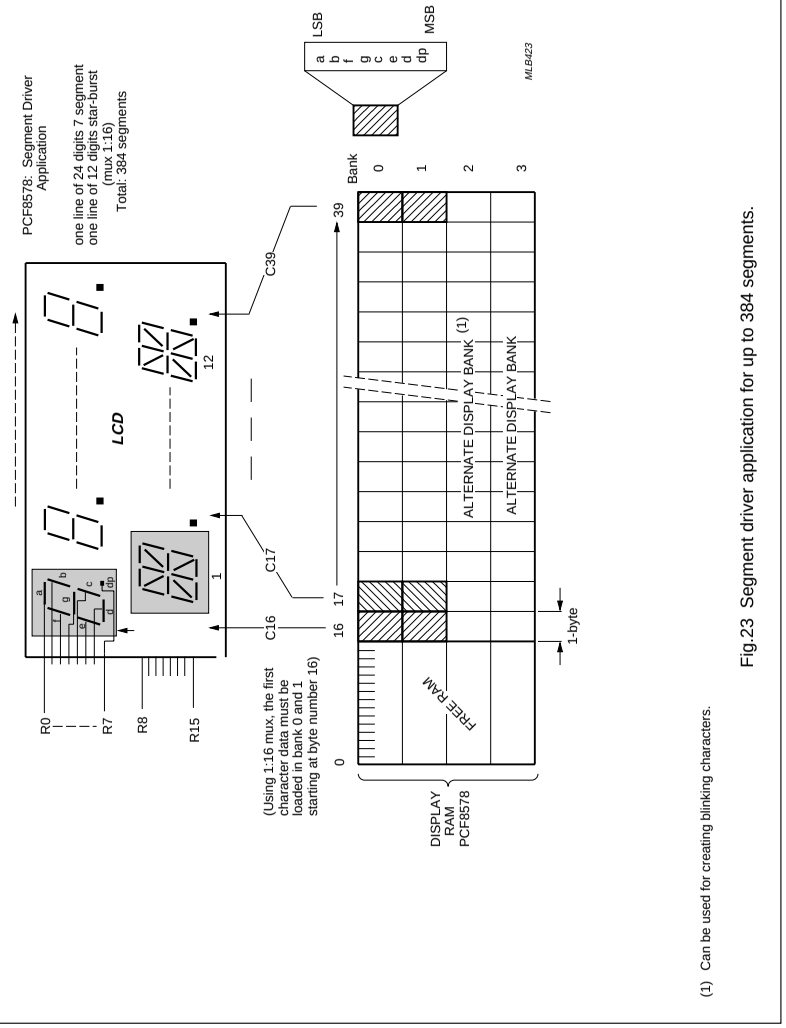


Fig.23 Segment driver application for up to 384 segments.

(1) Can be used for creating blinking characters.

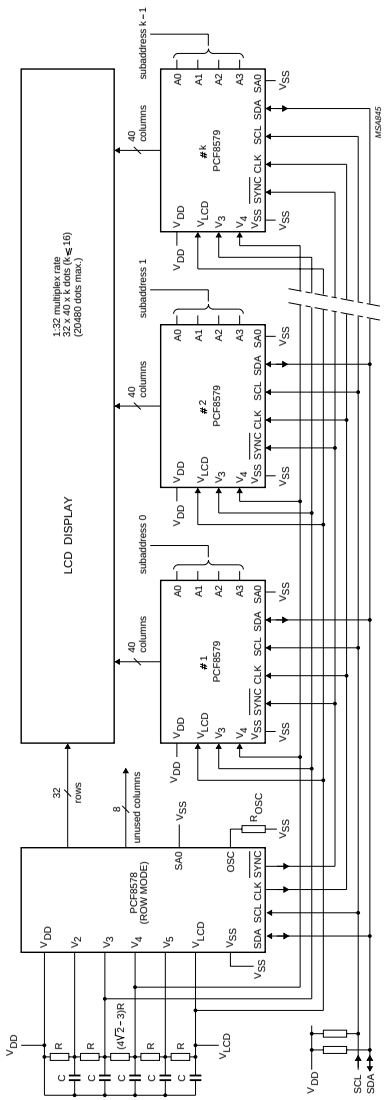


Fig.24 Typical LCD driver system with 1 : 32 multiplex rate.

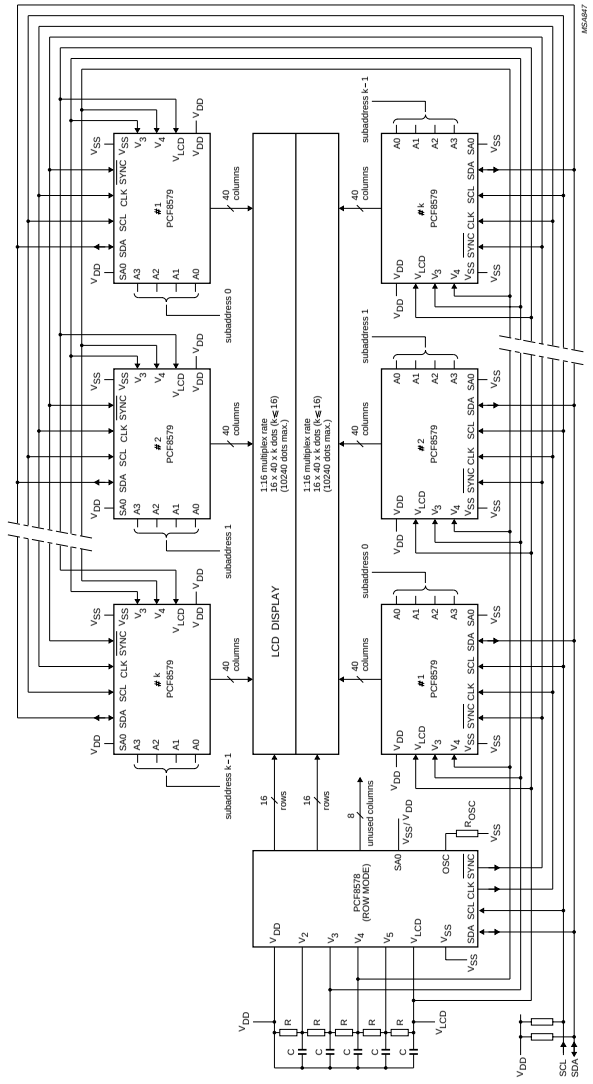


Fig.25 Split screen application with 1 : 16 multiplex rate for improved contrast.

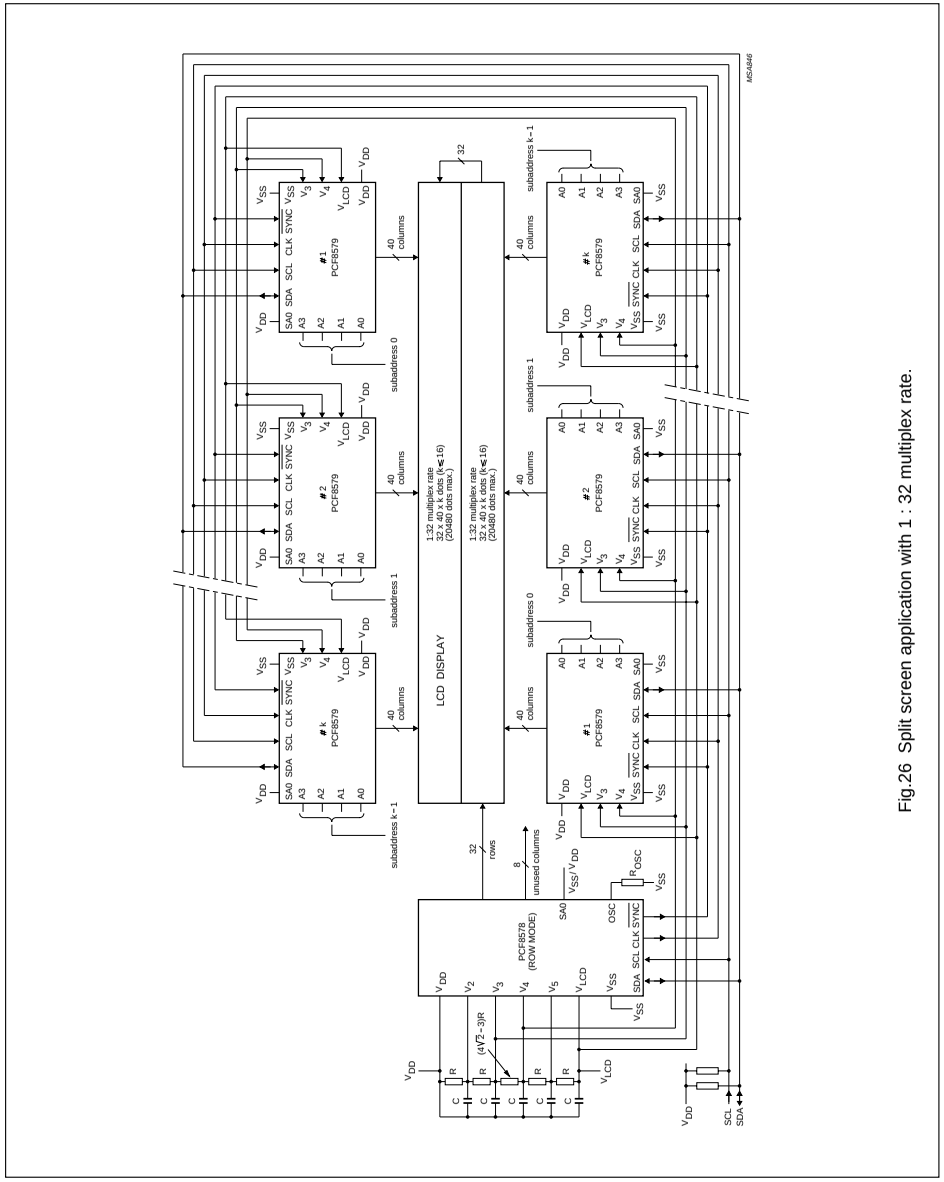


Fig.26 Split screen application with 1 : 32 multiplex rate.

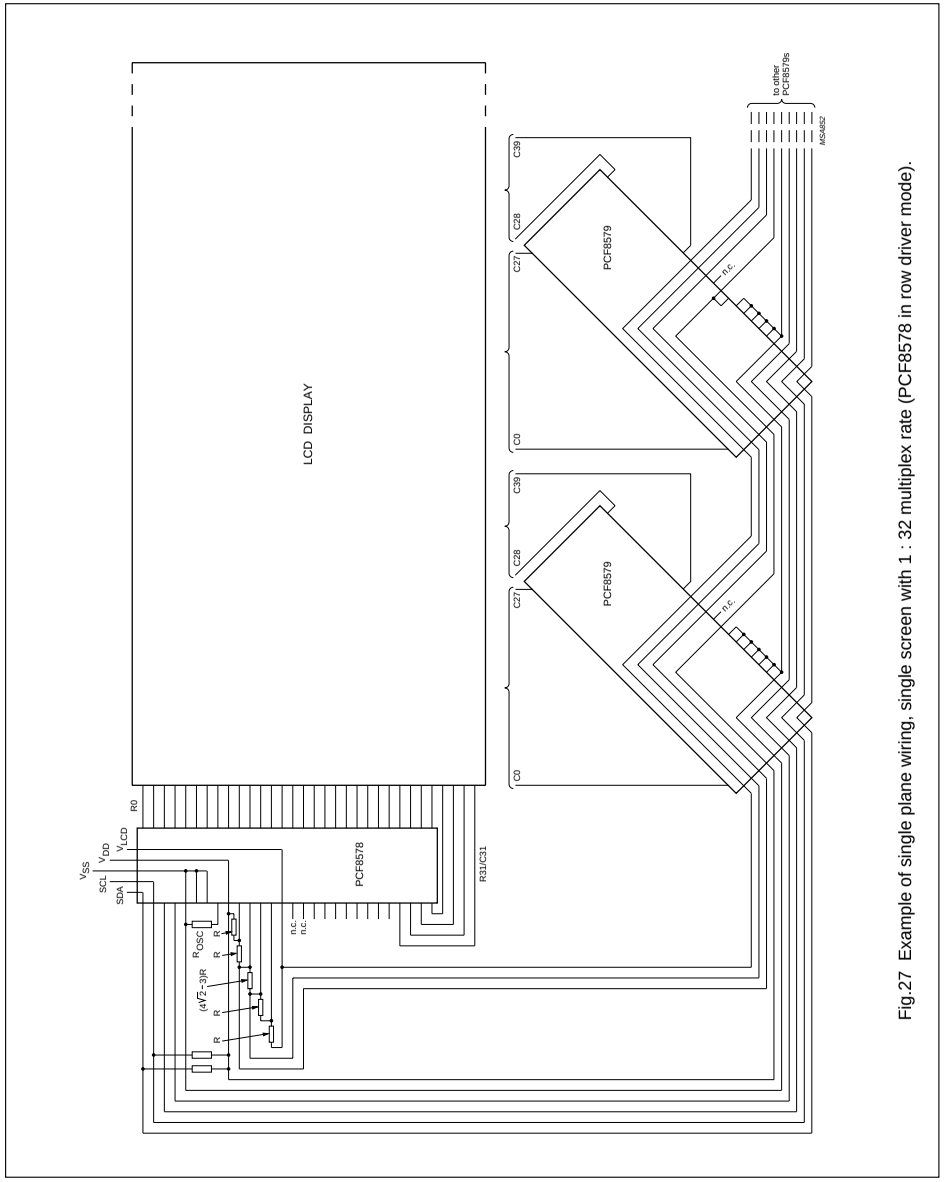
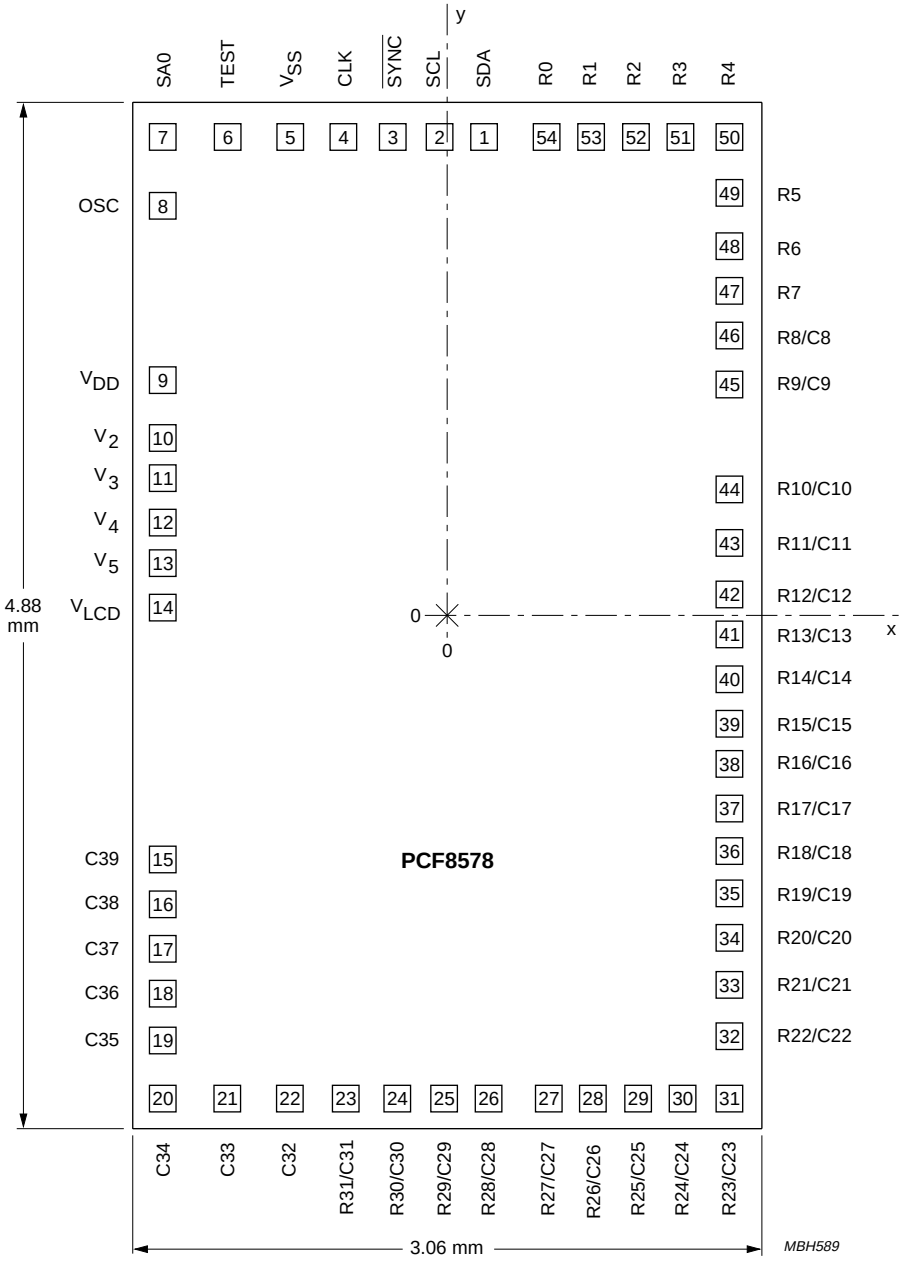


Fig.27 Example of single plane wiring, single screen with 1 : 32 multiplex rate (PCF8578 in row driver mode).

15 CHIP DIMENSIONS AND BONDING PAD LOCATIONS



Chip area: 14.93 mm^2.
Bonding pad dimensions: 120 µm × 120 µm.
The numbers given in the small squares refer to the pad numbers.

Fig.28 Bonding pad locations.

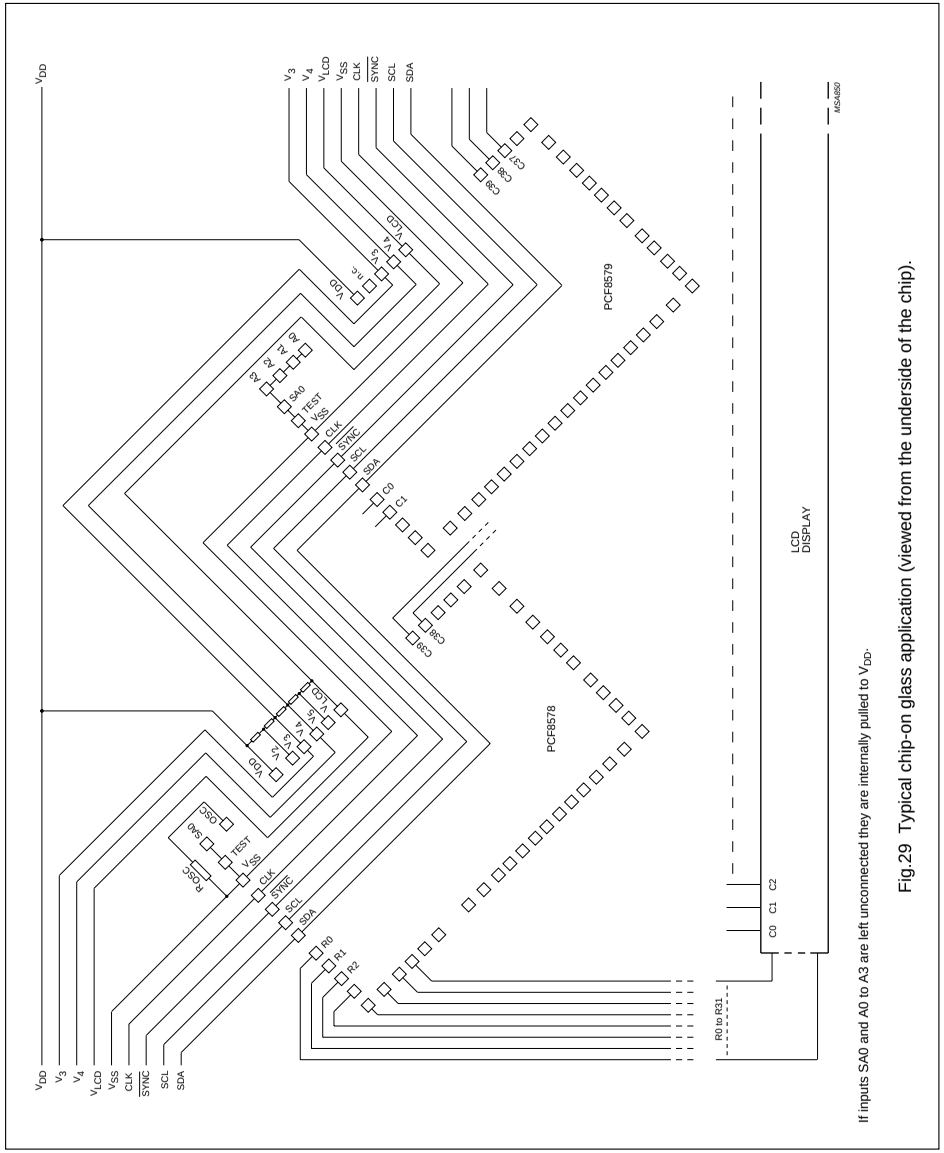
Table 15 Bonding pad locations (dimensions in μm)

All x/y coordinates are referenced to centre of chip, see Fig.28.

PAD NUMBER	SYMBOL	x	y	PINS	
				VSO56	LQFP64
1	SDA	174	2241	1	7
2	SCL	−30	2241	2	8
3	$\overline{SYNC}$	−234	2241	3	9
4	CLK	−468	2241	4	10
5	V_{SS}	−726	2241	5	11
6	TEST	−1014	2241	6	12
7	SA0	−1308	2241	7	13
8	OSC	−1308	1917	8	16
9	V_{DD}	−1308	1113	9	20
10	V_2	−1308	873	10	21
11	V_3	−1308	663	11	22
12	V_4	−1308	459	12	23
13	V_5	−1308	255	13	24
14	V_{LCD}	−1308	51	14	25
15	C39	−1308	−1149	17	29
16	C38	−1308	−1353	18	30
17	C37	−1308	−1557	19	31
18	C36	−1308	−1773	20	32
19	C35	−1308	−1995	21	33
20	C34	−1308	−2241	22	34
21	C33	−1014	−2241	23	35
22	C32	−726	−2241	24	37
23	R31/C31	−468	−2241	25	38
24	R30/C30	−234	−2241	26	39
25	R29/C29	−30	−2241	27	40
26	R28/C28	174	−2241	28	41
27	R27/C27	468	−2241	29	42
28	R26/C26	672	−2241	30	43
29	R25/C25	876	−2241	31	44
30	R24/C24	1080	−2241	32	45
31	R23/C23	1308	−2241	33	46
32	R22/C22	1308	−1977	34	48
33	R21/C21	1308	−1731	35	49
34	R20/C20	1308	−1515	36	50
35	R19/C19	1308	−1305	37	51
36	R18/C18	1308	−1101	38	52
37	R17/C17	1308	−897	39	53

PAD NUMBER	SYMBOL	x	y	PINS	
				VSO56	LQFP64
38	R16/C16	1308	−693	40	54
39	R15/C15	1308	−489	41	55
40	R14/C14	1308	−285	42	56
41	R13/C13	1308	−81	43	57
42	R12/C12	1308	123	44	58
43	R11/C11	1308	351	45	59
44	R10/C10	1308	603	46	60
45	R9/C9	1308	1101	47	61
46	R8/C8	1308	1305	48	62
47	R7	1308	1515	49	63
48	R6	1308	1731	50	64
49	R5	1308	1977	51	1
50	R4	1308	2241	52	2
51	R3	1080	2241	53	3
52	R2	876	2241	54	4
53	R1	672	2241	55	5
54	R0	468	2241	56	6
–	n.c.	–	–	15, 16	14, 15, 17 to 19, 26 to 28, 36, 47

16 CHIP-ON GLASS INFORMATION

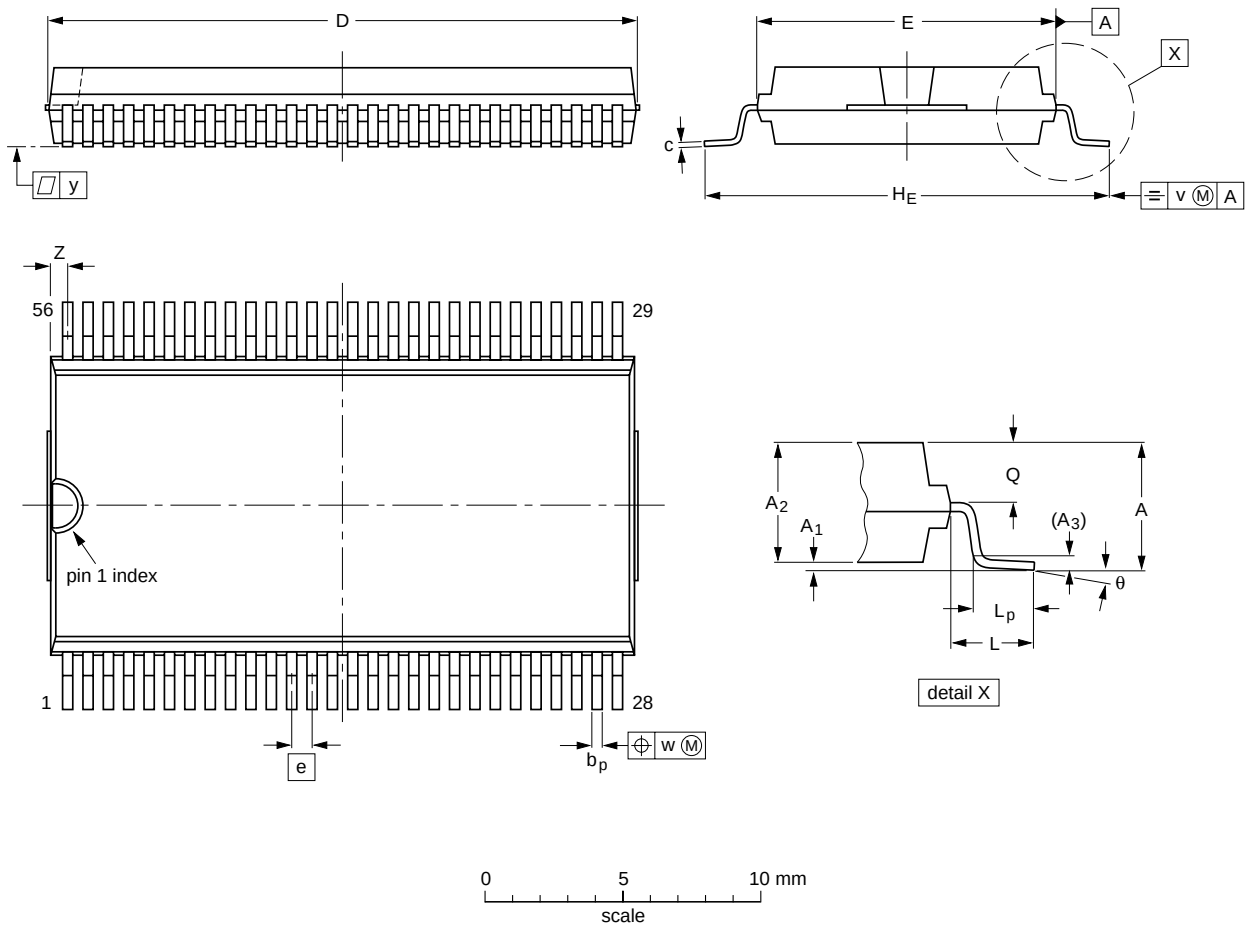


If inputs SA0 and A0 to A3 are left unconnected they are internally pulled to V_{DD}.

Fig.29 Typical chip-on glass application (viewed from the underside of the chip).

17 PACKAGE OUTLINES

VSO56: plastic very small outline package; 56 leads **SOT190-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

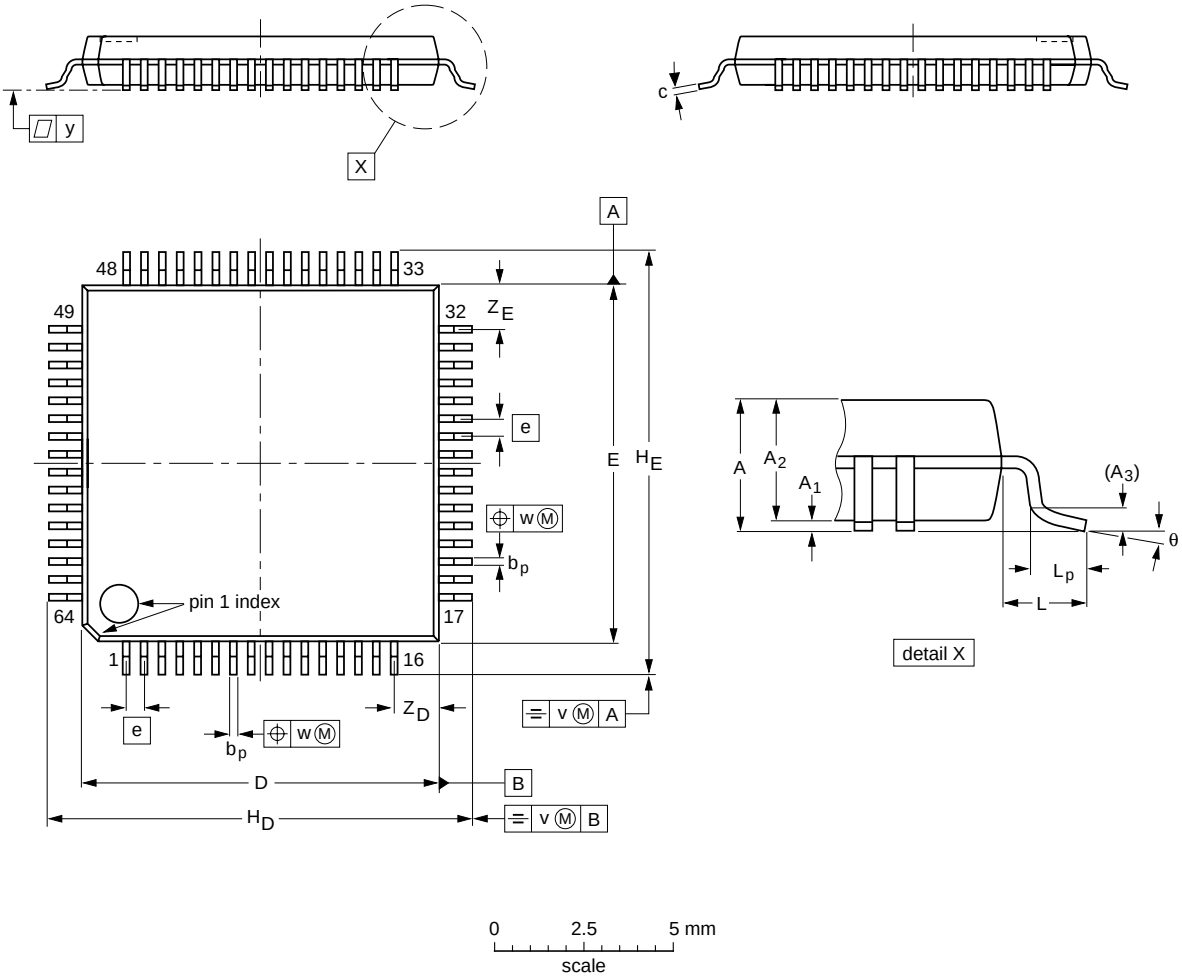
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7^o 0^o
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Note

1. Plastic or metal protrusions of 0.3 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT190-1						~~96-04-02~~ 97-08-11

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1.0	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT314-2						~~95-12-19~~ 97-08-01

18 SOLDERING

18.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

18.2 Reflow soldering

Reflow soldering techniques are suitable for all LQFP and VSO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

18.3 Wave soldering

18.3.1 LQFP

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all LQFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for LQFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

18.3.2 VSO

Wave soldering techniques can be used for all VSO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

18.3.3 METHOD (LQFP AND VSO)

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

18.4 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

19 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

20 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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