DATA SHEET

SAA8117HL
Digital camera USB interface IC

Product specification
File under Integrated Circuits, IC22

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Philips
Semiconductors

PHILIPS

CONTENTS

Digital camera USB interface IC SAA8117HL

1 FEATURES

- Medium resolution CCD sensors (PAL non-interlaced mode) or VGA CCD sensors (progressive mode)
- D1 digital video input (8 bits YUV 4 : 2 : 2, time multiplexed)
- Internal Pulse Pattern Generator (PPG) dedicated for medium resolution Sharp or compatible sensors and VGA sensors and for frame rate selection
- Video formatter (programmable CIF formatter and compression engine) controlled via SNERT (UART) interface
- Selectable output frame rate (1 fps in VGA, up to 15 fps in CIF format)
- Video packetizer FIFO
- I^{2}C-bus interface for communication between the USB protocol hardware and the external microcontroller
- Integrated analog bus driver (ATX)
- Microphone/audio input to USB (FGA, ADC, PLL and decimator filter)
- Integrated analog bus driver (ATX)
- Integrated main oscillator
- Miscellaneous functions e.g. power management, PLL backup oscillator.

2 APPLICATIONS

- Low-cost desktop video applications with USB interface.

3 GENERAL DESCRIPTION

The SAA8117HL is a monolithic integrated circuit which can be used in PC video cameras to convert D1 video signals and analog audio signals to properly formatted USB packets.

It is designed as a back-end for the SAA8110G or SAA8112HL (general camera digital processing ICs) and is optimized for use with the TDA8784/87 (camera pre-processing IC) and the 83C51RC (microcontroller).

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
SAA8117HL	LQFP100	plastic low profile quad flat package; 100 leads; body 14 × 14 × 1.4 mm	SOT407-1

5 QUICK REFERENCE DATA

Measured over full voltage and operating temperature range.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
$I_{DD(tot)}$	total supply current	V_{DD} = 3.3 V	–	91	–	mA
$V_{i(bus)}$	input voltage on I^2C-bus interface pins		5 V tolerant TTL compatible			V
$V_{o(bus)}$	output voltage on I^2C-bus interface pin SDA		5 V tolerant TTL compatible			V
$V_{i(n)}$	input signal voltage on other pins	3.0 V < V_{DD} < 3.6 V	low voltage TTL compatible			V
$V_{o(n)}$	output signal voltage on other pins	3.0 V < V_{DD} < 3.6 V	low voltage TTL compatible			V
f_{clk}	clock frequency		–	48	–	MHz
P_{tot}	total power dissipation	T_{amb} = 25 °C	–	300	–	mW
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		0	25	70	°C
T_j	junction temperature	T_{amb} = 70 °C	–40	–	+125	°C

6 BLOCK DIAGRAM

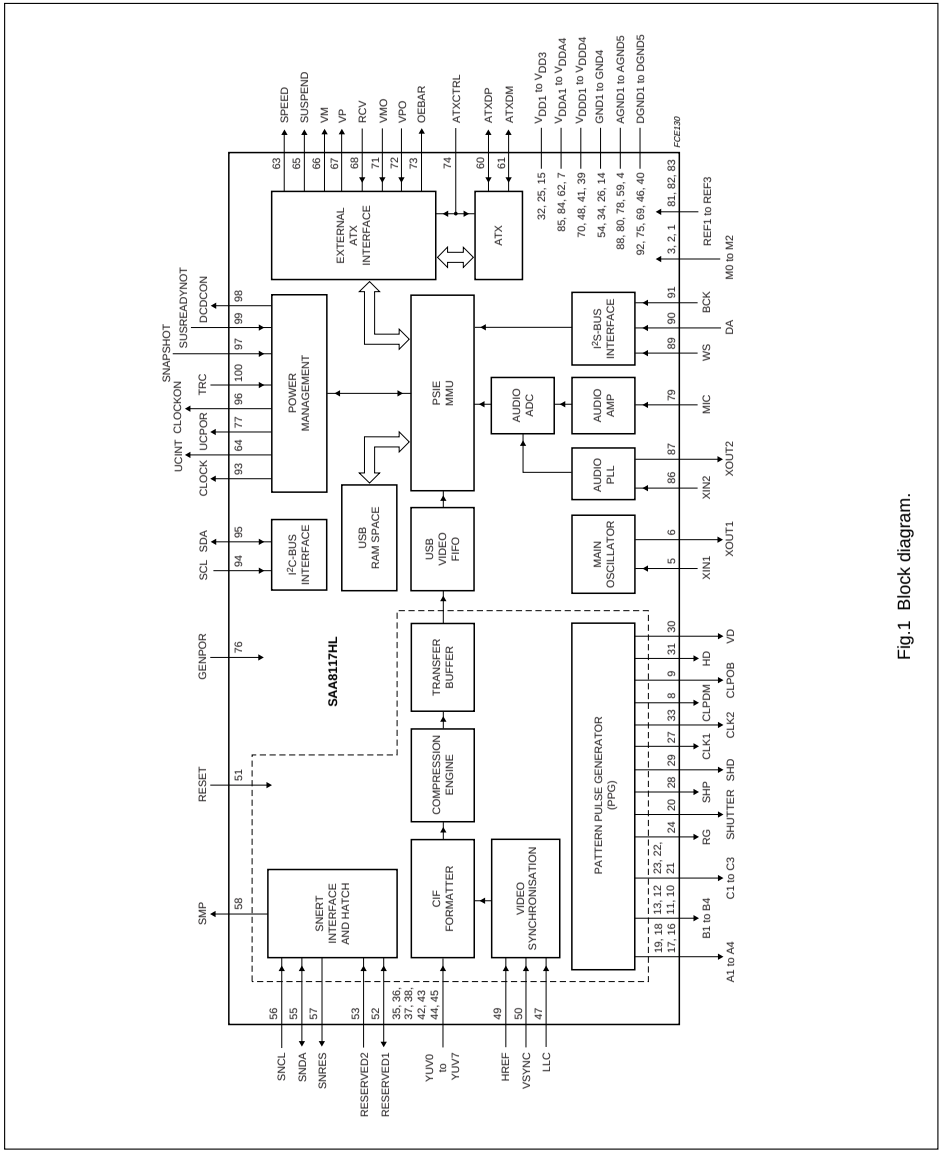


Fig.1 Block diagram.

7 PINNING

SYMBOL	PIN	TYPE	DESCRIPTION
M2	1	I	test mode control signal bit 2
M1	2	I	test mode control signal bit 1
M0	3	I	test mode control signal bit 0
AGND1	4	P	analog ground 1 for main oscillator (48 MHz, 3rd overtone)
XIN1	5	I	oscillator input
XOUT1	6	O	oscillator output
V_{DDA1}	7	P	analog supply voltage 1 for main oscillator (48 MHz, 3rd overtone)
CLPDM	8	O	dummy clamp pulse output to TDA8784/87
CLPOB	9	O	optical black clamp pulse output to TDA8784/87
B4	10	O	vertical CCD load pulse output (VH1X)
B3	11	O	vertical CCD load pulse output (VH3X)
B2	12	O	vertical CCD load pulse output
B1	13	O	vertical CCD load pulse output
GND1	14	P	ground 1 for output buffers
V_{DD1}	15	P	supply voltage 1 for output buffers
A4	16	O	vertical CCD transfer pulse output (V4X)
A3	17	O	vertical CCD transfer pulse output (V3X)
A2	18	O	vertical CCD transfer pulse output (V2X)
A1	19	O	vertical CCD transfer pulse output (V1X)
SHUTTER	20	O	shutter control output for CCD charge reset
C3	21	O	horizontal CCD transfer pulse output
C2	22	O	horizontal CCD transfer pulse output (FH1)
C1	23	O	horizontal CCD transfer pulse output (FH2)
RG	24	O	reset output for CCD output amplifier gate
V_{DD2}	25	P	supply voltage 2 for output buffers
GND2	26	P	ground 2 for output buffers
CLK1	27	O	pixel clock output to TDA8784/87and SAA8110G
SHP	28	O	preset sample-and-hold pulse output to TDA8784/87 (FCDS)
SHD	29	O	data sample-and-hold pulse output to TDA8784/87 (FS)
VD	30	O	vertical definition pulse output to SAA8110G
HD	31	O	horizontal definition pulse output to SAA8110G
V_{DD3}	32	P	supply voltage 3 for output buffers
CLK2	33	O	double pixel clock output to SAA8110G
GND3	34	P	ground 3 for output buffers
YUV0	35	I	multiplexed input YUV-bit 0 (LSB)
YUV1	36	I	multiplexed input YUV-bit 1 input
YUV2	37	I	multiplexed input YUV-bit 2 input
YUV3	38	I	multiplexed input YUV-bit 3 input
V_{DDD1}	39	P	digital supply voltage 1 for input buffers and predrivers and one part of the digital core

SYMBOL	PIN	TYPE	DESCRIPTION
DGND1	40	P	digital ground 1 for input buffers and predrivers and for the digital core
V_{DDD2}	41	P	digital supply voltage 2 for digital core
YUV4	42	I	multiplexed input YUV-bit 4
YUV5	43	I	multiplexed input YUV-bit 5
YUV6	44	I	multiplexed input YUV-bit 6
YUV7	45	I	multiplexed input YUV-bit 7
DGND2	46	P	digital ground 2 for input buffers and predrivers and for the digital core
LLC	47	I	line-locked clock input (delayed CLK2) for YUV-port from SAA8110G
V_{DDD3}	48	P	digital supply voltage 3 for digital core
HREF	49	I	horizontal reference input for YUV-port from SAA8110G
VSYNC	50	I	vertical synchronization input for YUV-port from SAA8110G
RESET	51	I	Power-on reset input (for video processing and PPG)
RESERVED1	52	–	test pin (should not be used)
RESERVED2	53	–	test pin (should not be used)
GND4	54	P	ground 4 for output buffer
SNDA	55	I/O	data I/O for SNERT-interface (communication between SAA8117HL and SAA8110G)
SNCL	56	I	input clock for SNERT-interface (communication between SAA8117HL and SAA8110G)
SNRES	57	O	output reset for SNERT-interface (communication between SAA8117HL and SAA8110G)
SMP	58	O	output switch mode pulse for DC-to-DC power supply
AGND2	59	P	analog ground 2 for ATX (transceiver)
ATXDP	60	I/O	positive driver of the differential data pair input/output (ATX)
ATXDM	61	I/O	negative driver of the differently data pair input/output (ATX)
V_{DDA2}	62	P	analog supply voltage 2 for ATX
SPEED	63	O	required output for ATX-backup solution
UCINT	64	O	interrupt output from USB protocol hardware to microcontroller
SUSPEND	65	O	control output from USB protocol hardware to microcontroller
VM	66	O	required output for ATX-backup solution (txdn)
VP	67	O	required output for ATX-backup solution (txdp)
RCV	68	I	required output for ATX-backup solution
DGND3	69	P	digital ground 3 for input buffers and predrivers and for the digital core
V_{DDD4}	70	P	digital supply voltage 4 for one part of input buffers and predrivers and for the digital core
VMO	71	I	required input or ATX-backup solution (rxdn)
VPO	72	I	required input for ATX-backup solution (rxdp)
OEBAR	73	O	required output for ATX-backup solution
ATXCTRL	74	I	required input for ATX-backup solution
DGND4	75	P	digital ground 4 for input buffers and predrivers and for the digital core
GENPOR	76	I	Power-on reset input (for USB protocol hardware)

SYMBOL	PIN	TYPE	DESCRIPTION
UCPOR	77	O	output control from USB protocol hardware to microcontroller
AGND3	78	P	analog ground 3 for FGA
MIC	79	I	microphone input
AGND4	80	P	analog ground 4 for FGA/ADC
REF1	81	I	reference input voltage 1 for FGA/ADC (double-bonding)
REF2	82	I	reference input voltage 2 for DACn (used in the ADC)
REF3	83	I	reference input voltage 3 for DACp (used in the ADC)
V_{DDA3}	84	P	analog supply voltage 3 for FGA/ADC
V_{DDA4}	85	P	analog supply voltage 4 for PLL
XIN2	86	I	oscillator input required for PLL backup solution
XOUT2	87	O	oscillator output required for PLL backup solution
AGND5	88	P	analog ground 5 for PLL
WS	89	I	I^2S-bus word select (required for FGA/ADC backup solution)
DA	90	I	I^2S-bus data (required for FGA/ADC backup solution)
BCK	91	I	I^2S-bus clock (required for FGA/ADC backup solution)
DGND5	92	P	digital ground 5 for input buffers and predrivers and for the digital core
CLOCK	93	O	clock output from USB protocol hardware to microcontroller
SCL	94	I	slave I^2C-bus clock input
SDA	95	I/O	slave I^2C-bus data input/output
CLOCKON	96	O	control output for main oscillator switched on
SNAPSHOT	97	I	input for remote wake-up (snapshot)
DCDCON	98	O	control output from USB protocol hardware to power supply module
SUSREADYNOT	99	I	input from microcontroller for SUSPEND mode
TRC	100	I	threshold control input for enabling the clock (switching for power management)

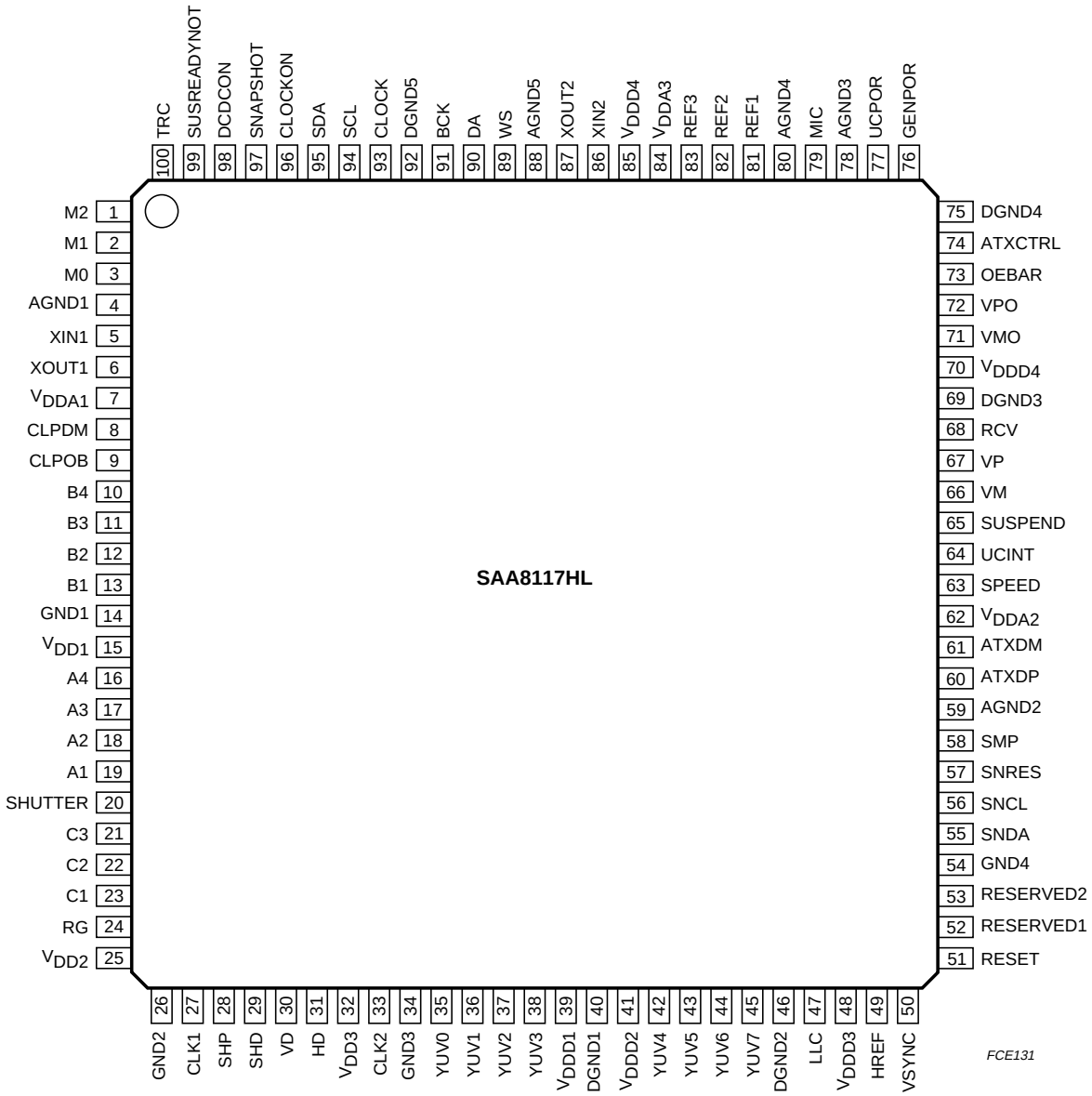


Fig.2 Pin configuration.

8 FUNCTIONAL DESCRIPTION

8.1 Video synchronization

The video synchronization module (see Fig.1) is capable of locking onto the video signal thereby implementing a horizontal gate signal HREF (HREF = HIGH when data is valid) and a VS signal indicating the start of a new video frame. This module expects, in the PAL mode, 288 active lines from a total of 292 lines and in the VGA mode, 480 active lines from a total of 486 lines. The module generates control signals for the CIF formatter.

8.2 CIF formatter

The video data must be progressive (or non-interlaced) and in 4 : 2 : 2 (UYVY) format. The CIF formatter module (see Figs 1 and 3) is programmable to perform down scaling from 512 × 288 (PAL mode) or 640 × 480 (VGA mode) to 352 × 288 or 176 × 144 without affecting the aspect ratio.

The horizontal scaling is achieved with a Variable Phase Delay filter (VPD-4). To avoid aliasing, this module also contains a prefilter which has three modes:

- Prefilter A (3 taps)
- Prefilter B (7 taps)
- Prefilter B-comb (13 taps).

Prefilter B-comb is similar to prefilter B, but inserts extra taps with amplification 0.

This prefilter must be chosen by selecting prefilter B and setting SN_Prefilter_B_Comb. Prefilter B-comb can be used independently from prefilter A.

The incoming 4 : 2 : 2 data is vertically filtered to 4 : 2 : 0 by throwing away colour samples. In the even lines the V-samples are discarded, in the odd lines the U-samples.

The vertical scaling in PAL mode is from CIF (352 × 288) to QCIF (176 × 144) only. This is done via a vertical prefilter A (3 taps). In VGA mode a VPD-4 vertical filter is applied to scale from 640 × 480 to CIF and QCIF.

From the QCIF image a sub-QCIF cut (128 × 96) can be made. Due to the granularity of the cropping origin, a UV interchange can occur. This interchange can be corrected with SN_EIRRAH.

In VGA mode the CIF formatter can be bypassed to create a full resolution snapshot. The snapshot can be in 4 : 2 : 0 and in 4 : 2 : 2 format, selectable with SN_4 : 2 : 2.

8.3 Compression engine

The compression engine module (see Figs 1 and 3) works on CIF format only. The CIF data is compressed to a fixed number of bytes per frame. This number can be selected leading a compression factor of either 3 or 4. As a result the data stream of CIF 4 : 2 : 0 equals the data stream of QCIF 4 : 2 : 2 (3 times compression) or QCIF 4 : 2 : 0 (4 times compression). The algorithm is Philips proprietary. Real-time decoding can be done in software on any Pentium platform.

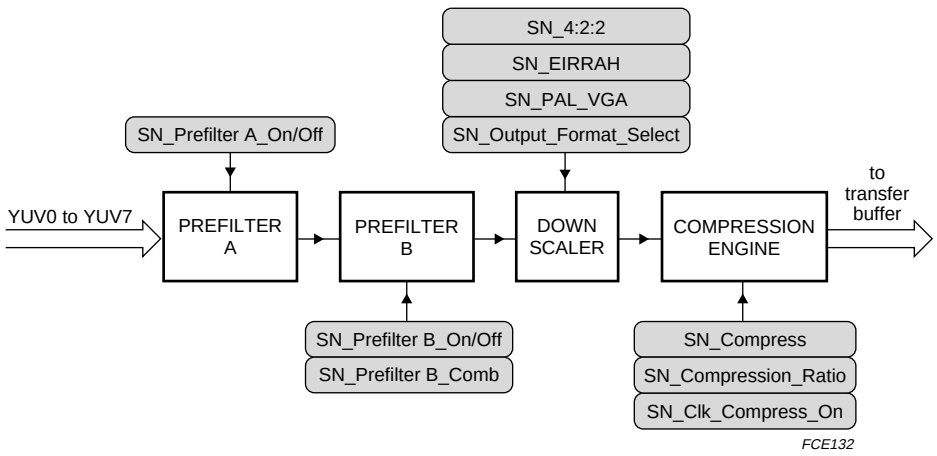


Fig.3 The CIF formatter and compression engine.

8.4 Transfer buffer

The transfer buffer module (see Fig.1) ensures a smooth transfer of the data to the FIFO of the USB. Moreover the transfer buffer can insert in band synchronization words in the video data stream.

This function can be switched on and off with SN_In band_Control in register CONTROL17_0. The synchronization words can only be used with non-compressed data streams and are formatted like 0x00 0xFF 0x<framecounter>$_7$<linecounter>$_9$. The subscript denotes the number of bits and the frame counter is circular incrementing.

The non-compressed data is formatted like:

4 : 2 : 0: <optional sync word><Y0><Y1><Y2><Y3> <C0><C2><Y4><Y5><Y6><Y7><C4><C6>....,

4 : 2 : 2: <optional sync word><Y0><Y1><Y2><Y3> <U0><V0><U2><V2><Y4>....,

where C denotes U-data in the even lines (0, 2, 4, etc.) and V-data in the odd lines (1, 3, 5, etc.).

8.5 SNERT interface

In a USB camera the SAA8110G will operate on a clock frequency which depends on the actual frame rate. For the slowest frame rates, this frequency can be so low that the SNERT communication is no longer functional over the specified entire frequency range of the microcontroller. The microcontroller must adapt its SNERT bus frequency to a frequency appropriate for the current mode in which the SAA8110G is operating.

The SAA8117HL itself is also partly controlled via SNERT. The CIF formatter, compression engine and the PPG function are controlled via SNERT. This SNERT interface works independently from the frame rate and can always be operated in the full frequency range.

8.6 Sensor pulse generator

The SAA8117HL incorporates a Pulse Pattern Generator (PPG) function. The PPG can be used for PAL medium resolution Sharp sensors (LZ2423) or compatible CCD sensors. The SAA8117HL can also handle VGA type CCD sensors, so a set of pulses is provided to simplify the use of such sensors. Depending on the type of sensor, it will be necessary to reformat these pulses externally according to the sensor specification.

It should be noted that in case of medium resolution Sharp or compatible sensors an external inverter driver is required to convert the 3 V pulses into a voltage suitable for the used CCD sensor. For the medium resolution Sharp CCD sensor driver, the name of the pins to which the PPG pulses must be connected are indicated between brackets in the SAA8117HL pinning list (pins C3, B1 and B2 are not used).

For both type of sensors the PPG generates 8 different frame rates (see Table 6). The active video size is 512×288 for PAL and 640×480 for VGA. The total $H \times V$ size is 685×292 for PAL and 823×486 for VGA.

It should be noted that additional HD pulses are added during the vertical blanking interval to reach a total of 312 lines in PAL mode and 525 lines in VGA mode as required by the SAA8110G.

The following registers are associated with the PPG:

- CONTROL17_0
- CONTROL17_2
- PPG_SHUTTERSPEED_0
- PPG_SHUTTERSPEED_1
- PPG_CLPOB_START_LSB
- PPG_CLPOB_STOP_LSB
- PPG_CLPDM_START_LSB
- PPG_CLPDM_STOP_LSB
- CLPMSB.

8.7 Pulse diagrams

For medium resolution CCD sensors (PAL):

- High-speed pulses, see Figs 4 and 5
- Horizontal pulses, see Fig.6
- Vertical pulses, see Figs 7 to 11.

For VGA-sensors:

- High-speed pulses, see Figs 12 to 14
- Horizontal pulses, see Fig.15
- Vertical pulses, see Figs 16 to 21.

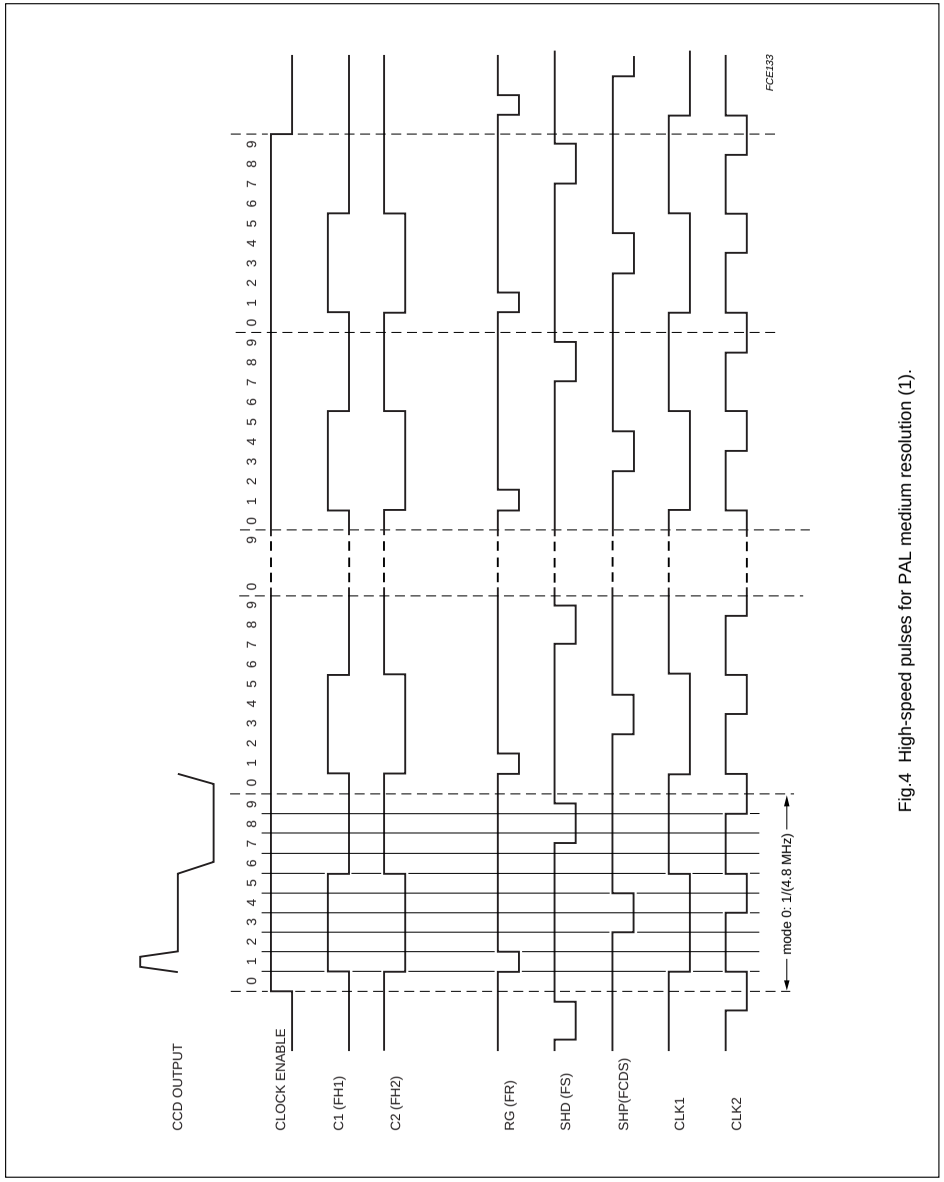


Fig.4 High-speed pulses for PAL medium resolution (1).

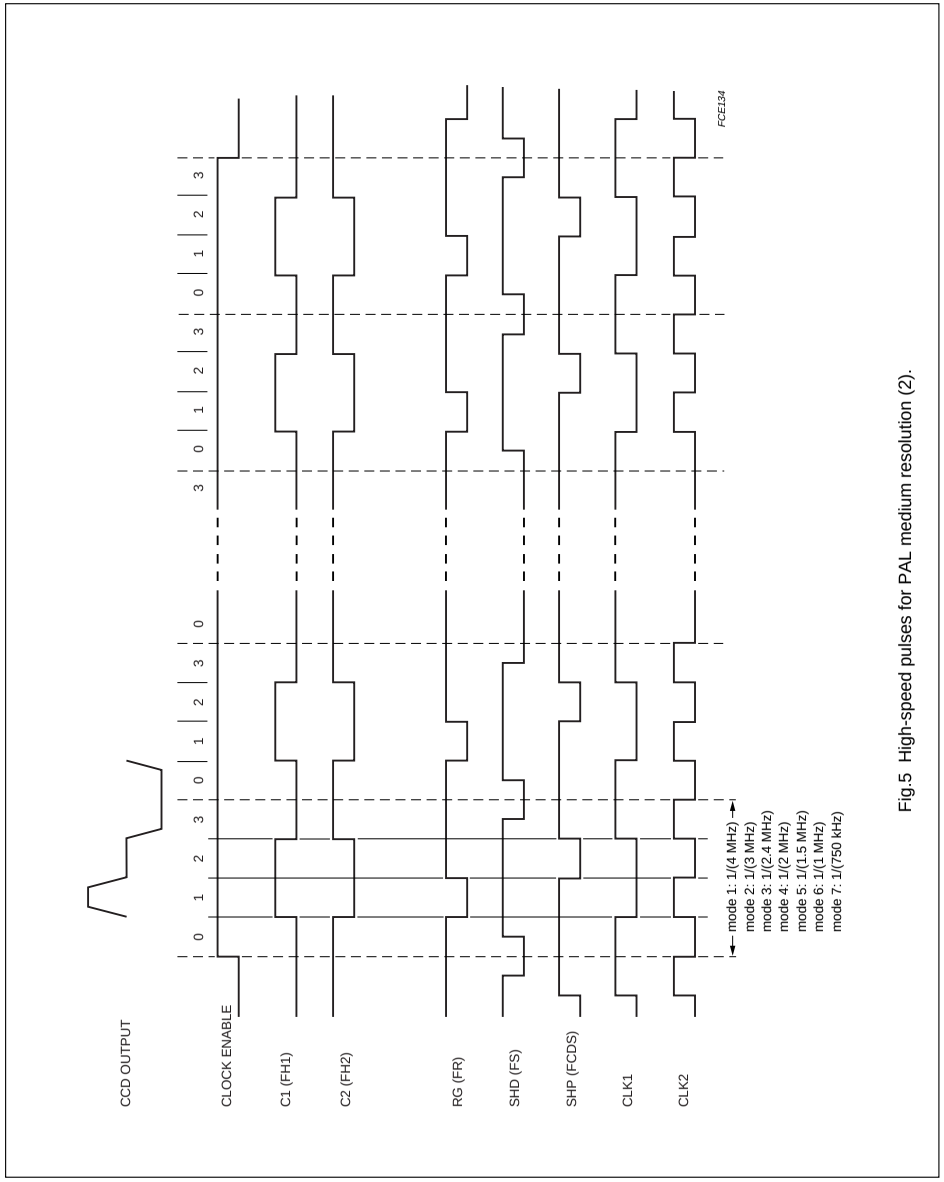


Fig.5 High-speed pulses for PAL medium resolution (2).

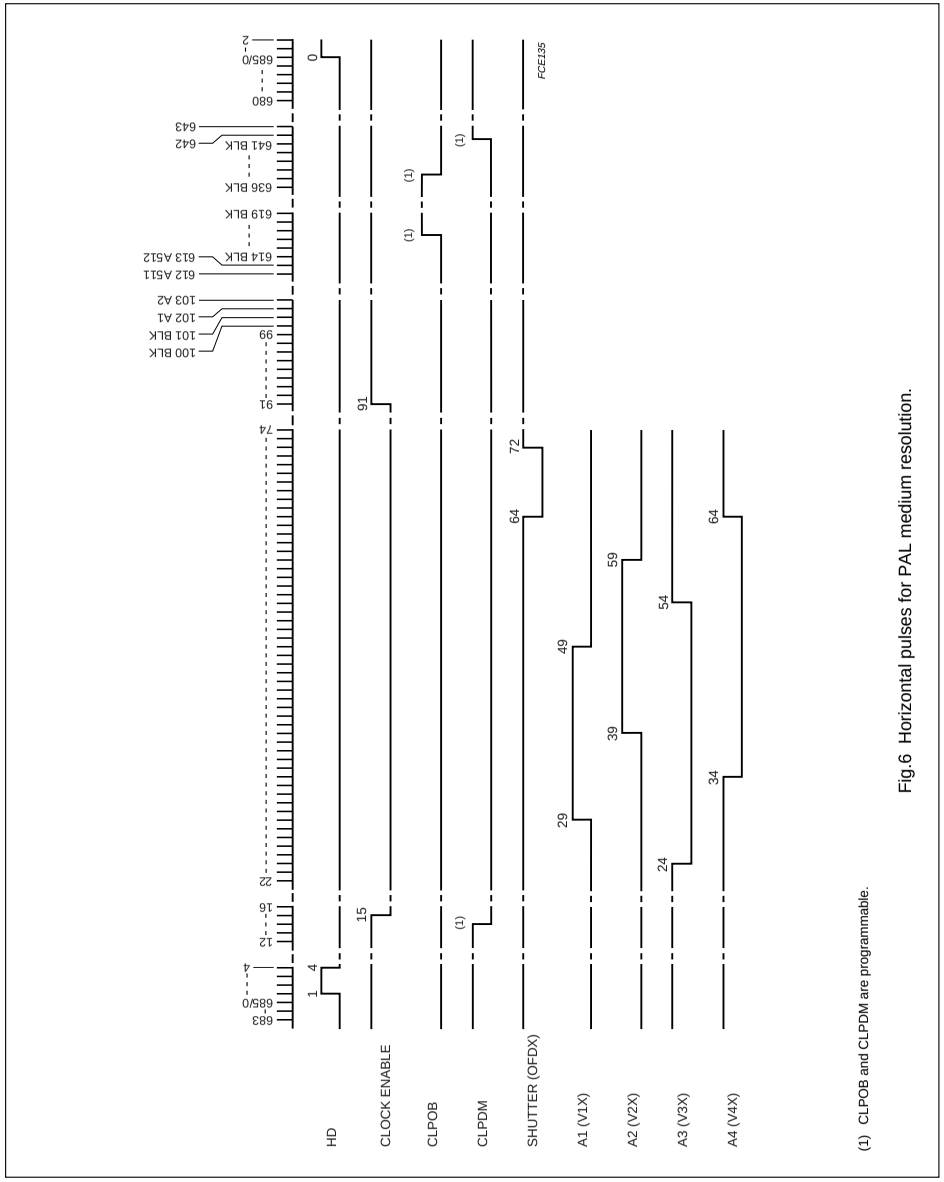


Fig.6 Horizontal pulses for PAL medium resolution.

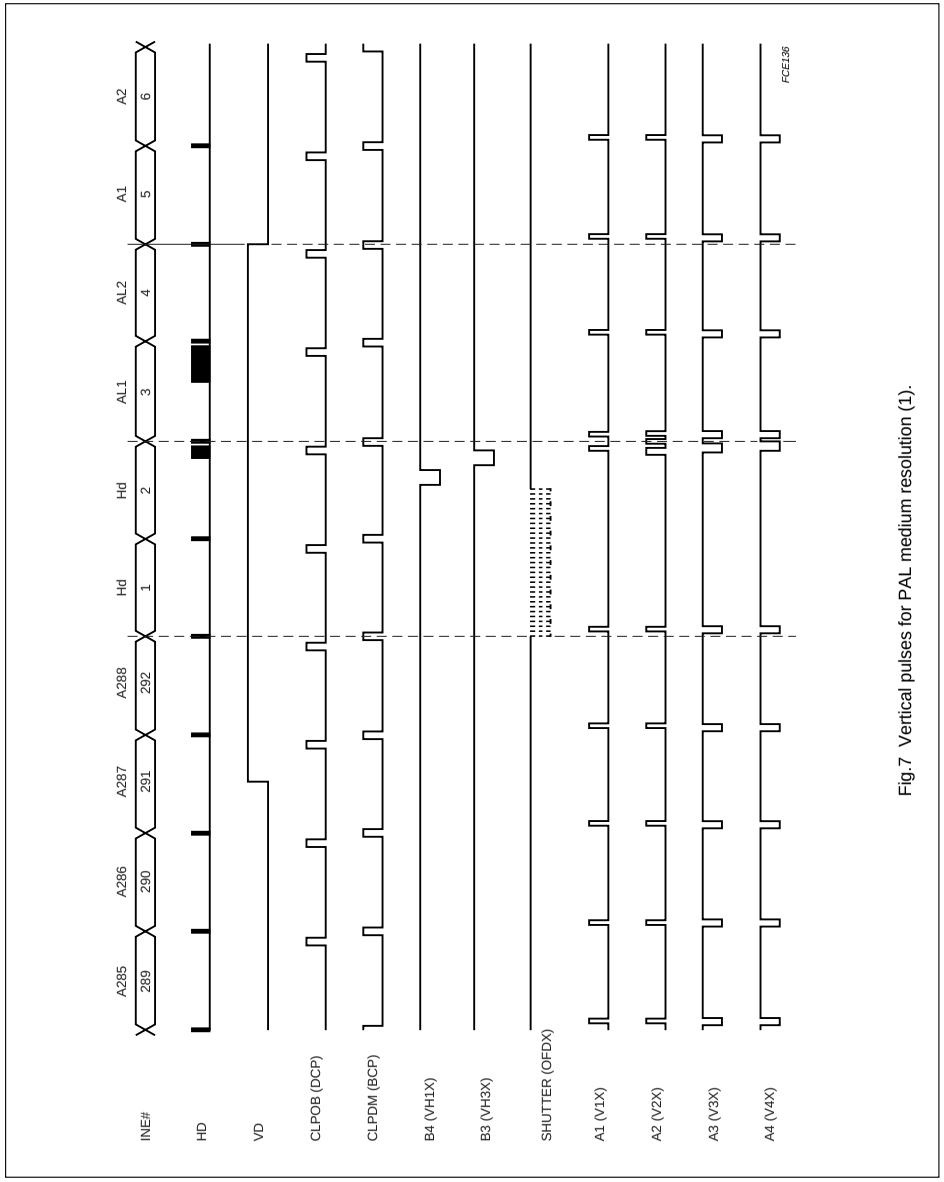


Fig.7 Vertical pulses for PAL medium resolution (1).

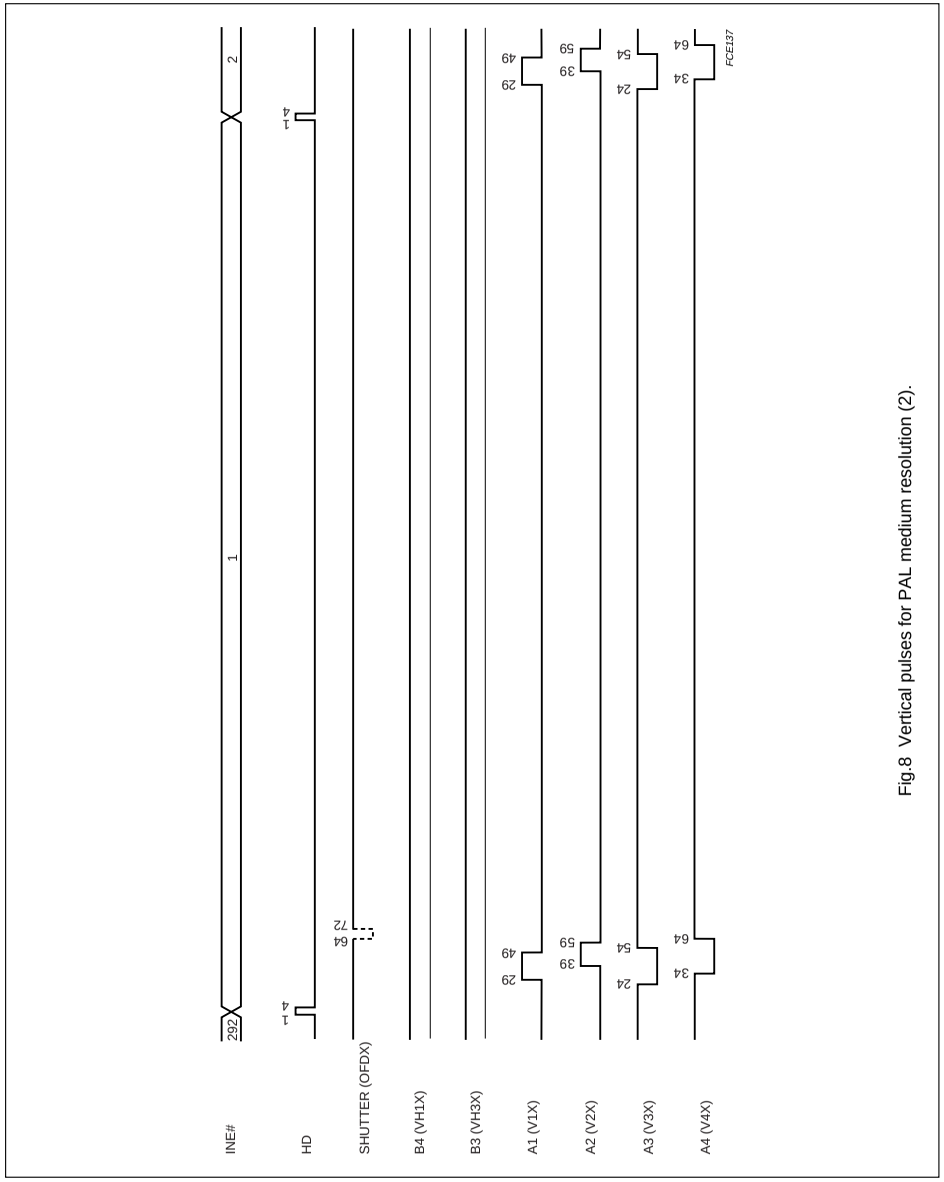


Fig.8 Vertical pulses for PAL medium resolution (2).

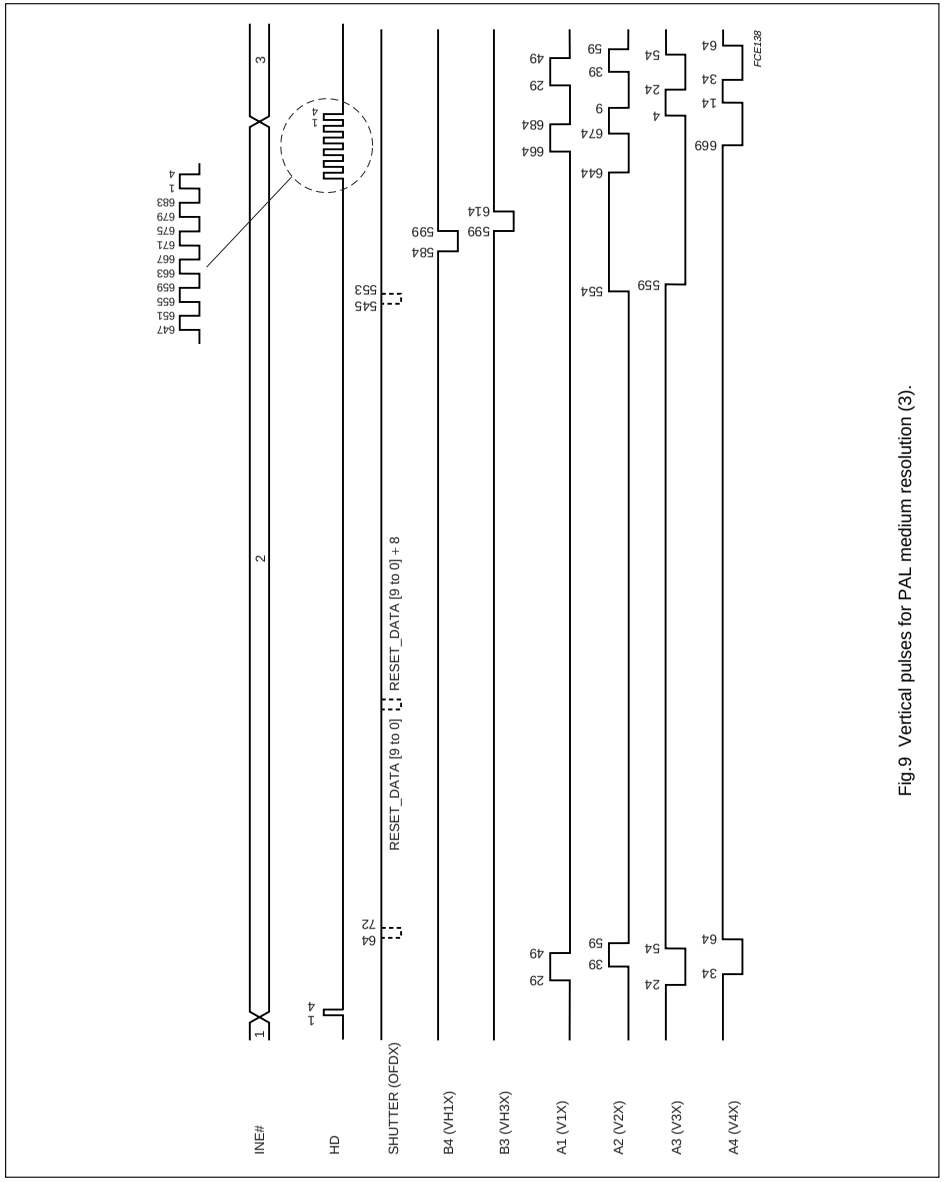


Fig.9 Vertical pulses for PAL medium resolution (3).

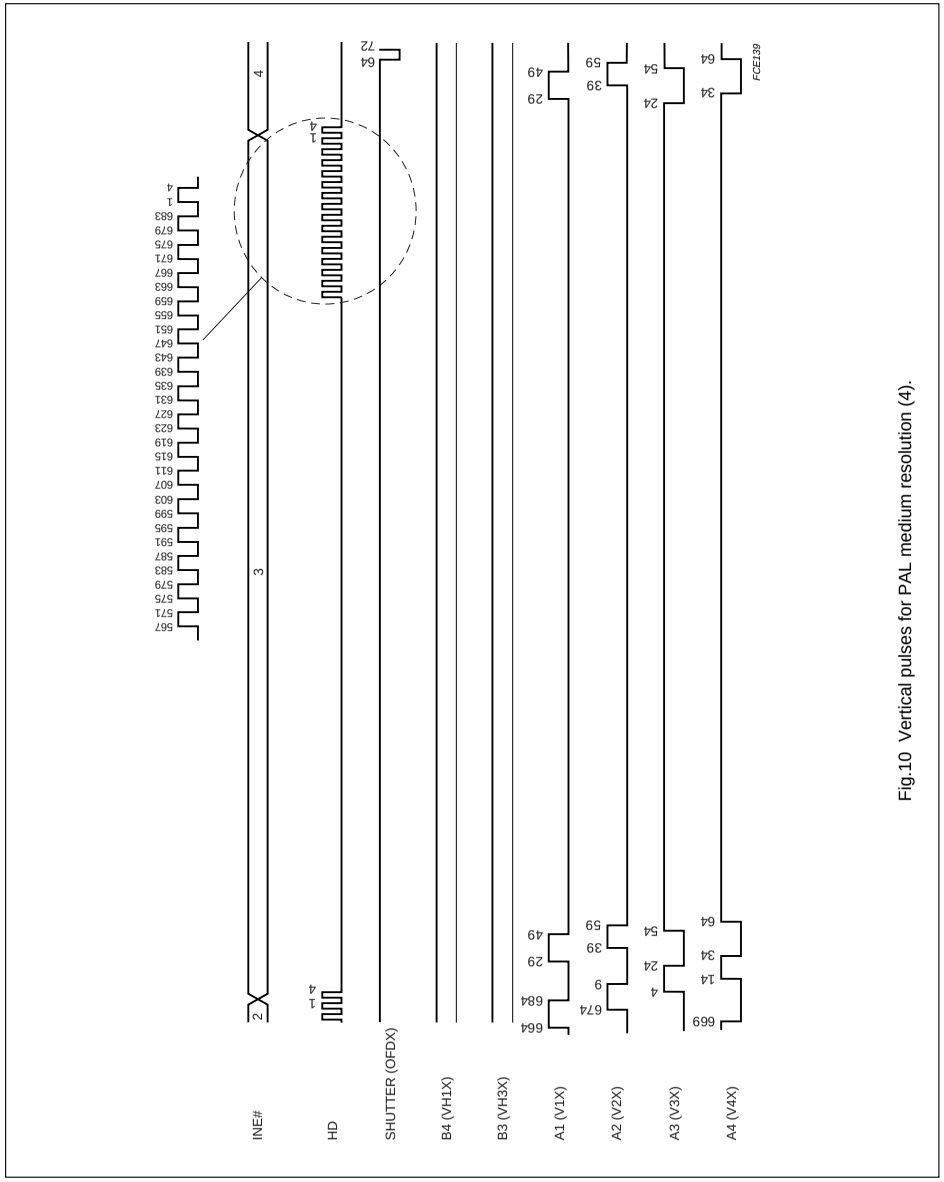


Fig.10 Vertical pulses for PAL medium resolution (4).

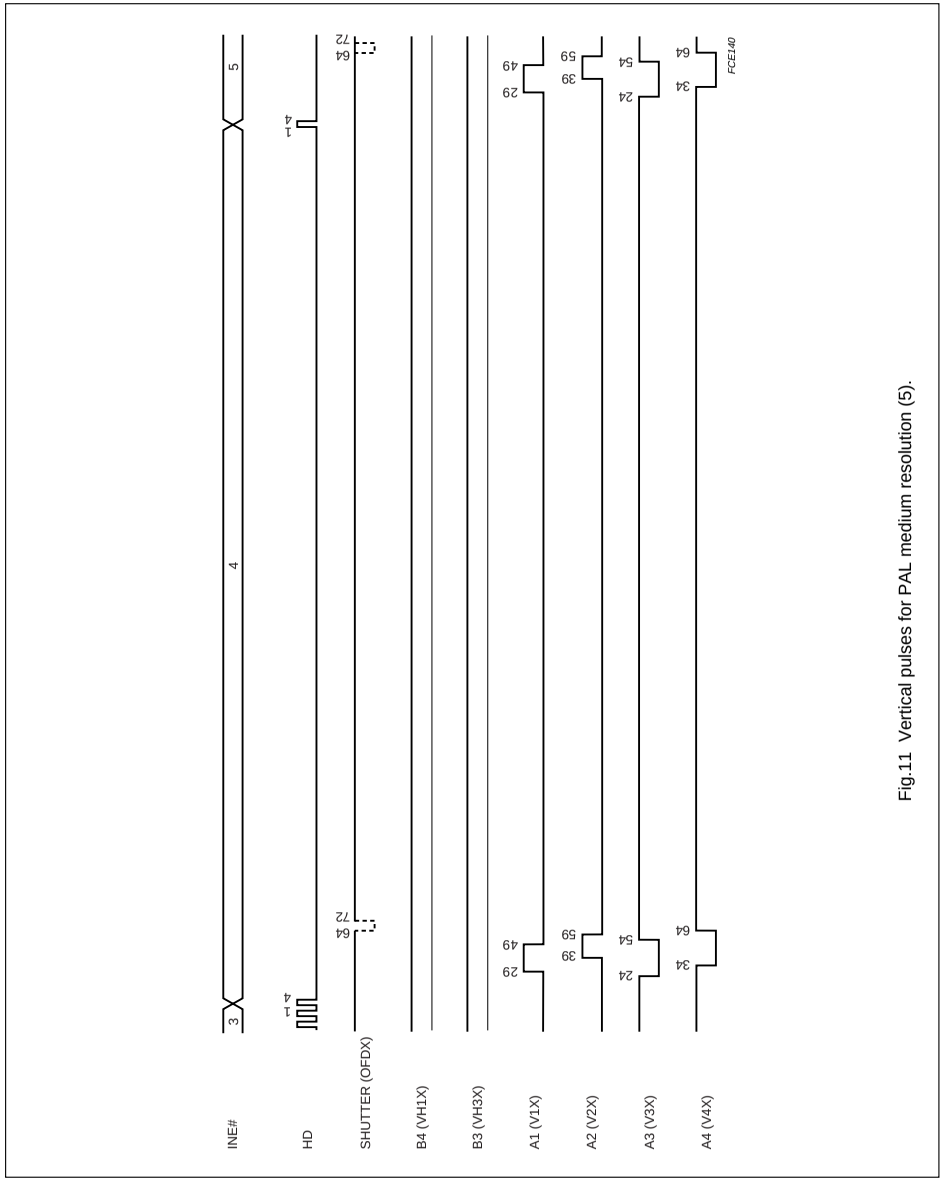


Fig.11 Vertical pulses for PAL medium resolution (5).

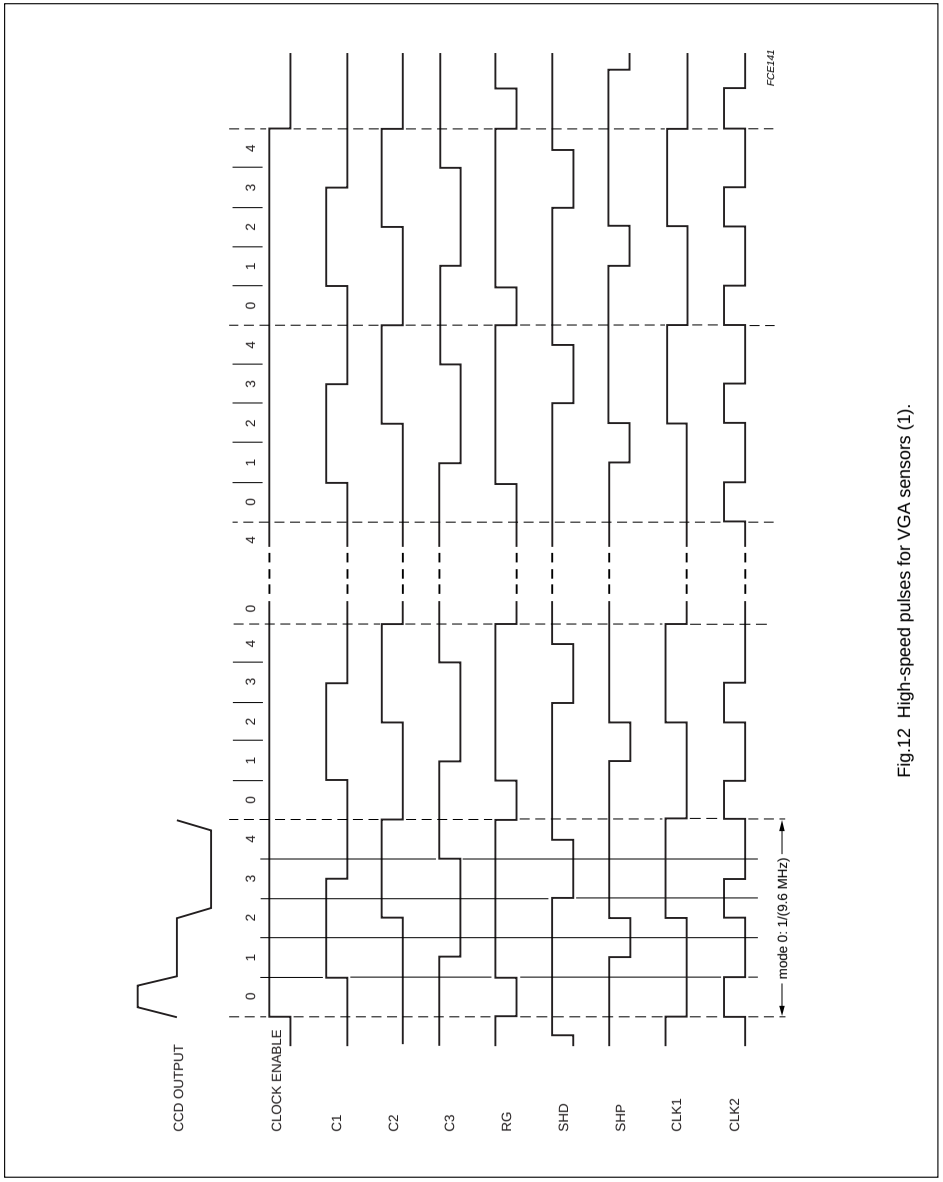


Fig.12 High-speed pulses for VGA sensors (1).

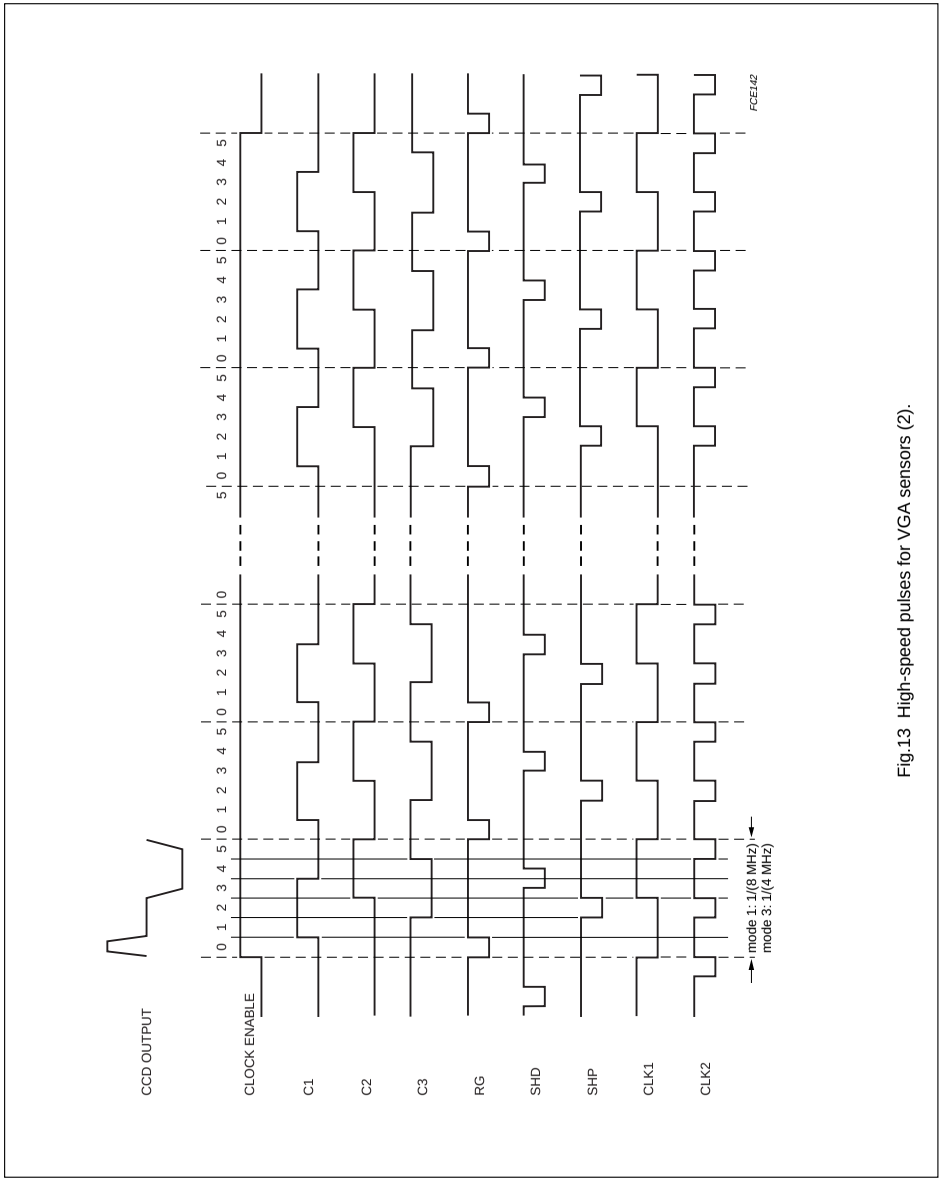


Fig.13 High-speed pulses for VGA sensors (2).

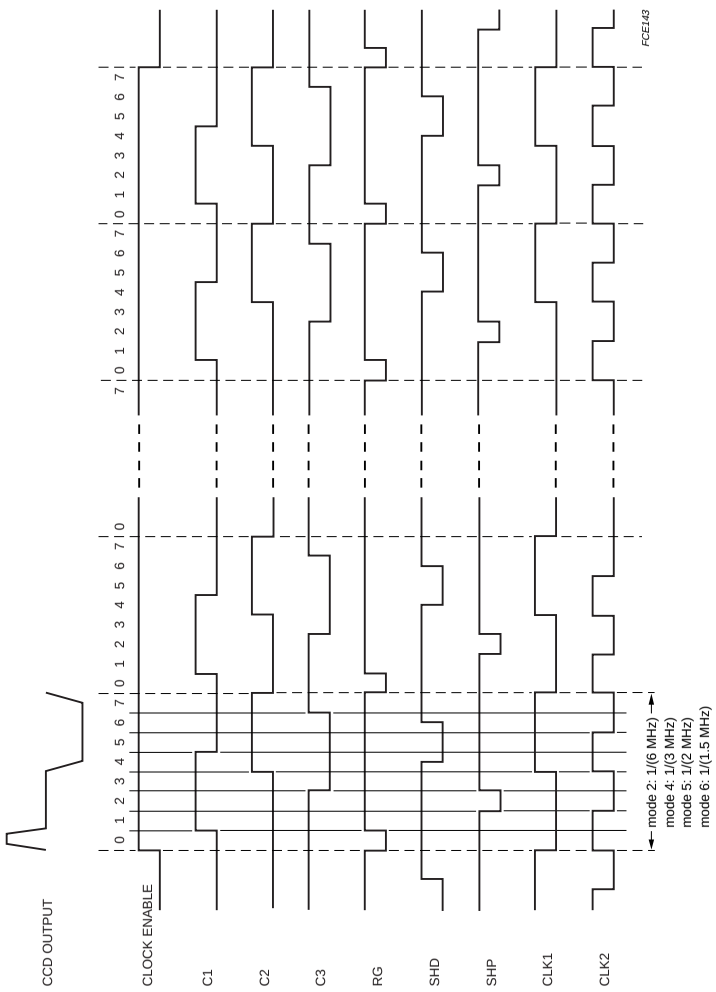


Fig.14 High-speed pulses for VGA sensors (3).

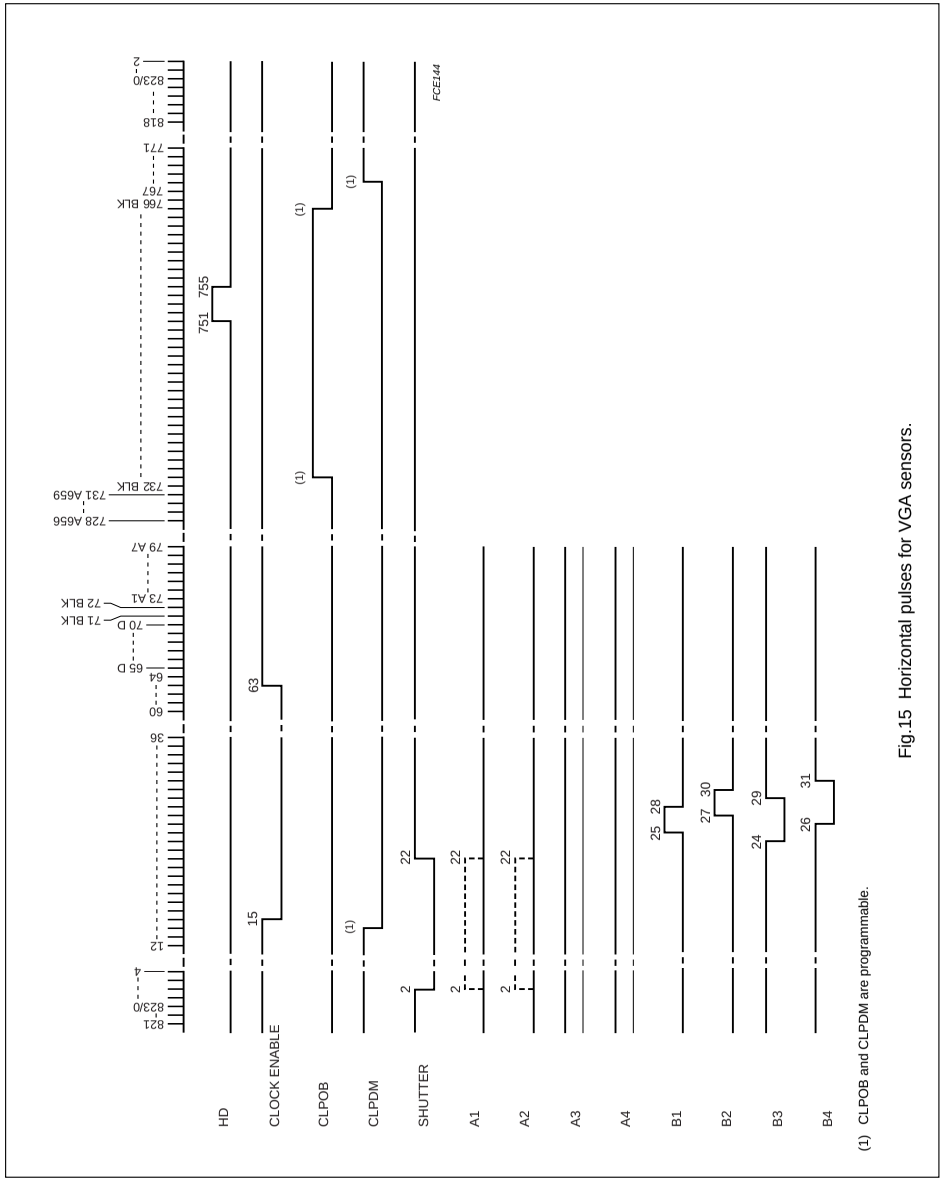


Fig.15 Horizontal pulses for VGA sensors.

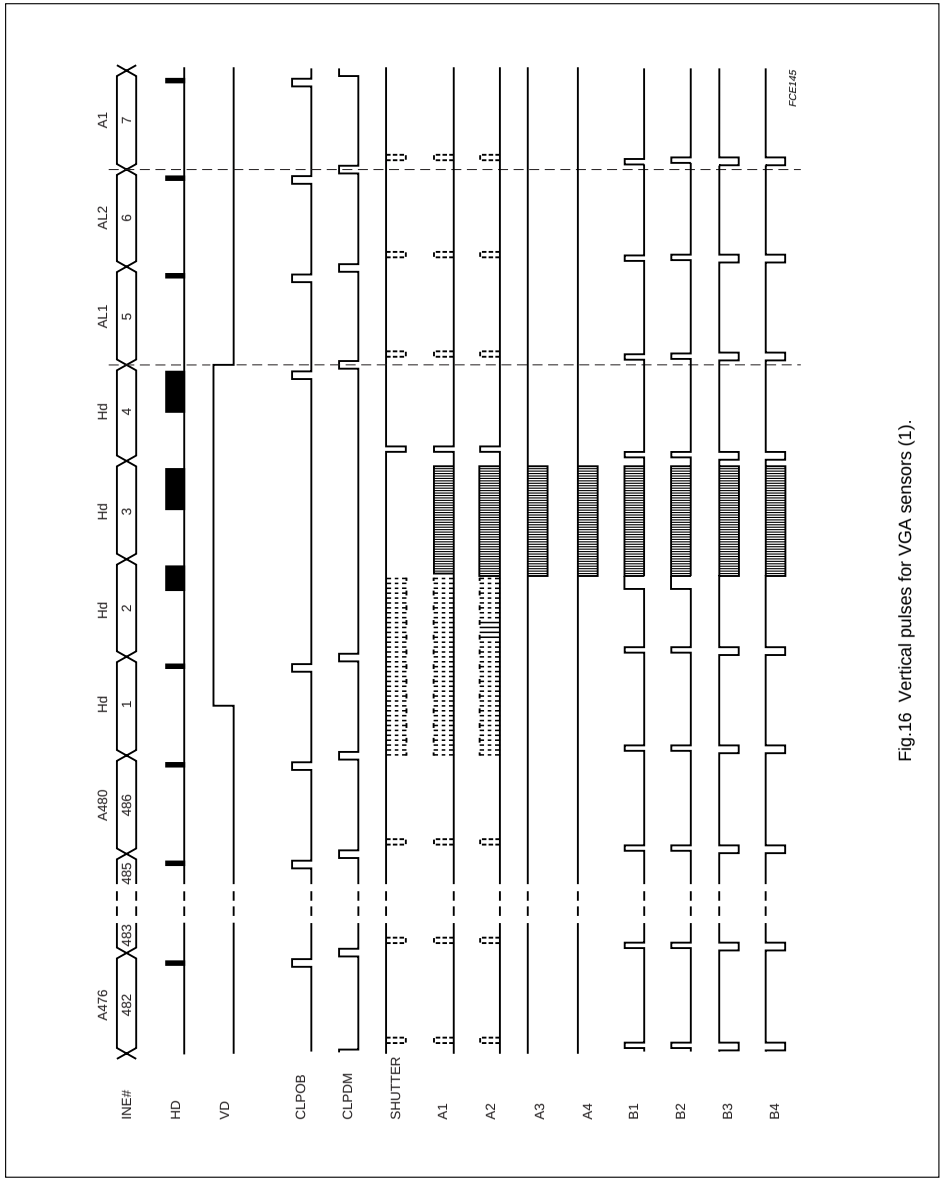


Fig.16 Vertical pulses for VGA sensors (1).

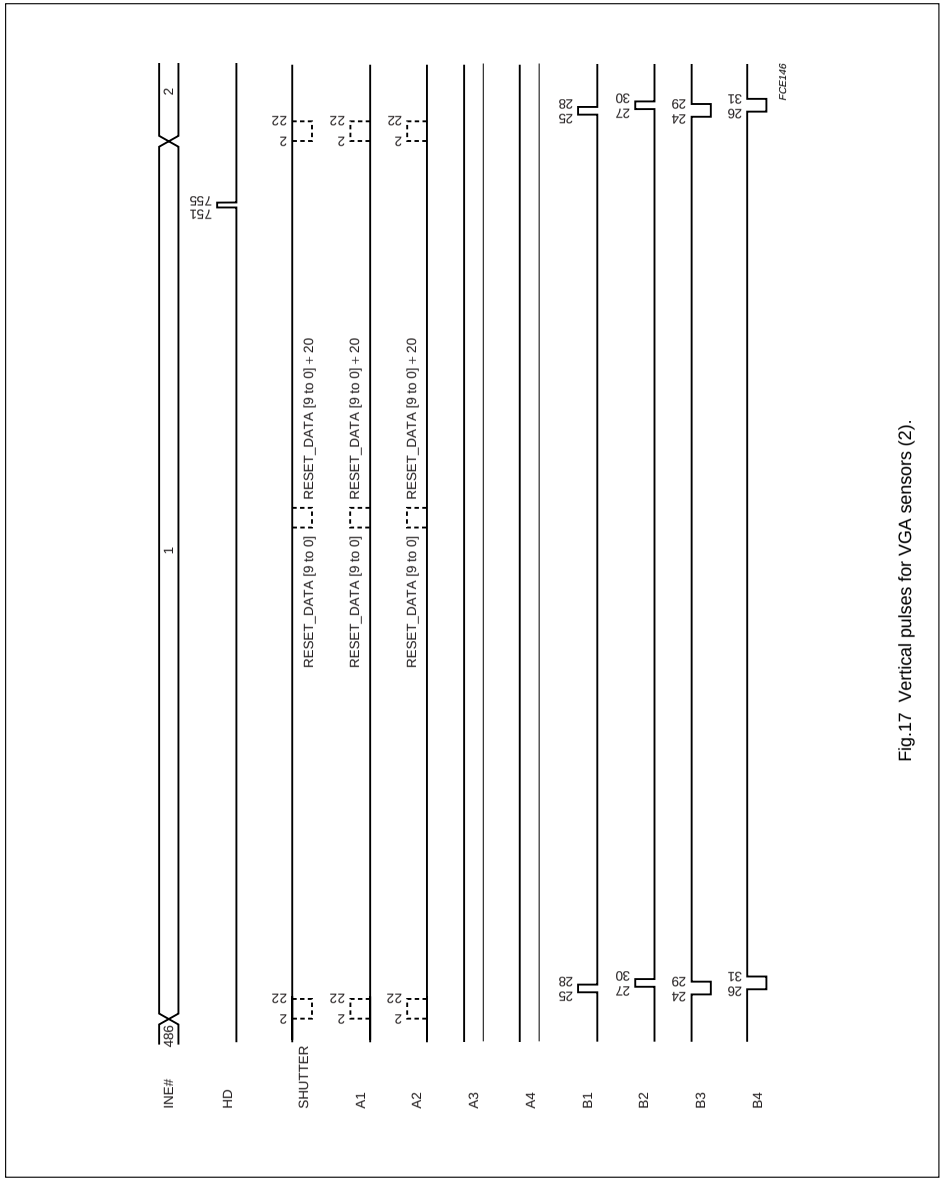


Fig.17 Vertical pulses for VGA sensors (2).

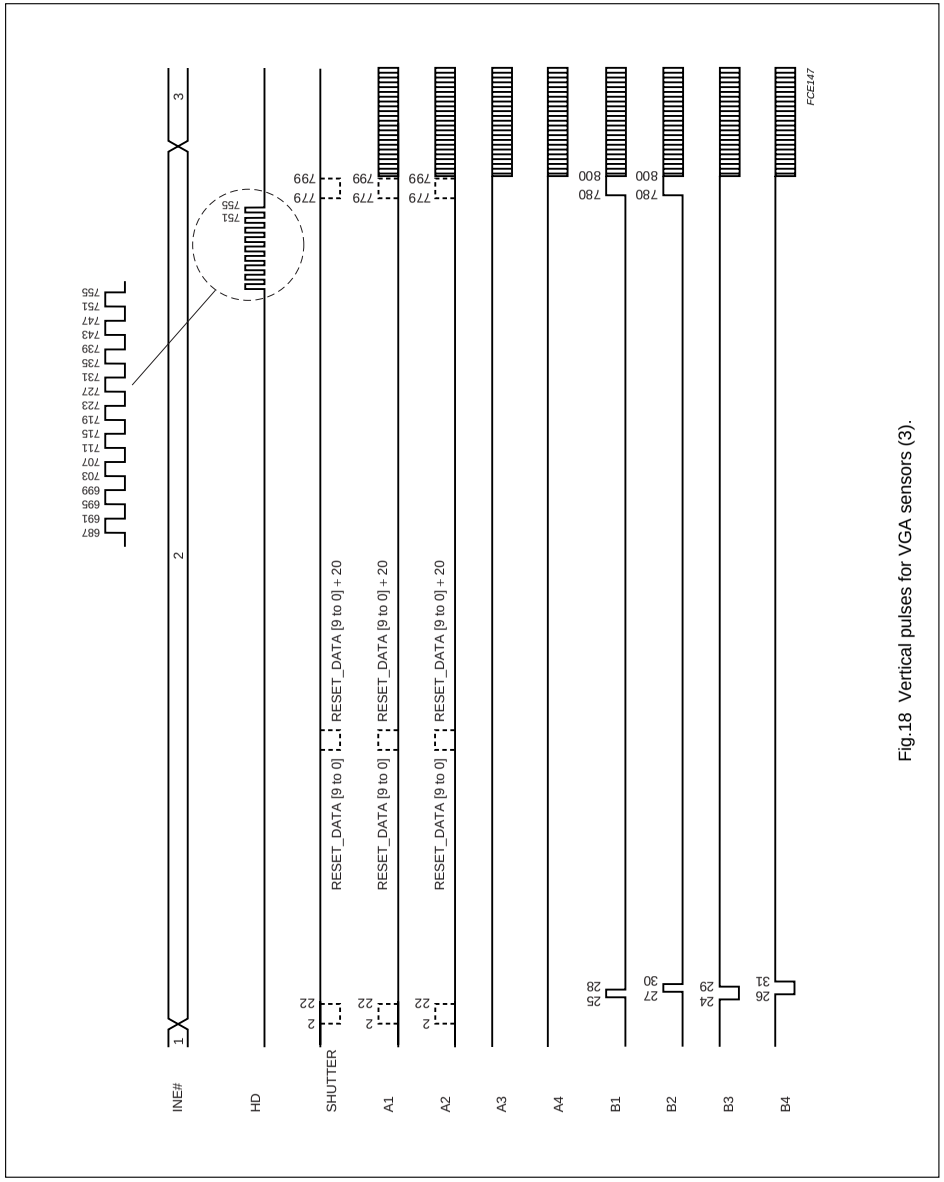


Fig.18 Vertical pulses for VGA sensors (3).

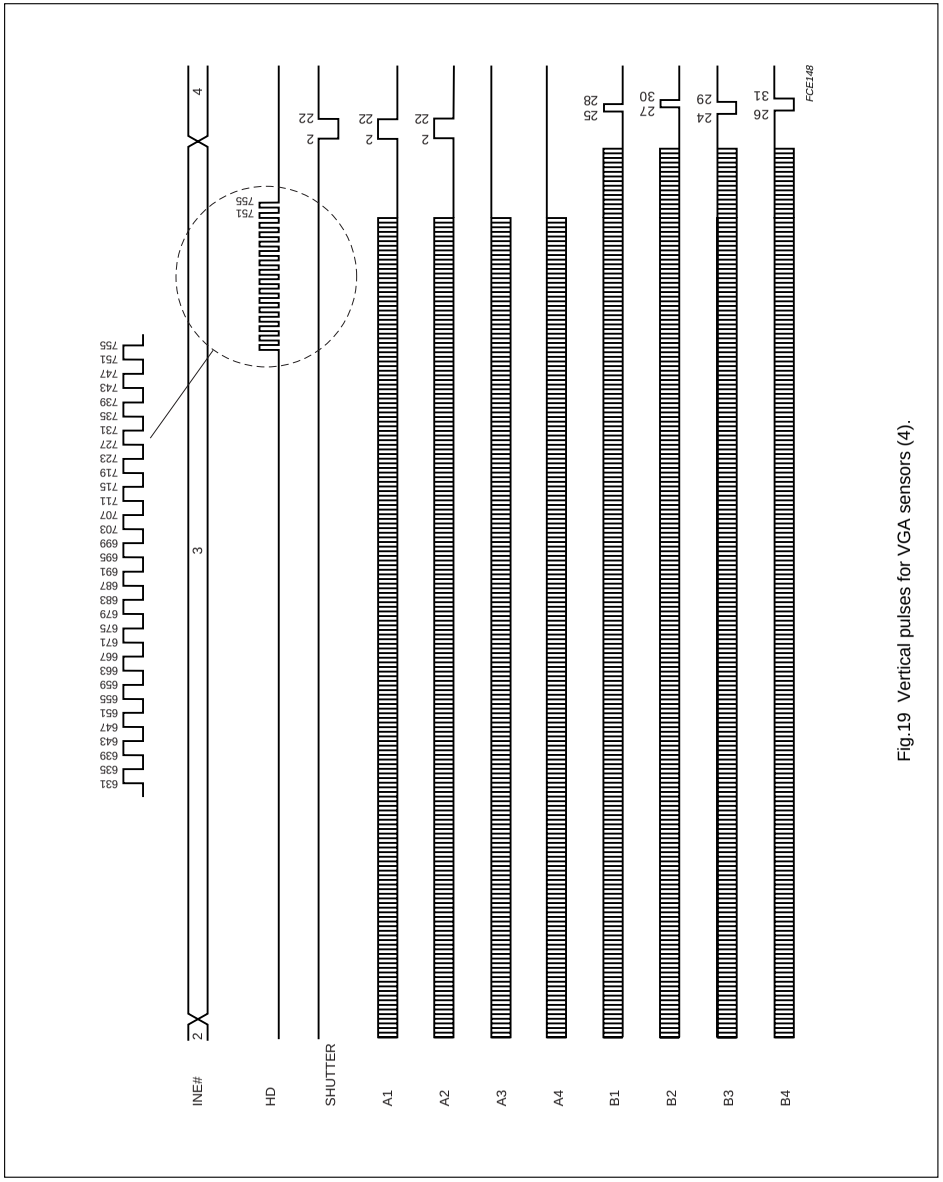


Fig.19 Vertical pulses for VGA sensors (4).

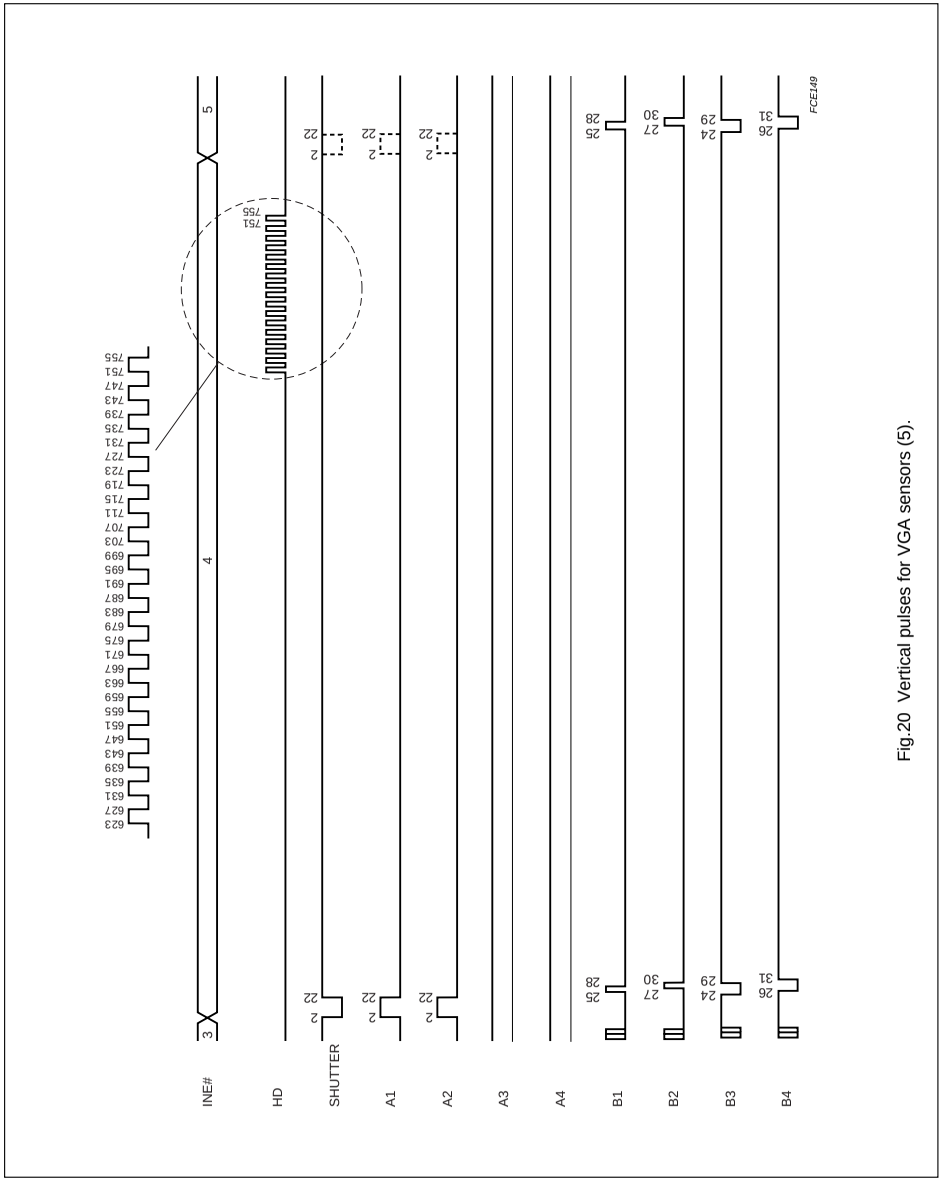


Fig.20 Vertical pulses for VGA sensors (5).

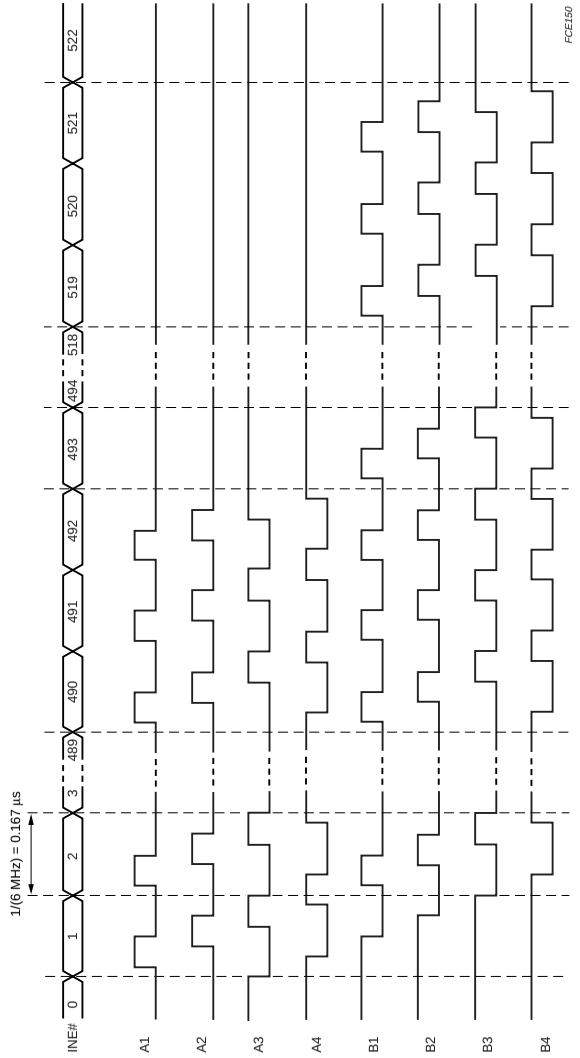


Fig.21 Vertical pulses for VGA sensors (6).

8.8 USB video FIFO

The USB video FIFO is programmed via the I²C-bus (see Fig.22). The FIFO is designed to achieve three different packets containing video on the isochronous USB channel. Video data is contained in a chain of equally sized USB packets, except for the last packet of a video frame which is always smaller. The video frames can be separated from each other by one or more 0-length packets. For low frame rates (below 10 frames/s) there are always 0-length packets in the stream. The host can synchronize on the smaller packets for the high frame rates and on the 0-length packets for the low frame rates.

For every mode the FIFO must be adjusted. There are three parameters to program the video FIFO:

- I²C_Packet_Size: this value indicates the length of all packets with video data except for the last packet of a video frame
- I²C_FIFO_Offset: this value indicates the number of data in the FIFO before a new packet is transmitted over the USB
- I²C_Read_Spacing: this value indicates the number of 12 MHz clock cycles between read actions from the FIFO.

Moreover the FIFO is enabled and disabled with I²C_Active.

The write process to the FIFO is controlled by the transfer buffer and is not programmable.

The read process is executed in the PSIE-MMU and is driven by the USB frame interval (1 ms). Every frame interval the PSIE-MMU tries to read I²C_Packet_Size bytes from the FIFO. This read process will not be started when a new video frame is stored in the FIFO and there are less than I²C_FIFO_Offset bytes written. The read process stops if the next bytes are of another video frame, or if the read-pointer overtakes the write-pointer.

I²C_Read_Spacing determines the read rate. Its value can easily be determined with the formula:

$$I^2C\_Read\_Spacing < \frac{12000}{I^2C\_Packet\_Size}$$

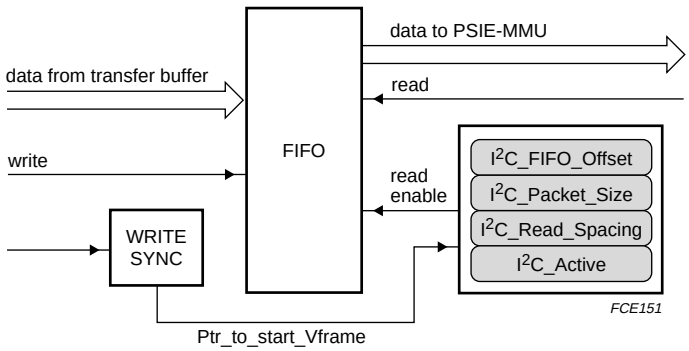


Fig.22 USB video FIFO.

8.9 PSIE-MMU, I²C-bus interface and USB RAM space

The Programmable Serial Interface Engine (PSIE) and Memory Management Unit (MMU) is the heart of the USB protocol hardware (see Fig.23). It formats the actual packets that are transferred to the USB and passes the incoming packets to the right end-point buffers. These buffers are allocated as part of the USB RAM space.

The microcontroller communicates via the I²C-bus with the PSIE-MMU. The I²C-bus protocol distinguishes three register spaces. These spaces are addressed via different commands. The command is sent to the command address. Depending on the command it is sent to the PSIE-MMU and/or to the command interpreter which configures the (de-)mux to open the path to the right register space. Subsequent write/read to/from the data address store or retrieve data from the register space is selected by the command.

8.10 ATX and external ATX interface

The SAA8117HL contains an analog bus driver, called the ATX. It incorporates a differential and two single-ended receivers and a differential transmitter. The interface to the bus consists of a differential data pair (ATXDM and ATXDP). The SAA8117HL contains also an interface to an external ATX as backup solution.

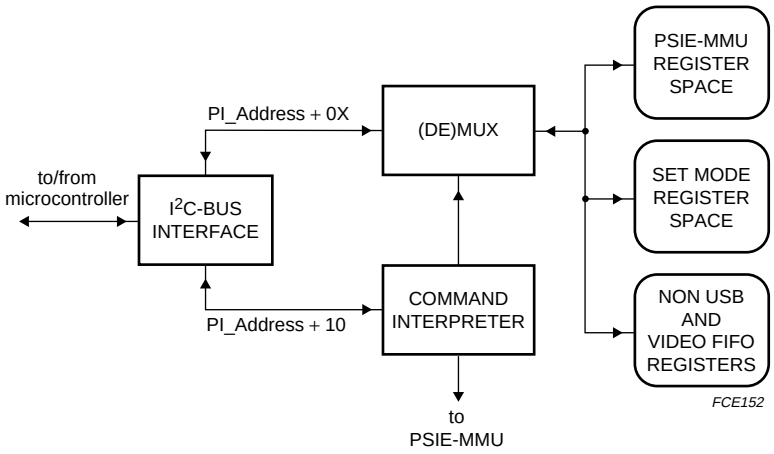


Fig.23 I²C-bus interface and register map.

8.11 Audio

The PLL converts the 48 MHz to 256f_s (f_s = audio sample frequency). There are three modes for the PLL to achieve the sample frequencies of 48, 44.1 or 32 kHz (see Table 1).

In the Fixed Gain Amplifier (FGA) the microphone input is amplified by 20 dB.

The bit stream ADC samples the audio signal. It runs at an oversample rate of 256 times the base sample rate. In the application, the bit stream can be converted to parallel 16-bit samples. This conversion is programmable with respect to the effective sample frequency (dropping sample results in a lower effective sample frequency) and sample resolution. As a result the effective sample rate can be determined.

Table 1 ADC clock frequencies and sample frequencies

CLOCK (MHz)	DIVIDING NUMBER	SAMPLE FREQUENCY (kHz)	ADC CLOCK (MHz)
8.1920	1	32	4.096
	2	16	2.048
	4	8	1.042
	8	note 1	note 1
11.2996	1	44.1	5.6448
	2	22.05	2.8224
	4	11.025	1.4112
	8	5.5125	0.7056
12.2880	1	48	6.144
	2	24	3.072
	4	12	1.536
	8	6	0.768

Note

1. Not supported.

8.12 Power management

The USB requires the device to switch power states. The SAA8117HL contains a power management module since the device may not consume more than 500 μA during the power state called SUSPEND. This requires that even the crystal oscillator must be switched off. The SAA8117HL is also not functional except for some logic that enables the IC to wake-up the camera. After wake-up of the SAA8117HL first the clock to the microcontroller is generated and thereafter an interrupt is generated to wake-up the controller. Therefore the clock of the microcontroller is generated by the SAA8117HL.

The power management module also sets a flag in register I^2C_SET_MODE_AND_READ. After a reset the microcontroller should check this register via the I^2C-bus and find the cause of the wake-up. Different causes may require different start-up routines.

The internal video processing core uses another V_{DDD} domain which can be switched during SUSPEND.

The PPG is switched off by setting SN_Resume and resetting SN_PAL_VGA. In non CIF modes the power consumption is reduced by resetting SN_Compress and SN_CLK_Compress_On.

The SAA8117HL has the feature to independently wake-up from SUSPEND, but requires a signal from the microcontroller before going into SUSPEND (via the signal on pin SUSREADYNOT).

Since the main oscillator of the SAA8117HL is switched off during SUSPEND precautions are needed to avoid undefined states when the clock is switched on. This is ensured via the pins CLOCKON and TRC.
Pin CLOCKON goes HIGH as soon as the main oscillator is switched on. The oscillator will need some time to make a stable 48 MHz signal. However, the clock is only passed through to other parts of the SAA8117HL when the level on pin TRC reaches a certain threshold. The time needed to reach the threshold can be trimmed with an RC-circuit.

9 CONTROL REGISTER DESCRIPTION

This Chapter gives an overview of all registers.

9.1 SNERT (UART)

The following registers are accessible via SNERT (see Table 2).

Table 2 SNERT write registers of the SAA8117HL

ADDRESS	NAME	FUNCTION	FORMAT
C0	–	reserved	–
C1	–	reserved	–
C2	CONTROL17_0	various control bits	see Table 3
C3	CONTROL17_1	various control bits	see Table 5
C4	VP_SQCIF_OFFSET	vertical (MSN) and horizontal (LSN) offset for sub-QCIF mode	nibble
C5	CONTROL17_2	various control bits	see Table 6
C6	PPG_SHUTTERSPEED_0	bits of shutter speed 0	see Table 8
C7	PPG_SHUTTERSPEED_1	bits of shutter speed 1	see Table 9
C8	PPG_CLPOB_START_LSB	LSB start position control for CLPOB pulse	byte
C9	PPG_CLPOB_STOP_LSB	LSB stop position control for CLPOB pulse	byte
CA	PPG_CLPDM_START_LSB	LSB start position control for CLPDM pulse	byte
CB	PPG_CLPDM_STOP_LSB	LSB stop position control for CLPDM pulse	byte
CC	CLPMSB	MSBs of CLPOB_Start, CLPOB_Stop, CLPDM_Start and CLPDM_Stop	see Table 10

Table 3 Detailed description of SNERT register CONTROL17_0 (address 0xC2)

7	6	5	4	3	2	1	0	PARAMETER
X								EIRRAH exchanges the chrominance irregularities when needed; toggle the bit to ensure timing of chrominance signal; the value must be determined experimentally (can be different for different modes)
	1							Snapshot transported in 4 : 2 : 2 format
	0							transported in 4 : 2 : 0 format
		1						Inband_Control in band synchronization words are inserted in the video data stream
		0						only active video data is transmitted over USB
			1					Compression_Ratio ratio is 4 times
			0					ratio is 3 times
				1				Compress compression is active; only to be used in case (for this register) bit 2 = 1 and bit 1 = 0 since compression functions are for CIF only; CIF format must be compressed unless the frame rate is 3.75 Hz
				0				compression module is switched off and power consumption is minimized for this module
					X	X		Output_Format_Select see Table 4
							1	PAL_VGA PAL sensor
							0	VGA sensor

Table 4 Detailed description of bit 2 and bit 1 of SNERT register CONTROL17_0

2	1	OUTPUT_FORMAT_SELECT PARAMETER	FRAME RATE WITH RESPECT TO OUTPUT FORMAT								
0	0	sub-QCIF	24	20	15	12	10	7.5	5	3.75	–
0	1	QCIF	24	20	15	12	10	7.5	5	3.75	–
1	0	CIF	–	–	15	12	10	7.5	5	3.75	–
1	1	VGA; note 1	–	–	–	–	–	–	–	–	0.9375

Note

1. Only valid when a VGA sensor is applied. The VGA output is not compressed.

Table 5 Detailed description of SNERT register CONTROL17_1 (address 0xC3)

7	6	5	4	3	2	1	0	PARAMETER
X	X	X	X					reserved
								CLK_Compress_On
				1				compression clock active
				0				compression module is brought to low power state
								Prefilter B_Comb
					1			horizontal scaling factor exceeds 3 (only functioning if bit 1 is also set to logic 1); this bit switches prefilter B to 13 taps
					0			prefilter B is as described for bit 1
								Prefilter B_On/Off
						1		horizontal scaling factor exceeds 2; the prefilter with 7 taps is switched on
						0		prefilter B is bypassed
								Prefilter A_On/Off
							1	prefilter A with 3 taps is on; must be set to logic 1 when bit 2 is set to logic 1 to obtain the overall wanted frequency response
							0	prefilter A is bypassed

Table 6 Detailed description of SNERT register CONTROL17_2 (address 0xC5)

7	6	5	4	3	2	1	0	PARAMETER
								PIX_nr0 to PIX_nr2
X	X	X						3 LSBs of 10 bits pixel number for autoexposure control (7 LSBs in register 0xC6)
								Shutter_Update_Buffer
			1					update of the shutter speed is buffered
			0					no buffering (immediately destroying of the current video frame)
								Resume
				1				video processing and PPG are switched of; if a VGA sensor is selected the vertical transport pulses are not switched off but this must be done by selecting a PAL sensor (register 0xC2 bit 0)
				0				PGG pulses generated
								PPG_Mode_Frame_Rate
					X	X	X	see Table 7

Table 7 Detailed description of bit 2 to bit 0 of SNERT register CONTROL17_2

BIT			PARAMETER OF PPG_MODE_FRAME_RATE	
2	**1**	**0**	**VGA**	**PAL**
0	0	0	24	24
0	0	1	20	20
0	1	0	15	15
0	1	1	10	12
1	0	0	7.5	10
1	0	1	5	7.5
1	1	0	3.75	5
1	1	1	0.9375	3.75

Table 8 Detailed description of SNERT register PPG_SHUTTERSPEED_0 (address 0xC6)

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**PARAMETER**
X								1 LSB of 9-bit line number (8 MSBs in register 0xC7)
	X	X	X	X	X	X	X	7 MSBs of 10-bit pixel number (3 LSBs in register 0xC5)

Table 9 Detailed description of SNERT register PPG_SHUTTERSPEED_1 (address 0xC7)

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**PARAMETER**
X	X	X	X	X	X	X	X	8 MSBs of 9-bit line number (LSB in register 0xC6)

Table 10 Detailed description of SNERT register CLPMSB (address0xCC)

7	**6**	**5**	**4**	**3**	**2**	**1**	**0**	**PARAMETER**
X	X							2 MSBs of CLPOB_Start (LSBs in register 0xC8)
		X	X					2 MSBs of CLPOB_Stop (LSBs in register 0xC9)
				X	X			2 MSBs of CLPDM_Start (LSBs in register 0xCA)
						X	X	2 MSBs of CLPDM_Stop (LSBs in register 0xCB)

9.2 I²C-bus interface

The I²C-bus interface uses two addresses:

- Command address for writing commands to the Memory Manager (MM)
- Data address for writing/reading data to/from the Memory Manager (MM).

The 6 MSBs of the two addresses are equal and are defined by the PI_address = 010111 (see Table 11). The LSBs of the addresses differentiate between the command address and the data address. When bit 1 is logic 1 the address is the command address (0x5E) and when bit 1 is logic 0 the address is one of the data addresses (0x5C or 0x5D).

Table 11 I²C-bus addresses

BIT								ADDRESS
7	6	5	4	3	2	1	0	
0	1	0	1	1	1	0	0	0x5C: for writing data to the memory manager
0	1	0	1	1	1	0	1	0x5D: for reading data from the memory manager
0	1	0	1	1	1	1	0	0x5E: for writing commands
0	1	0	1	1	1	1	1	0x5F: not in use

9.2.1 COMMANDS

The commands listed in Table 12 must be sent to the I²C-bus address 0x5E.

Table 12 I²C-bus USB command codes

BIT								FUNCTION
7	6	5	4	3	2	1	0	
0	0	end-point number						select end-point
0	1	end-point number						read/write status
1	0	end-point number						initialize/read status information
1	1	0	1	address				read/write register bank
1	1	1	0	0	X	X	X	not used
1	1	1	0	1	0	0	0	set non-USB register
1	1	1	1	0	0	0	0	read/write data
1	1	1	1	0	0	0	1	acknowledge setup
1	1	1	1	0	0	1	0	set buffer empty
1	1	1	1	1	0	1	0	set buffer full
1	1	1	1	0	1	0	0	read interrupt register
1	1	1	1	0	1	0	1	read current frame number
1	1	1	1	0	1	1	0	send resume
1	1	1	1	0	1	1	1	set status change bits
1	1	1	1	0	0	1	1	set mode

Table 13 Set mode and write register overview

BYTE	SET MODE AND WRITE
1	N1 timer; programmable timer for power management; counts 12 MHz cycles; must be bigger than number of cycles needed for the microcontroller to go in power-down state after pin SUSREADYNOT is made LOW
2	N2 timer; programmable timer for power management; counts 12 MHz cycles; determines the time between when the microcontroller clock is switched off and the main clock is switched off
3	PSIE-MMU control byte (see Table 14)

Table 14 Detailed description of PSIE-MMU control byte (byte 3)

7	6	5	4	3	2	1	0	PARAMETER
X	X	X						reserved
								interrupt after isochronous audio transfer
			1					for each isochronous audio transfer an interrupt to the microcontroller will be generated; default set to logic 1 upon general Power-on reset and/or bus reset by the SAA8117HL
			0					no interrupts are given to the microcontroller
								interrupt after isochronous video transfer
				1				for each isochronous video transfer an interrupt to the microcontroller will be generated; default set to logic 1 upon general Power-on reset and/or bus reset by the SAA8117HL
				0				no interrupts are given to the microcontroller
								audio end-point
					1			audio end-point enabled; default set to logic 1 upon general Power-on reset and/or bus reset by the SAA8117HL
					0			audio end-point disabled; the PSIE-MMU will not react on in-tokens on the audio end-point
								video end-point
						1		video end-point enabled; default set to logic 1 upon general Power-on reset and/or bus reset by the SAA8117HL
						0		video end-point disabled; the PSIE-MMU will not react on in-tokens on the video end-point
								error debug mode
							1	interrupts are generated only in the event that the transfer is not successfully completed; the microcontroller can read data from the interrupt and status registers to see the cause of this error
							0	all successful USB transactions are reported to the microcontroller via an interrupt; default set to logic 0 upon general Power-on reset by the SAA8117HL

Table 15 Detailed description of PSI-MMU set mode and status byte

7	6	5	4	3	2	1	0	PARAMETER
X	X	X	X					reserved
								remote wake-up status flag
				1				remote wake-up when device is in SUSPEND mode
				0				no remote wake-up
								resume status flag
					1			bus resume by the host when device is in SUSPEND mode
					0			no bus resume
								bus reset status flag
						1		bus reset
						0		no bus reset
								power-up status flag
							1	general power up reset
							0	no power up reset

9.2.2 END-POINTS

The SAA8117HL has 6 logical end-points which are listed in Table 16.

Table 16 Mapping of logic to physical end-point numbers for used end-points

END-POINT NAME	LOGIC END-POINT	BUFFER SIZE	PHYSICAL END-POINT	
			OUT	IN
Control end-point	0	8	0	1
Control end-point	1	8	2	3
Interrupt end-point	2	8	–	4
Interrupt end-point	3	8	–	5
Iso video end-point	4	96.0	–	6
Iso video end-point	5	35.1	–	7

9.2.3 CONTROL TOP REGISTERS

The following registers can be written on I²C-bus address 1 after the command 0xE8 on I²C-bus address 0.

Table 17 I²C-bus control top registers (base address 0x08)

ADDRESS	NAME	FUNCTION
0x08	CLKSHOP CONTROL	clock control
0x09	RSTGEN AND_PLL CONTROL	reset control
0x0A	I/O MUX CONTROL	mux block control
0x0B	POWER CONTROL ANALOG MODULES	power-on analog modules control

Table 18 Detailed description of I²C-bus control top register CLKSHOP CONTROL (address 0x08)

7	6	5	4	3	2	1	0	PARAMETER
								select ADC clock source
1								sel_ad: clock generated from ADC
0								sel_pll: clock generated from PLL
								set clock dividers for ADC
	0	0						set_divide00: divided by 1
	0	1						set_divide01: divided by 2
	1	0						set_divide10: divided by 4
	1	1						set_divide11: divided by 8
			X					reserved
								disable 48 MHz clock
				1				dis_clk_48: disable 48 MHz clock
				0				enable clock
								disable receiver clock
					1			dis_clk_rec: disable receiver clock
					0			enable clock
								disable ADC clock
						1		dis_clk_ad: disable ADC clock
						0		enable clock
							X	reserved

Table 19 Detailed description of I²C-bus control top register RSTGEN AND PLL CONTROL (address 0x09)

7	6	5	4	3	2	1	0	PARAMETER
								set PLL frequency
0	0							fcode00: 256 × 44.1 kHz
0	1							fcode01: 256 × 32 kHz
1	0							fcode10: 256 × 48 kHz
1	1							fcode11: 256 × 44.1 kHz
		X	X					reserved
								reset PSIE-MMU top module
				1				upc_rst_mmu: resetting the USB protocol block (called PSIE-MMU) during tests or in the event of errors
				0				no reset
					X			reserved
								reset ADIF top module
						1		upc_rst_adif: resetting the digital audio part during tests or in the event of errors
						0		no reset
								reset AGC module
							1	upc_rst_AGC: resetting the AGC control during tests or in the event of errors
							0	no reset

Table 20 Detailed description of I²C-bus control top register I/O MUX CONTROL (address 0x0A)

7	6	5	4	3	2	1	0	PARAMETER
X	X	X	X	X	X	X	X	reserved

Table 21 Detailed description of I²C-bus control top register POWER CONTROL OF ANALOG MODULES (address 0x0B)

7	6	5	4	3	2	1	0	PARAMETER
X	X							reserved
								power control PLL module
		1						upc_pll_off: PLL power off
		0						power on
			X					reserved
								power control ADC module left channel
				1				upc_adl_off: power off
				0				power on
								power control ADC module right channel
					1			upc_adr_off: power off
					0			power on
								power control AGC module left channel
						1		upc_AGCl_off: power off
						0		power on
								power control AGC module right channel
							1	upc_AGCr_off: power off
							0	power on

9.2.4 VIDEO FIFO REGISTERS

Table 22 Overview of I²C-bus video FIFO registers (base address 0x04)

ADDRESS	NAME	FUNCTION
0x04	FIFO OFFSET	8 LSBs of the offset value
0x05	FIFO ACTIVE AND FIFI OFFSET	FIFO active and 3 MSBs of the offset value
0x06	PACKET SIZE	8 LSBs of packet size value
0x07	READ SPACING AND PACKET SIZE	read spacing and 2 MSBs of packet size value

Table 23 Detailed description of I²C-bus video FIFO register FIFO OFFSET (address0x04)

7	6	5	4	3	2	1	0	PARAMETER
X	X	X	X	X	X	X	X	FIFO offset mode_fifo_offset: sets the minimum contents of the FIFO that has to be reached, before a new video frame will be put on the USB bus. This value can be set between 0 and 2047. Total of 11 bits with 8 LSBs in this register and 3 MSBs in register 0x05.

Table 24 Detailed description of I²C-bus video FIFO register FIFO ACTIVE AND FIFI OFFSET (address 0x05)

7	6	5	4	3	2	1	0	PARAMETER
1								FIFO active mode_active: FIFO is active and the contents of the other mode registers should not be updated by the microcontroller (maledictive)
0								FIFO not active
	X	X	X	X				reserved
					X	X	X	FIFO offset 3 MSBs of the offset value; see also register 0x04

Table 25 Detailed description of I²C-bus video FIFO register PACKET SIZE (address 0x06)

7	6	5	4	3	2	1	0	PARAMETER
X	X	X	X	X	X	X	X	packet size mode_packet_size: sets the packet size of the USB video channel. Packets can vary in size between 0 and 1023. Total of 10 bits with 8 LSBs in this register and 2 MSBs in register 0x07.

Table 26 Detailed description of I²C-bus video FIFO register READ SPACING AND PACKET SIZE (address 0x07)

7	6	5	4	3	2	1	0	PARAMETER
X	X	X	X	X	X			read spacing mode_read_spacing: sets the periodicity of the read pulses; the periodicity can be set from 1 to 63 (from ‘000001’ to ‘111111’)
						X	X	packet size mode_packet_size: 2 MSBs of the value (8 LSBs in register 0x06)

9.2.5 ADIF TOP REGISTERS

Table 27 Overview of I²C-bus ADIF top registers (base address 0x0C)

ADDRESS	NAME	FUNCTION
0x0C	AGC CONTROL GENERAL	AGC control general
0x0D	AGC CONTROL GAIN LEFT	AGC control gain left
0x0E	AGC CONTROL GAIN RIGHT	AGC control gain right
0x0F	ADIF CONTROL	I²S-bus input and ADIF2MMU

Table 28 Detailed description of I²C-bus ADIF top register ADIF CONTROL (address 0x0F)

7	6	5	4	3	2	1	0	PARAMETER
X								reserved
								number of bytes per sample
	0	0						0 (reserved)
	0	1						1 (8 bits audio samples)
	1	0						2 (16 bits audio samples)
	1	1						3 (24 bits audio samples)
								selection mono/stereo operation
			0					mono
			1					stereo
								selection input for ADC path (ADIF mux)
				0				digital input (from I²S-bus)
				1				analog input (from Vin_left and Vin_right)
								selection high-pass filter (DC filter) for ADC down-sample filter
					0			high-pass filter off
					1			high-pass filter on
								selection UDAI serial input format
						0	0	I²S-bus
						0	1	LSB justified, 16 bits
						1	0	LSB justified, 18 bits
						1	1	LSB justified, 20 bits

10 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDA}	analog supply voltage		–0.5	+4.0	V
V_{DDD}	digital supply voltage		–0.5	+4.0	V
V_n	voltage on				
	pins AGND and DGND		–0.5	+4.0	V
	pins SCL and SDA	note 1	–0.5	+5.5	V
	all other pins		–0.5	V_{DD} + 0.5	V
T_{stg}	storage temperature		– 55	+150	°C
T_{amb}	operating ambient temperature		0	70	°C
T_j	junction temperature		–40	+125	°C

Note

1. 5 V tolerant buffers.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	51	K/W

12 CHARACTERISTICS

V_{DDD} = V_{DDA} = 3.3 V ±10%; T_{amb} = 0 to 70 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDD}	digital supply voltage		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
V_{DGND}	voltage on pins DGND		0	0	0	V
V_{AGND}	voltage on pins AGND		0	0	0	V
I_{DDD}	digital supply current	T_{amb} = 25 °C	–	70	–	mA
I_{DDA}	analog supply current	T_{amb} = 25 °C	–	20	–	mA
T_{amb}	operating ambient temperature		0	25	70	°C
Inputs						
DATA AND CONTROL INPUTS: PINS M0 TO M2, YUV0 TO YUV7, LLC, HREF, VSYNC, RESET, GENPOR, ATXCTRL, RCV, VM0 AND VP0						
V_{IL}	LOW-level input voltage		–	–	0.8	V
V_{IH}	HIGH-level input voltage		2	–	–	V
Outputs						
DATA AND CONTROL OUTPUTS: PINS CLK2, SMP, SPEED, SUSPEND, VM, VP AND OEBAR						
V_{OL}	LOW-level output voltage		–	–	$0.1V_{DDD}$	V
V_{OH}	HIGH-level output voltage		$0.85V_{DDD}$	–	–	V
CONTROL OUTPUTS: PINS RG, SHUTTER, C1 TO C3, CLK1, SHP AND SHD						
V_{OL}	LOW-level output voltage		–	–	0.8	V
V_{OH}	HIGH-level output voltage		2.0	–	–	V
CONTROL OUTPUTS: PINS A1 TO A4 AND B1 TO B4						
V_{OL}	LOW-level output voltage		–	–	0.8	V
V_{OH}	HIGH-level output voltage		2.6	–	–	V
CONTROL OUTPUTS: PINS CLPDM AND CLPOB						
V_{OL}	LOW-level output voltage		–	–	0.6	V
V_{OH}	HIGH-level output voltage		2.2	–	–	V
Interfaces						
I^2S-BUS: PINS DA, BCK AND WS						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDD}$	–	–	V
I^2C-BUS AND SNERT BUS: PINS SDA, SCL, SNDA, SNCL AND SNRES						
V_{IL}	LOW-level input voltage		–	–	0.7	V
V_{IH}	HIGH-level input voltage		$0.2V_{DDD}$ + 0.9	–	V_{DDD} + 0.5	V
V_{OL}	LOW-level output voltage	note 1	–	–	0.4	V
V_{OH}	HIGH-level output voltage	note 1	V_{DDD} – 0.7	–	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
MICROCONTROLLER INTERFACE: PINS SUSREADYNOT, UCPOR, UCINT, CLOCK, CLOCKON, TRC, SNAPSHOT AND DCDCON						
V_{IL}	LOW-level input voltage	note 2	–	–	0.7	V
V_{IH}	HIGH-level input voltage	note 2	$0.2V_{DDD} + 0.9$	–	$V_{DDD} + 0.5$	V
V_{OL}	LOW-level output voltage	note 3	–	–	0.4	V
V_{OH}	HIGH-level output voltage	note 3	$V_{DDD} - 0.7$	–	–	V
Audio Phase-Locked Loop (PLL)						
f_i	clock input frequency		–	48	–	MHz
f_o	clock output frequency	note 4	–	11.2996	–	MHz
B	bandwidth		–	2.3	–	kHz
ζ	damping		–	0.98	–	
$\sum\Delta$ **convertor**						
INPUTS						
f_i	input signal frequency		1	–	20	kHz
$V_{i(rms)}$	input voltage (RMS value)		–	800	–	mV
TRANSFER FUNCTION						
N	order of the $\sum\Delta$		–	3	–	
N_{bit}	number of output bits		–	1	–	
N_{eqbit}	equivalent output resolution (bit)		–	16	–	
DR_i	dynamic range at input	note 5	–	96.6	–	dB
f_{clk}	clock frequency		–	–	5.6448	MHz
δ	clock frequency duty factor		–	50	–	%
Fixed Gain Amplifier (FGA)						
LOAD						
R_L	load resistance		5	–	–	kΩ
C_L	load capacitance		–	–	15	pF
TRANSFER FUNCTION						
$V_{i(nom)(p-p)}$	nominal input voltage (peak-to-peak value)		–	226.3	–	mV
A1	amplification		–	20	–	dB
$V_{o(nom)(rms)}$	nominal output voltage (RMS value)		–	800	–	mV
S/N	signal-to-noise ratio	note 6	–	60	–	dB
THD	total harmonic distortion	at HIGH-level; note 7	–	–65	–	dB
R_i	input impedance		3.35	4.7	6.0	kΩ
R_o	output impedance		–	–	100	Ω
f_i	input frequency	±3 dB range	100	–	20000	Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
BIASING						
I_{ref}	reference current		–	25	–	μA
FGA/∑Δ path						
TRANSFER FUNCTION						
A1	amplification		–	20	–	dB
S/N	signal-to-noise ratio		51	60	70	dB
THD	total harmonic distortion		–70	–66	–61	dB
ATX transceiver						
DRIVER CHARACTERISTICS IN FULL SPEED MODE: PINS ATXDP AND ATXDM						
$f_{o(sample)}$	audio sample output frequency		4	–	48	MHz
$t_{t(rise)}$	rise transition time	C_L = 50 pF	4	–	20	ns
$t_{t(fall)}$	fall transition time	C_L = 50 pF	4	–	20	ns
$t_{t(match)}$	transition time matching	note 8	90	–	110	%
$V_{o(cr)}$	output signal crossover voltage		1.3	–	2.0	V
Z_o	driver output impedance	steady state drive	30	–	42	Ω
RECEIVER CHARACTERISTICS IN FULL SPEED MODE: PINS ATXDP AND ATXDM						
f_s	audio sample input frequency		5	–	55	kHz
$f_{i(D)}$	data input frequency rate		–	12.00	–	Mbits/s
t_{frame}	frame interval		–	1.000	–	ms

Notes

1. This applies the outputs: pins SDA and SNDA.
2. This applies the inputs: pins SUSREADYNOT, TRC and SNAPSHOT.
3. This applies the outputs: pins CLOCK, UCINT, UCPOR, CLOCKON and DCDCON.
4. Frequencies depend on PLL settings (see Table 1).
5. Defined here as: $20 \times \log \frac{V_i}{V_{n(i)(eq)}}$ where V_i = input voltage and $V_{n(i)(eq)}$ = equivalent input noise voltage.
6. The noise is measured with A-weighting at the nominal input voltage.
7. The distortion is measured at a maximum output voltage of 2.4 V (p-p).
8. Transition time matching: $t_{t(match)} = \frac{t_{t(rise)}}{t_{t(fall)}}$

13 TIMING

V_{DDD} = V_{DDA} = 3.3 V ±10%; load capacitance = 10 pF; T_{amb} = 0 to 70 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data input related to LCC (see Fig.24)						
Pins YUV0 toYUV7, HREF and VSYNC						
$t_{su(i)(D)}$	data input set-up time		1	–	–	ns
$t_{h(i)(D)}$	data input hold time		1	–	–	ns
PPG high-speed pulses for PAL medium resolution sensors; mode 0 (see Fig.25)						
t_{d1}	delay between falling edge C2 and rising edge C1		–2	–1.5	0	ns
t_{d2}	delay between rising edge C2 and falling edge C1		1	1.5	2	ns
t_{d3}	delay between falling edge C1 and rising edge SHP		–3	–1.5	–1	ns
t_{d4}	delay between rising edge C1 and rising edge SHD		–0.5	0	+0.5	ns
t_{d5}	delay between rising edge C1 and falling edge RG		0.5	1	2	ns
t_{d6}	delay between falling edge CLK1 and rising edge C1		0	1	2	ns
t_{d7}	delay between rising edge CLK1 and falling edge C1		–0.5	0	+0.5	ns
t_{d8}	delay between rising edge CLK2 and rising edge C1		–2	0	+2	ns
$t_{WH(C1)}$	C1 pulse width HIGH		164	165	–	ns
$t_{WL(C2)}$	C2 pulse width LOW		166	167	–	ns
$t_{WL(SHP)}$	SHP pulse width LOW		81	82	–	ns
$t_{WL(SHD)}$	SHD pulse width LOW		81	82	–	ns
$t_{WL(RG)}$	RG pulse width LOW		83	84	–	ns
$t_{WL(CLK1)}$	CLK1 pulse width LOW		164	165	–	ns
$t_{WH(CLK2)}$	CLK2 pulse width HIGH		79	80	–	ns
t_r	rise time	note 1				
	pulse C1		–	4.5	–	ns
	pulse C2		–	4	–	ns
	pulse RG		–	4	–	ns
	pulse SHP		–	4	–	ns
	pulse SHD		–	4	–	ns
t_f	fall time	note 1				
	pulse C1		–	4	–	ns
	pulse C2		–	4	–	ns
	pulse RG		–	4	–	ns
	pulse SHP		–	4.5	–	ns
	pulse SHD		–	4.5	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
PPG high-speed pulses for VGA sensors (see Fig.26)						
t_{d1}	delay between rising edge C2 and rising edge C1		61	62	63	ns
t_{d2}	delay between rising edge C3 and rising edge C2		61	62	63	ns
t_{d3}	delay between rising edge SHP and falling edge C3		–1.5	–1	+0.5	ns
t_{d4}	delay between falling edge SHD and rising edge C2		8	9	10	ns
t_{d5}	delay between rising edge SHD and rising edge C3		–12	–11	–10	ns
t_{d6}	delay between rising edge RG and rising edge C1		–0.5	0	+0.5	ns
t_{d7}	delay between rising edge C1 and falling edge CLK1		18	19	21	ns
t_{d8}	delay between rising edge C1 and rising edge CLK2		20	21	22	ns
$t_{WH(C1)}$	C1 pulse width HIGH		81	82	–	ns
$t_{WH(C2)}$	C2 pulse width HIGH		81	82	–	ns
$t_{WH(C3)}$	C3 pulse width HIGH		82	85	–	ns
$t_{WL(SHP)}$	SHP pulse width LOW		21	22	–	ns
$t_{WL(SHD)}$	SHD pulse width LOW		43	44	–	ns
$t_{WL(RG)}$	RG pulse width LOW		21	22	–	ns
$t_{WH(CLK1)}$	CLK1 pulse width HIGH		81	82	–	ns
$t_{WH(CLK2)}$	CLK2 pulse width HIGH		41	43	–	ns

Note

1. Load capacity = 11 pF; $V_{DDD} = V_{DDA} = 3.3$ V; $T_{amb} = 25$ °C.

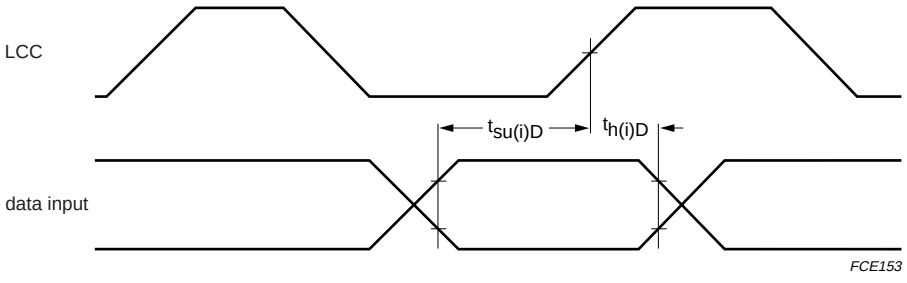


Fig.24 Data input timing.

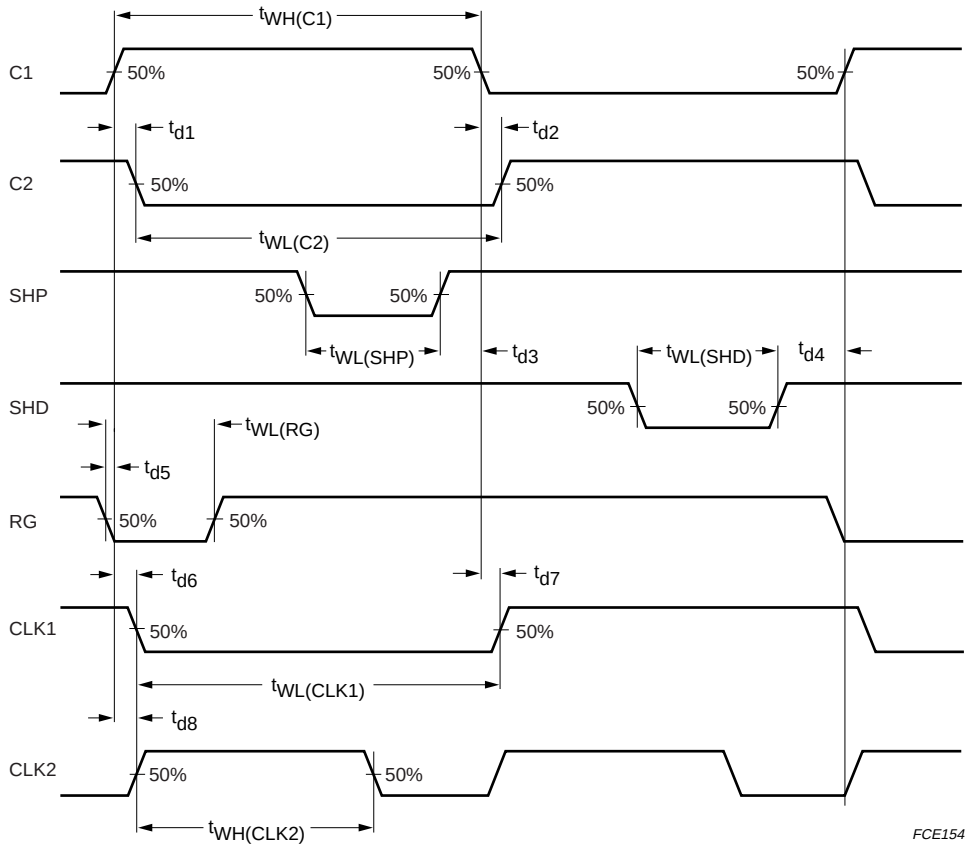


Fig.25 PPG high-speed pulses for PAL medium resolution sensors (mode 0).

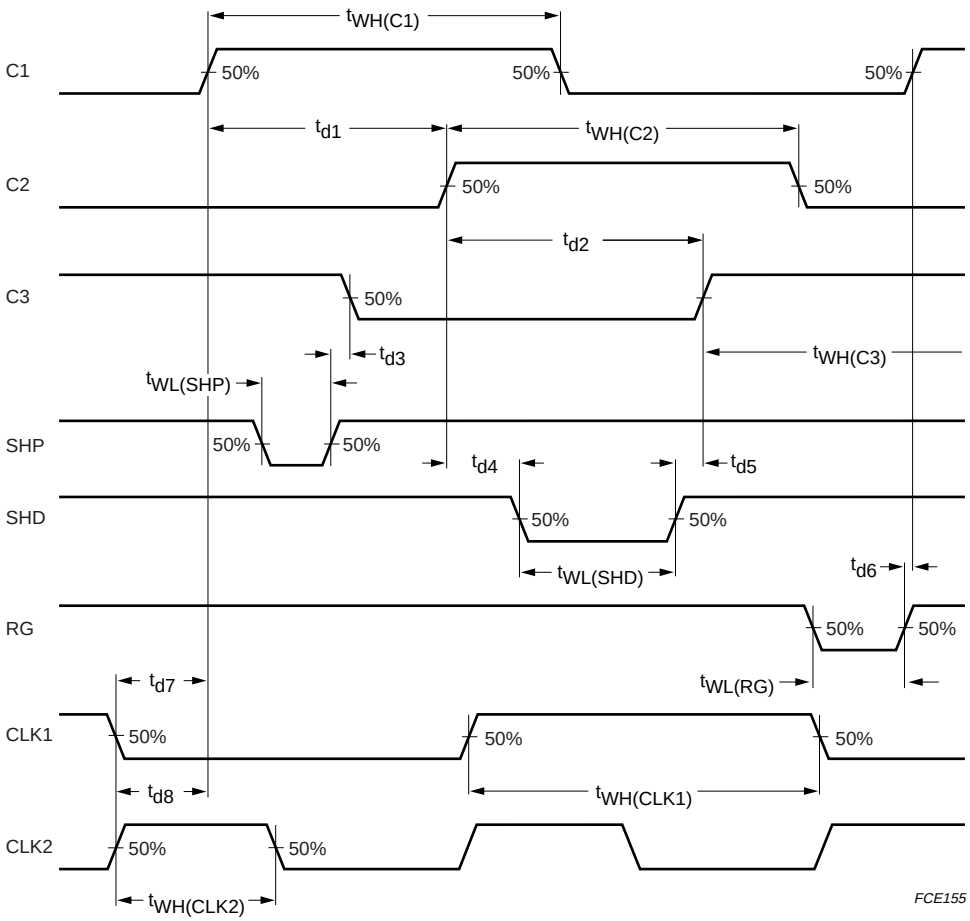


Fig.26 PPG high-speed pulses for VGA sensors (mode 2).

14 APPLICATION INFORMATION

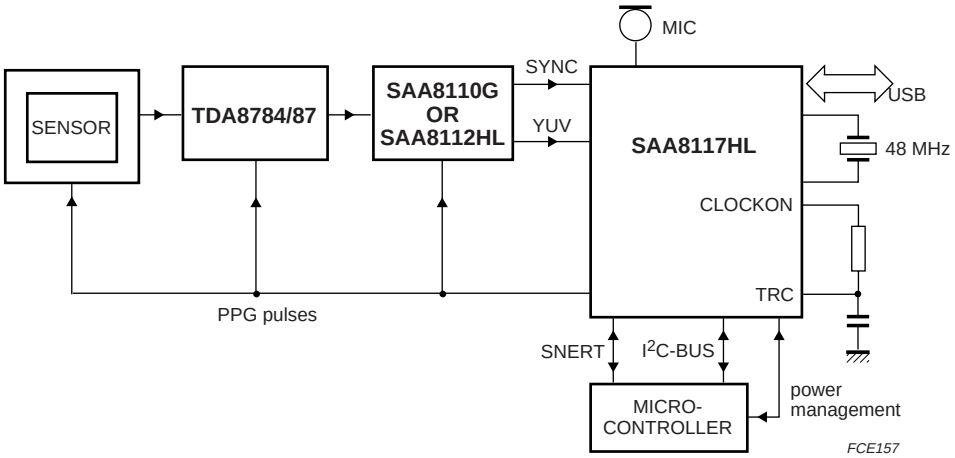
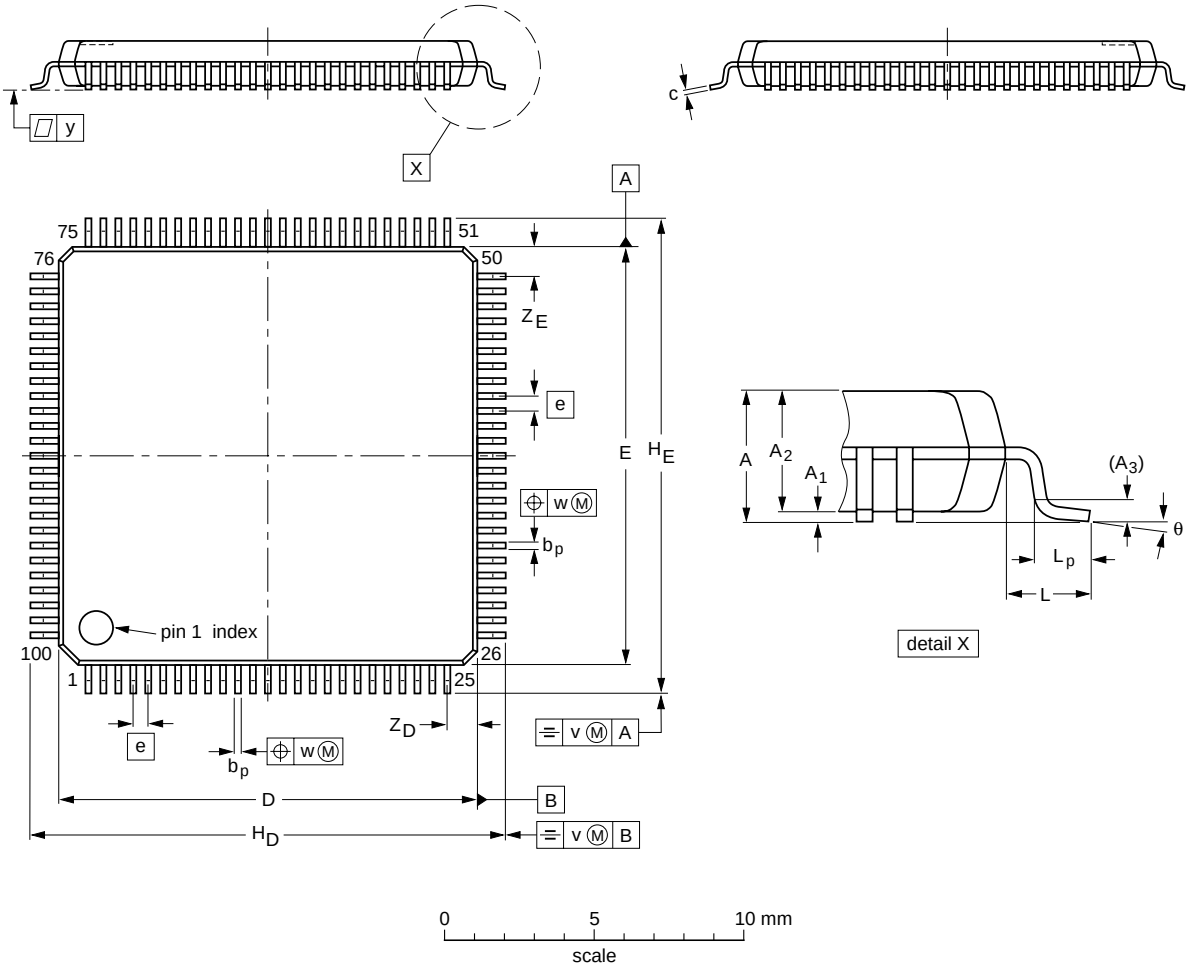


Fig.27 Application diagram.

15 PACKAGE OUTLINE

LQFP100: plastic low profile quad flat package; 100 leads; body 14 x 14 x 1.4 mm **SOT407-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.5 1.3	0.25	0.28 0.16	0.18 0.12	14.1 13.9	14.1 13.9	0.5	16.25 15.75	16.25 15.75	1.0	0.75 0.45	0.2	0.12	0.1	1.15 0.85	1.15 0.85	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT407-1						~~95-12-19~~ 97-08-04

16 SOLDERING

16.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

16.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

16.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

16.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

16.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

17 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

18 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

19 PURCHASE OF PHILIPS I²C COMPONENTS

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NOTES

NOTES

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