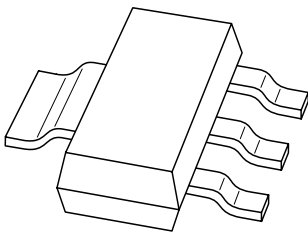


# DATA SHEET



**BDP32**

**PNP medium power transistor**

Product specification  
Supersedes data of 1997 Mar 10

1999 Apr 23

# PNP medium power transistor

# BDP32

### FEATURES

- High current (max. 3 A)
- Low voltage (max. 45 V).

### APPLICATIONS

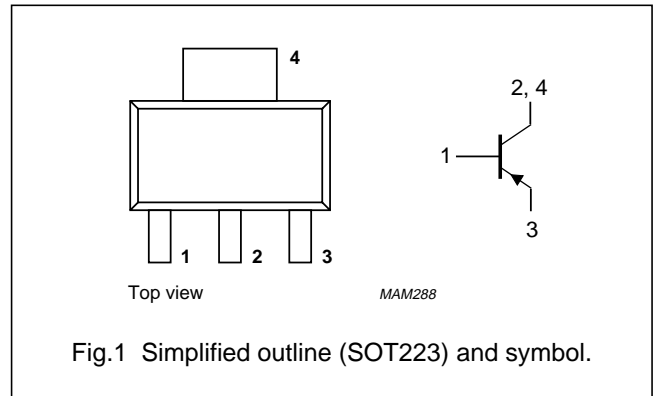
- General purpose medium power applications.

### DESCRIPTION

PNP medium power transistor in a SOT223 plastic package. NPN complement: BDP31.

### PINNING

PIN	DESCRIPTION
1	base
2,4	collector
3	emitter



### LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter	–	–45	V
$V_{CEO}$	collector-emitter voltage	open base	–	–45	V
$V_{EBO}$	emitter-base voltage	open collector	–	–5	V
$I_C$	collector current (DC)		–	–3	A
$I_{CM}$	peak collector current		–	–6	A
$I_{BM}$	peak base current		–	–0.5	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$ ; note 1	–	1.35	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	150	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

### Note

1. Device mounted on a printed-circuit board, single sided copper, tinplated, mounting pad for collector 1 cm<sup>2</sup>. For other mounting conditions, see “*Thermal considerations for the SOT223 in the General Part of associated Handbook*”.

## PNP medium power transistor

## BDP32

## THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	91	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		10	K/W

## Note

1. Device mounted on a printed-circuit board, single sided copper, tinplated, mounting pad for collector 1 cm<sup>2</sup>. For other mounting conditions, see "Thermal considerations for the SOT223 in the General Part of associated Handbook".

## CHARACTERISTICS

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

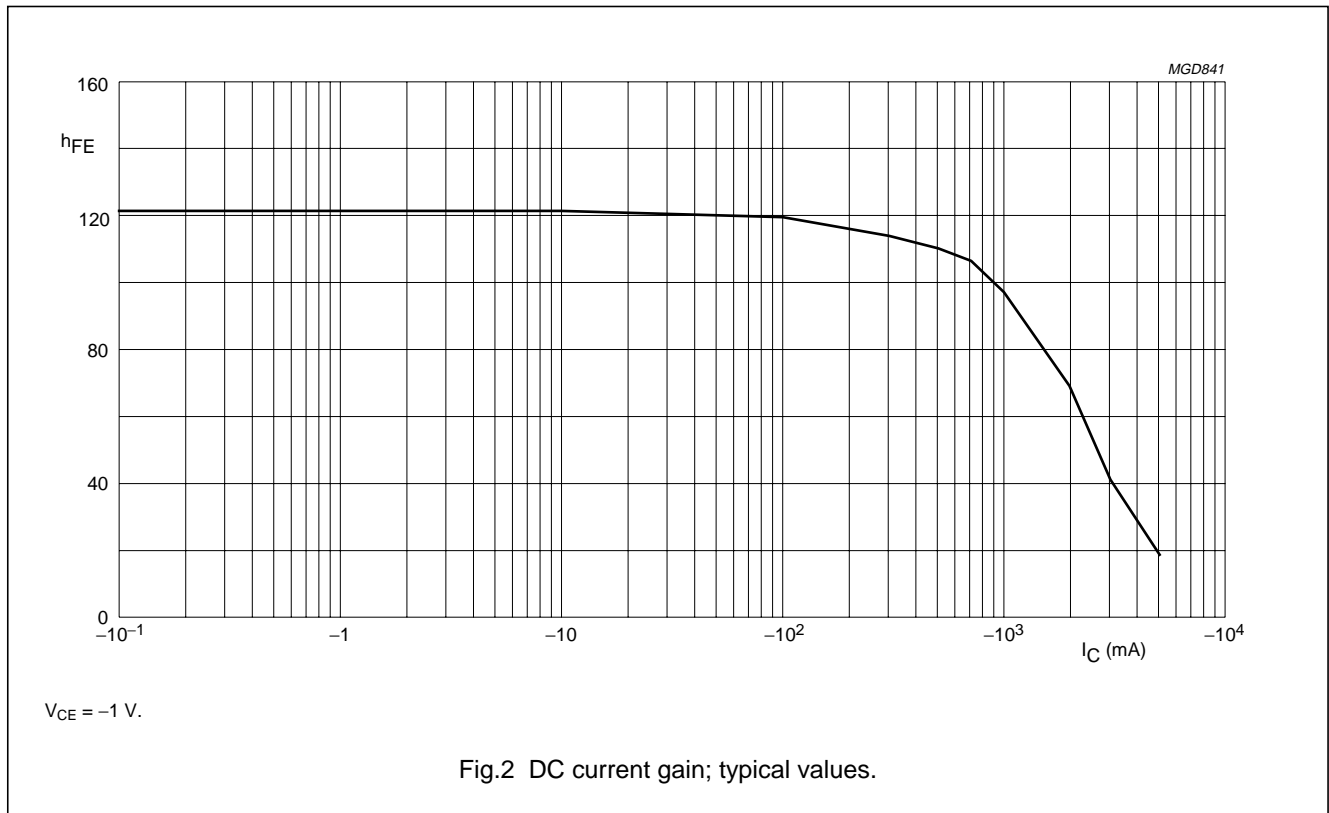
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$I_{CBO}$	collector cut-off current	$I_E = 0; V_{CB} = -40\text{ V}$	–	–50	nA
		$I_E = 0; V_{CB} = -40\text{ V}; T_j = 150\text{ °C}$	–	–10	μA
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{EB} = -5\text{ V}$	–	–50	nA
$h_{FE}$	DC current gain	$I_C = -0.5\text{ A}; V_{CE} = -12\text{ V};$ note 1; see Fig.2	40	–	
		$I_C = -2\text{ A}; V_{CE} = -1\text{ V};$ note 1; see Fig.2	20	–	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA};$ note 1	–	–300	mV
		$I_C = -2\text{ A}; I_B = -200\text{ mA};$ note 1	–	–700	mV
$V_{BEsat}$	base-emitter saturation voltage	$I_C = -500\text{ mA}; I_B = -50\text{ mA};$ note 1	–	–1.2	V
		$I_C = -2\text{ A}; I_B = -200\text{ mA};$ note 1	–	–1.5	V
$f_T$	transition frequency	$V_{CE} = -5\text{ V}; I_C = -250\text{ mA}; f = 100\text{ MHz}$	60	–	MHz

## Note

1. Pulse test:  $t_p \leq 300\text{ μs}; \delta \leq 0.02$ .

PNP medium power transistor

BDP32



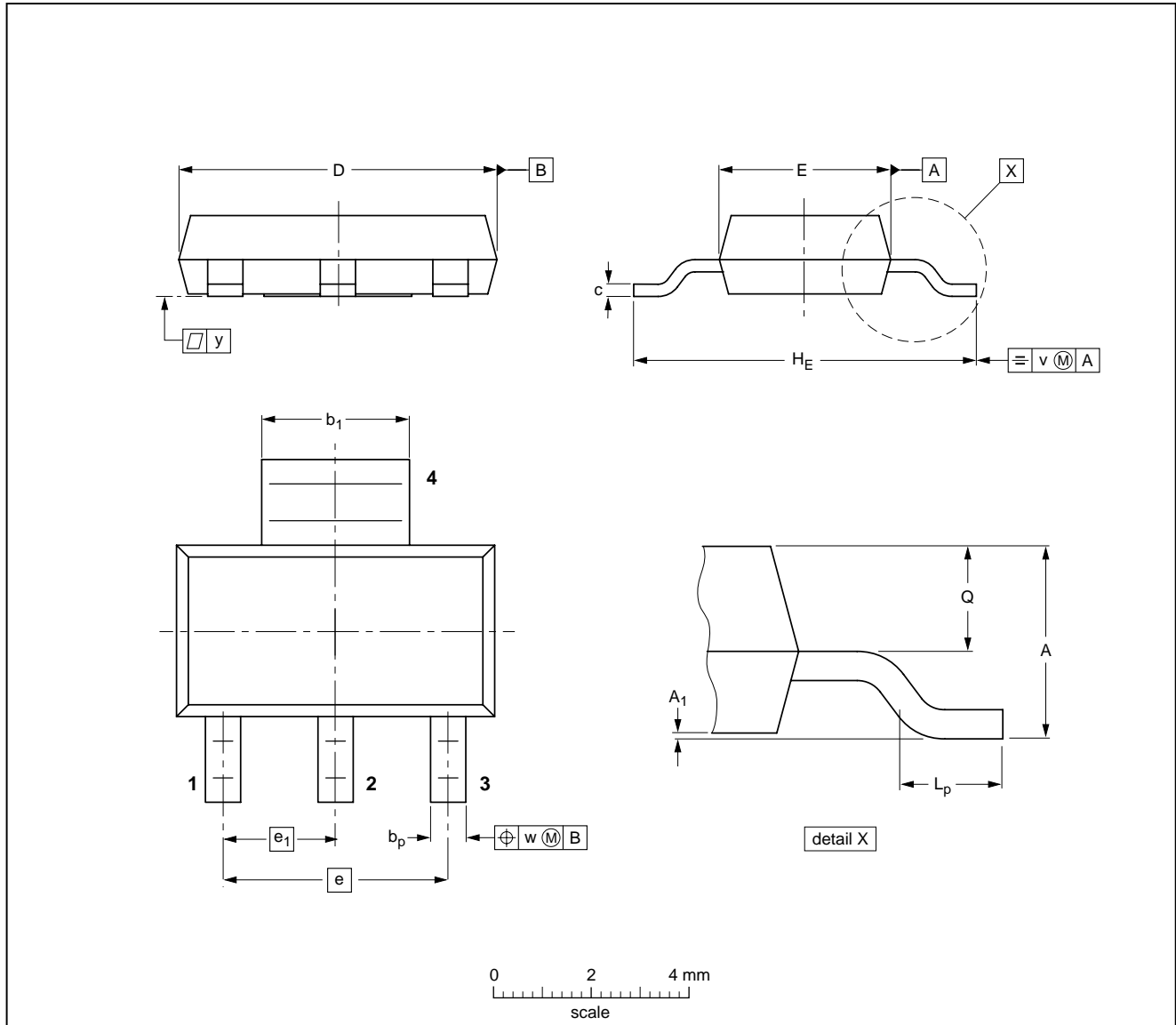
PNP medium power transistor

BDP32

PACKAGE OUTLINE

Plastic surface mounted package; collector pad for good heat transfer; 4 leads

SOT223



DIMENSIONS (mm are the original dimensions)

UNIT	A	A <sub>1</sub>	b <sub>p</sub>	b <sub>1</sub>	c	D	E	e	e <sub>1</sub>	H <sub>E</sub>	L <sub>p</sub>	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						96-11-11 97-02-28

## PNP medium power transistor

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**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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PNP medium power transistor

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