

DATA SHEET

SAA7212

Integrated MPEG AVG decoder

Preliminary specification
Supersedes data of 1998 Feb 18
File under Integrated Circuits, IC02

1998 Sep 07

Integrated MPEG AVG decoder

SAA7212

FEATURES

General features

- Single external Synchronous DRAM organized as $1\text{ M} \times 16$ interfacing at 81 MHz. Due to efficient memory use in MPEG decoding, more than 1 Mbit available for graphics
- Fast 16-bit data + 8-bit address interface with external controller on 27 MHz. Sustained data rate to external SDRAM ≤ 9 Mbytes/s in bursts of 128 bytes
- Dedicated input for audio and video in PES or ES in byte wide. Data input rate: ≤ 9 Mbytes/s in byte mode. Accompanying strobe signals distinguish between audio and video data
- Dedicated compressed data input compatible with the VLSI VES2020/2030 demultiplexers; video is received in byte format and audio serially
- Audio and/or video can also be input via the CPU interface in PES/ES in 8 or 16-bit parallel format up to a peak data rate of 9 Mbytes/s
- Single 27 MHz external clock for time base reference and internal processing. Internal system time base at 90 kHz can be synchronized via CPU port. All required decoding and presentation clocks are generated internally
- Flexible memory allocation under control of the external CPU enables optimized partitioning of memory for different tasks
- Boundary scan testing implemented
- External SDRAM self test
- Supply voltage 3.3 V
- Package QFP160.

CPU related features

- 16 bits data, 8 bits address, or 16 bits multiplexed bus. Motorola 68xxx and Intel x 86 compatible.
- Support fast DMA transfer
- Flexible bidirectional interface to external SDRAM. Minimum sustained rate is 9 Mbytes/s
- Enhanced block mover allows 3 D data move in the external SDRAM. Picture move/Graphic bit maps construction can be done with minimum CPU support.

MPEG2 system features

- Parsing of MPEG2 PES and MPEG1 packet streams
- Double system time clock counters
- Stand-alone or supervised audio/video synchronization
- Processing of errors flagged by channel decoding section
- Support for retrieval of PES header.

MPEG2 video features

- Decoding of MPEG2 video up to main level, main profile
- Output picture format: CCIR-601 4 : 2 : 2 interlaced pictures. Picture format 720×576 at 50 Hz or 720×480 at 60 Hz
- Support of constant and variable bit rates up to 15 Mbits/s
- Stand-alone or CPU controlled mode for decoding/display processes
- Stand-alone mode can be used by applications requiring still pictures manipulations
- Output interface at 8-bit wide, 27 MHz UYVY multiplexed bus
- Horizontal and vertical pan and scan allows the extraction of a window from the coded picture
- Flexible horizontal scaling from 0.5 up to 4 allows easy aspect ratio conversion including support for 2.21 : 1 aspect ratio movies. In case of shrinking an anti-aliasing pre-filter is applied
- Vertical scaling with fixed factors 0.5, 1 or 2. Factor 0.5, realizing picture shrink. Factor 2 can be used for up-conversion of pictures with 288 (240) lines or less.
- Vertical down-scaling with 0.75 factor, realizing letter box conversion
- Horizontal and vertical scaling can be combined to scale pictures to $\frac{1}{4}$ their original size, thus freeing up screen space for graphic applications like electronic program guides
- Non full screen MPEG pictures will be displayed in a box of which position and background colour are adjustable by the external microcontroller
- Nominal video input buffer size for ml@mp 2.7 Mbit
- Video output may be slaved to internally (master) generated or externally (slave) supplied HV synchronization signals. The position of active video is programmable. Display phase is not affected by MPEG timebase changes.

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- Video output direct connectable to SAA718x encoder family
- Various trick modes under control of external microcontroller in stand-alone mode:
 - Freeze field/frame on I or P pictures; restart on I picture
 - Freeze field on B pictures; restart on the next I or P picture.
 - Scanning and decoding of I or I + P pictures in a IBP sequence
 - Single step mode
 - Repeat/skip field for time base correction.

MPEG2 audio features

- Decoding of 2 channels, layer I and II MPEG audio. Support for mono, stereo, intensity stereo and dual channel mode.
- Constant and variable bit rates up to 448 kbit/s
- Supported audio sampling frequencies: 48, 44.1, 32, 24, 22.05 and 16 kHz
- CRC error detection
- 3 decoding modes for dual channel streams: decoding of CH1 only, decoding of CH2 only and decoding of both CH1 and CH2
- Storage of last 54 bytes in ancillary data field
- Dynamic Range Control (DRC) at output
- Independent channel volume control and programmable inter channel crosstalk through a baseband audio processing unit
- Muting possibility via external controller. Automatic muting in case of errors or data lack.
- Generation of 'beeps' with programmable tone height, duration and amplitude
- Serial two channel digital audio output with 16, 18, 20 or 22 bits per sample, compatible either to I²S or Japanese formats. Output can be set to high-impedance mode via the external controller.
- Serial SPDIF audio output. Output can be set to high-impedance mode.
- Clock output 256 or 384 × f_s for external DA converter. Output can be set to high-impedance mode.
- Audio FIFO in external SDRAM. Programmable buffer size, at least 64 kbit is available.
- Synchronization modes: PTS controlled, PTS free running, software controlled, buffer controlled
- PTS register can be set via external controller
- Programmable processing delay compensation
- Software controlled stop and restart functions.

Graphics features

- Graphics are presented in boxes independent of video format
- Screen arrangement of boxes is determined by display list mechanism which allows for multiple boxes, background loading, fast switching, scrolling and fading of regions
- Support of 2, 4, 8-bit/pixel in fixed bit maps format or coded in accordance to the DVB variable/run length standard for region based graphics
- Display colours are obtained via colour look up tables. CLUT output is YUVT at 8-bit for each signal component thus enabling 16 M different colours and 6-bit for T which gives 64 mixing levels with video, (T = transparency).
- Bit-map table mechanism to specify a sub set of entries if the CLUT is larger than required by the coded bit pattern. Supported bit-map tables are 16 to 256, 4 to 256 and 4 to 16.
- Graphics boxes may not overlap vertically. If 256 entry CLUT has to be down loaded, a vertical separation of 1 line is mandatory.
- Optimized memory utilization in MPEG video decoding allows for a storage capacity of 1.2 Mbit for graphics bit maps. Flexibility in memory control enables larger capacity in a lot of applications. Moreover variable length/run length encoding makes better use of available memory capacity for graphics bit maps thus making full screen graphics at 8-bit/pixel feasible.
- Fast CPU access (9 Mbytes/s) enables full 1.2 Mbit bit map update within 20 ms
- Internal support for fast block moves in external SDRAM
- Graphics mechanism can be used for signal generation in the vertical blanking interval. Useful for teletext, wide screen signalling, closed caption, etc.
- Support for a single down loadable cursor of 1k pixel with programmable shape. Supported shapes are 8 × 128 pixels, 16 × 64 pixels, 32 × 32 pixels, 64 × 16 pixels and 128 × 8 pixels.
- Cursor colours obtained via 4 entry CLUT with YUVT at 6,4,4 respectively 2 bits. Mixing of cursor with video + graphics in 4 levels.
- Cursor can be moved freely across the screen without overlapping restrictions.

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APPLICATIONS

- Tbf.

GENERAL DESCRIPTION

The SAA7212 is an MPEG2 source decoder which combines audio decoding and video decoding. Additionally to these basic MPEG functions it also provides means for enhanced graphics and/or on-screen display (OSD). Due to an optimized architecture for audio and video decoding, maximum capacity in external memory and processing power from the external CPU is available for graphics support.

QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---------------|--|---------|------|---------|------|
| V_{DD} | functional supply voltage | 3.0 | 3.3 | 3.6 | V |
| $I_{DD(tot)}$ | total supply current; $V_{DD} = 3.3$ V | – | tbf | – | mA |
| f_{clk} | device clock frequency | –30 ppm | 27.0 | +30 ppm | MHz |

ORDERING INFORMATION

| TYPE NUMBER | PACKAGE | | |
|-------------|---------|--|----------|
| | NAME | DESCRIPTION | VERSION |
| SAA7212H | QFP160 | plastic quad flat package; 160 leads (lead length 1.95 mm); body $28 \times 28 \times 3.4$ mm; high stand-off height | SOT322-1 |

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BLOCK DIAGRAM

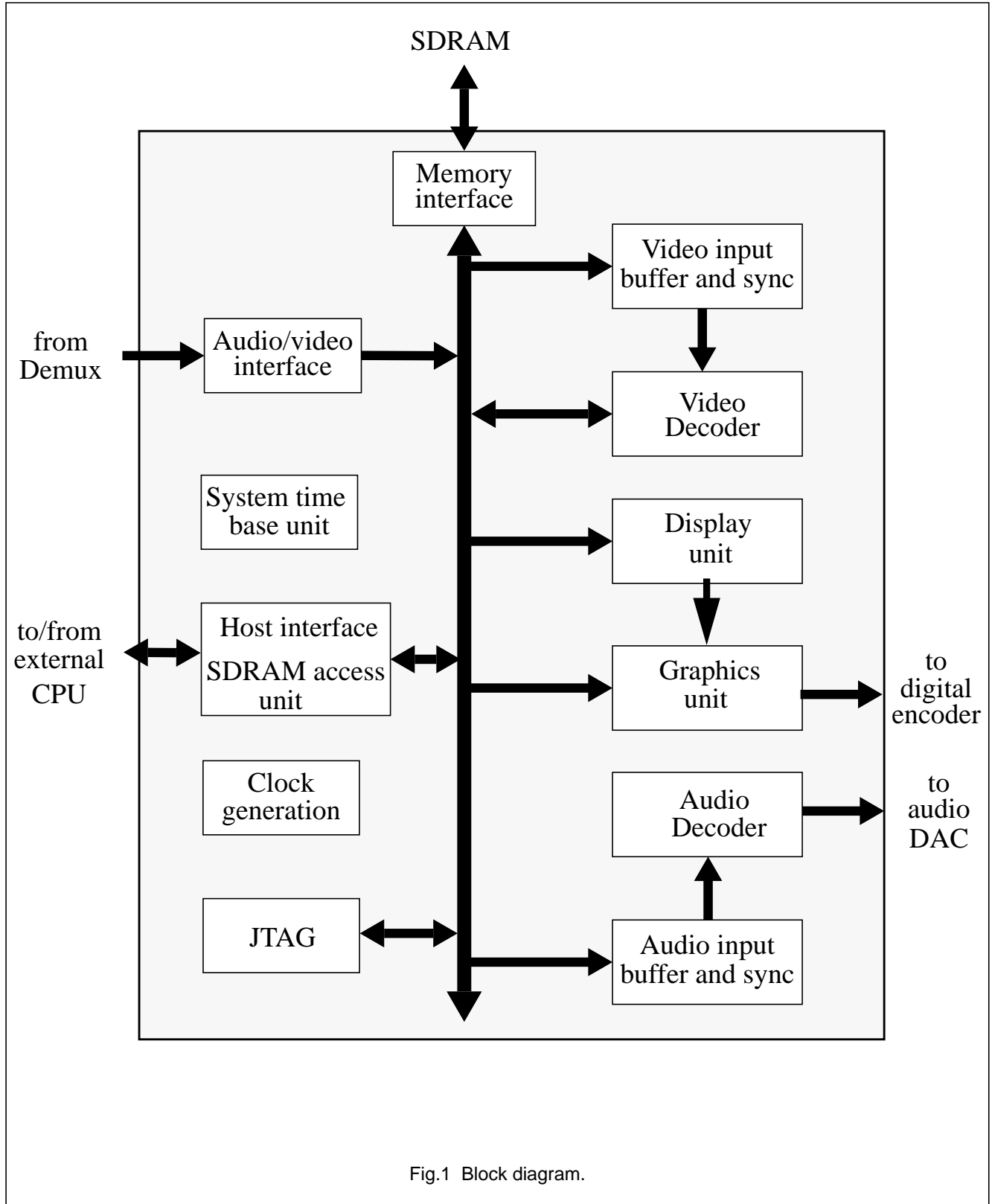


Fig.1 Block diagram.

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PINNING

| SYMBOL | PIN | DESCRIPTION |
|-------------------|-----|----------------------------------|
| MUX | 1 | multiplexed/non multiplexed bus |
| CPU_TYPE | 2 | Intel/Motorola selection |
| DMA_ACK | 3 | DMA acknowledge |
| DMA_REQ | 4 | DMA request |
| DMA_DONE | 5 | DMA end |
| DMA_RDY | 6 | DMA ready |
| V _{SS} | 7 | ground for pad ring |
| CS | 8 | chip select. |
| DS | 9 | data strobe |
| AS | 10 | address strobe |
| RWN | 11 | read/write |
| DTACK | 12 | data acknowledge |
| V _{DD} | 13 | 3.3 V supply for pad ring |
| IRQ 0 | 14 | individually maskable interrupts |
| IRQ 1 | 15 | individually maskable interrupts |
| V_REQ | 16 | compressed video data request |
| A_REQ | 17 | compressed audio data request |
| V _{SS} | 18 | ground for pad ring |
| V _{SSCO} | 19 | ground for core logic |
| V _{DCCO} | 20 | 3.3 V supply for core logic |
| DATA 0 | 21 | CPU data interface |
| DATA 1 | 22 | CPU data interface |
| DATA 2 | 23 | CPU data interface |
| DATA 3 | 24 | CPU data interface |
| V _{DD} | 25 | 3.3 V supply for pad ring |
| DATA 4 | 26 | CPU data interface |
| DATA 5 | 27 | CPU data interface |
| DATA 6 | 28 | CPU data interface |
| DATA 7 | 29 | CPU data interface |
| V _{SS} | 30 | ground for pad ring |
| DATA 8 | 31 | CPU data interface |
| DATA 9 | 32 | CPU data interface |
| DATA 10 | 33 | CPU data interface |
| DATA 11 | 34 | CPU data interface |
| V _{DD} | 35 | 3.3 V supply for pad ring |
| DATA 12 | 36 | CPU data interface |
| DATA 13 | 37 | CPU data interface |
| DATA 14 | 38 | CPU data interface |
| DATA 15 | 39 | CPU data interface |
| V _{SS} | 40 | ground for pad ring |

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| SYMBOL | PIN | DESCRIPTION |
|-------------------|-----|-----------------------------|
| ADDRESS 1 | 41 | CPU address interface |
| ADDRESS 2 | 42 | CPU address interface |
| ADDRESS 3 | 43 | CPU address interface |
| ADDRESS 4 | 44 | CPU address interface |
| V _{DD} | 45 | 3.3 V supply for pad ring |
| ADDRESS 5 | 46 | CPU address interface |
| ADDRESS 6 | 47 | CPU address interface |
| ADDRESS 7 | 48 | CPU address interface |
| ADDRESS 8 | 49 | CPU address interface |
| V _{SS} | 50 | ground for pad ring |
| V _{SSCO} | 51 | ground for core logic |
| V _{DDCO} | 52 | 3.3 V supply for core logic |
| SDRAM_DATA 0 | 53 | SDRAM data |
| SDRAM_DATA 15 | 54 | SDRAM data |
| SDRAM_DATA 1 | 55 | SDRAM data |
| V _{DD} | 56 | 3.3 V supply for pad ring |
| SDRAM_DATA 14 | 57 | SDRAM data |
| SDRAM_DATA 2 | 58 | SDRAM data |
| SDRAM_DATA 13 | 59 | SDRAM data |
| V _{SS} | 60 | ground for pad ring |
| SDRAM_DATA 3 | 61 | SDRAM data |
| SDRAM_DATA 12 | 62 | SDRAM data |
| SDRAM_DATA 4 | 63 | SDRAM data |
| V _{DD} | 64 | 3.3 V supply for pad ring |
| SDRAM_DATA 11 | 65 | SDRAM data |
| SDRAM_DATA 5 | 66 | SDRAM data |
| SDRAM_DATA 10 | 67 | SDRAM data |
| V _{SS} | 68 | ground for pad ring |
| SDRAM_DATA 6 | 69 | SDRAM data |
| SDRAM_DATA 9 | 70 | SDRAM data |
| SDRAM_DATA 7 | 71 | SDRAM data |
| V _{DD} | 72 | 3.3 V supply for pad ring |
| SDRAM_DATA 8 | 73 | SDRAM data |
| SDRAM_WE | 74 | SDRAM write enable |
| SDRAM_CAS | 75 | SDRAM column address strobe |
| V _{SS} | 76 | ground for pad ring |
| SDRAM_RAS | 77 | SDRAM row address strobe |
| SDRAM_UDQ | 78 | SDRAM write mask |
| V _{DD} | 79 | 3.3 V supply for pad ring |
| READ_IN | 80 | read command in |
| READ_OUT | 81 | read command out |

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| SYMBOL | PIN | DESCRIPTION |
|-------------------|-----|------------------------------------|
| V _{SS} | 82 | ground for pad ring |
| CP81MEXT | 83 | 81 MHz SDRAM clock return path |
| CP81M | 84 | 81 MHz SDRAM memory clock |
| V _{DD} | 85 | 3.3 V supply for pad ring |
| SDRAM_ADDR 8 | 86 | SDRAM address |
| SDRAM_ADDR 9 | 87 | SDRAM address |
| SDRAM_ADDR 11 | 88 | SDRAM address |
| V _{SS} | 89 | ground for pad ring |
| SDRAM_ADDR 7 | 90 | SDRAM address |
| SDRAM_ADDR 10 | 91 | SDRAM address |
| SDRAM_ADDR 6 | 92 | SDRAM address |
| V _{DD} | 93 | 3.3 V supply for pad ring |
| SDRAM_ADDR 0 | 94 | SDRAM address |
| SDRAM_ADDR 5 | 95 | SDRAM address |
| SDRAM_ADDR 1 | 96 | SDRAM address |
| V _{SS} | 97 | ground for pad ring |
| SDRAM_ADDR 4 | 98 | SDRAM address |
| SDRAM_ADDR 2 | 99 | SDRAM address |
| SDRAM_ADDR 3 | 100 | SDRAM address |
| V _{SSCO} | 101 | ground for core logic |
| V _{DDCO} | 102 | 3.3 V supply for core logic |
| V _{DD} | 103 | 3.3 V supply for pad ring |
| Test 5 | 104 | IC test interface (see note 2) |
| Test 6 | 105 | IC test interface (see note 2) |
| HS | 106 | horizontal synchronization |
| VS | 107 | vertical synchronization |
| V _{SS} | 108 | ground for pad ring |
| YUV 0 | 109 | YUV video output at 27 MHz |
| YUV 1 | 110 | YUV video output at 27 MHz |
| YUV 2 | 111 | YUV video output at 27 MHz |
| YUV 3 | 112 | YUV video output at 27 MHz |
| V _{DD} | 113 | 3.3 V supply for pad ring |
| YUV 4 | 114 | YUV video output at 27 MHz |
| YUV 5 | 115 | YUV video output at 27 MHz |
| YUV 6 | 116 | YUV video output at 27 MHz |
| YUV 7 | 117 | YUV video output at 27 MHz |
| Test 4 | 118 | IC test interface (see note 3) |
| GRPH | 119 | indicator for graphics information |
| Test 3 | 120 | IC test interface (see note 4) |
| V _{DDAN} | 121 | 3.3 V supply for analog blocks |
| V _{SSAN} | 122 | ground for analog blocks |

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| SYMBOL | PIN | DESCRIPTION |
|-------------------|-----|--|
| V _{SS} | 123 | ground for pad ring |
| CLK | 124 | 27 MHz Clock input |
| V _{SS} | 125 | ground for pad ring |
| TCK | 126 | boundary scan test clock |
| TRST | 127 | boundary scan test reset |
| TMS | 128 | boundary scan test mode select |
| TDO | 129 | boundary scan test data output |
| TDI | 130 | boundary scan test data input |
| V _{DD} | 131 | 3.3 V supply for pad ring |
| Test 0 | 132 | IC test interface (see note 4) |
| Test 1 | 133 | IC test interface (see note 4) |
| Test 2 | 134 | IC test interface (see note 4) |
| AUDDEN | 135 | synchronization of the serial audio input (A_DATA) |
| A_DATA | 136 | serial audio input |
| V _{DD} | 137 | 3.3 V supply for pad ring |
| RESET | 138 | hard reset input, active LOW |
| FSCLK | 139 | 256 or 384f _s (audio sampling) |
| V _{DDCO} | 140 | 3.3 V supply for core logic |
| V _{SSCO} | 141 | ground for core logic |
| SCK | 142 | serial audio clock |
| SD | 143 | serial audio data output |
| V _{SS} | 144 | ground for pad ring |
| WS | 145 | word select |
| SPDIF | 146 | digital audio output |
| ERROR | 147 | flag for bitstream error. |
| V_STROBE | 148 | video strobe |
| V _{DD} | 149 | 3.3 V supply for pad ring |
| AV_DATA 0 | 150 | MPEG stream input port |
| AV_DATA 1 | 151 | MPEG stream input port |
| AV_DATA 2 | 152 | MPEG stream input port |
| AV_DATA 3 | 153 | MPEG stream input port |
| V _{SS} | 154 | ground for pad ring |
| AV_DATA 4 | 155 | MPEG stream input port |
| AV_DATA 5 | 156 | MPEG stream input port |
| AV_DATA 6 | 157 | MPEG stream input port |
| AV_DATA 7 | 158 | MPEG stream input port |
| A_STROBE | 159 | audio strobe |
| V _{DD} | 160 | 3.3 V supply for pad ring |

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Notes

1. 5 V tolerant outputs swing between V_{SS} and V_{DD} but 5 V tolerant input can receive signal swinging between V_{SS} and 3.3 V or V_{SS} and 5 V.
2. Should be left open in normal mode.
3. Should be tied up to V_{DD} in normal mode.
4. Should be tied down to ground in normal mode.

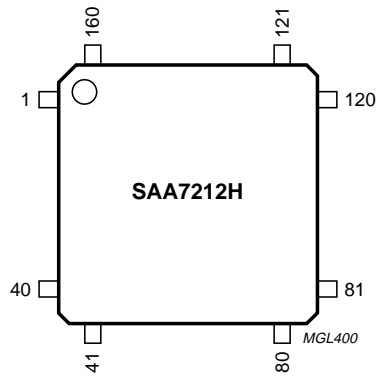


Fig.2 Pin configuration.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|--------------|-------------------------------|--|------|------|------|--------------------|
| V_{DD} | supply voltage | | -0.5 | +5 | tbf | V |
| $V_{n(max)}$ | voltage on all pins | | 0 | 5 | tbf | V |
| P_{tot} | total power dissipation | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | - | 1 | tbf | W |
| T_{stg} | IC storage temperature | | -55 | 150 | tbf | $^{\circ}\text{C}$ |
| T_{amb} | operating ambient temperature | | 0 | 70 | tbf | $^{\circ}\text{C}$ |

THERMAL CHARACTERISTICS

| SYMBOL | PARAMETER | VALUE | UNIT |
|---------------|---|-------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient in free air | 30 | K/W |

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

CHARACTERISTICS

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|------------------------------|---|----------------|--------|--------------|---------------|
| Supply | | | | | |
| V_{DD} | functional supply voltage | 3.0 | 3.3 | 3.6 | V |
| $I_{DD(tot)}$ | total supply current; $V_{DD} = 3.3\text{ V}$ | - | tbf | - | mA |
| Inputs | | | | | |
| $V_{IH(5V\text{ tolerant})}$ | input voltage HIGH | 2.0 | - | 6.5 | V |
| V_{IH} | input voltage HIGH | $0.7V_{DD}$ | - | $V_{DD}+2.0$ | V |
| $V_{IL(5V\text{ tolerant})}$ | input voltage LOW | -0.5 | - | 0.8 | V |
| V_{IL} | input voltage LOW | -0.5 | - | $0.3V_{DD}$ | V |
| I_L | leakage current | - | - | 20 | μA |
| C_i | input capacitance | 0 | - | 10 | pF |
| Outputs | | | | | |
| $V_{OH(5V\text{ tolerant})}$ | output voltage HIGH | 2.4 | - | - | V |
| V_{OH} | output voltage HIGH | $V_{DD} - 0.4$ | - | - | V |
| $V_{OL(5V\text{ tolerant})}$ | output voltage LOW | - | - | 0.4 | V |
| V_{OL} | output voltage LOW | - | - | 0.4 | V |
| DC timing | | | | | |
| T_{cy} | cycle time | - | 37.037 | - | ns |
| δ | duty factor | 40 | - | 60 | % |

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APPLICATION INFORMATION

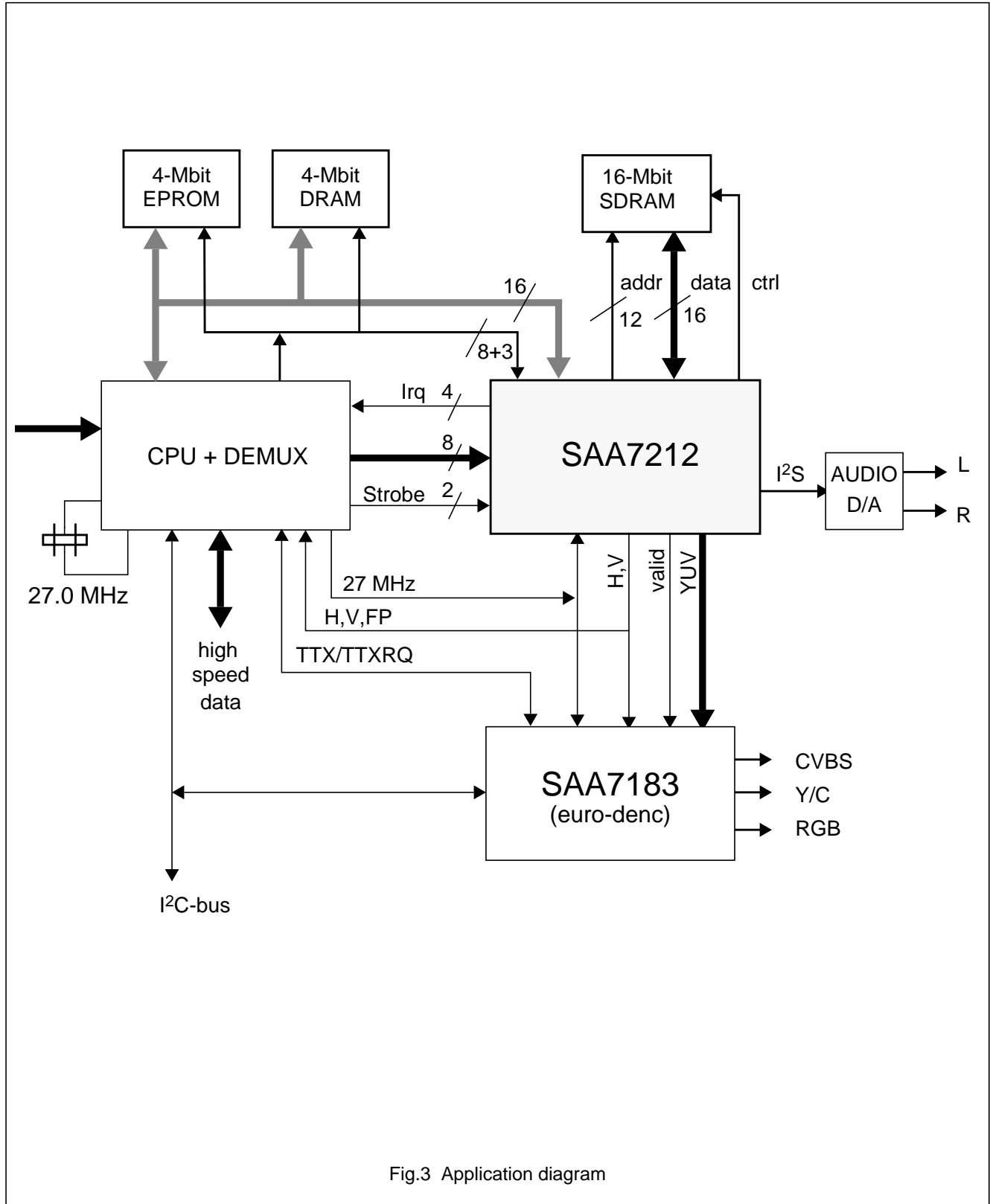
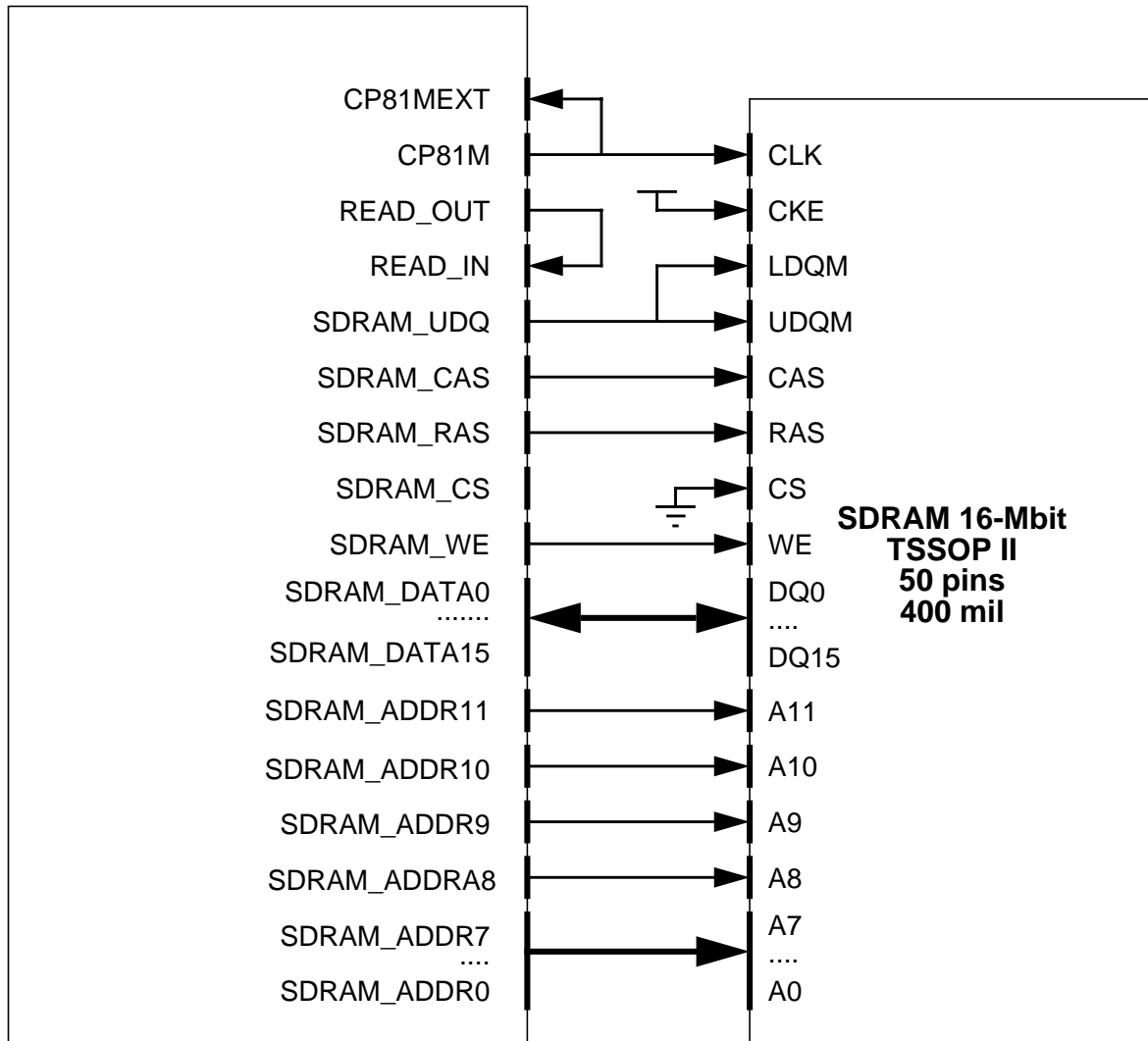


Fig.3 Application diagram

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The board should be designed to insure a similar load on the CP81M and READ_OUT pins as well as a similar fly time between the CP81M and CP81MEXT pins on one side and the READ_OUT and READ_IN pins on the other side.

Fig.4 Connection SAA7212 SDRAM.

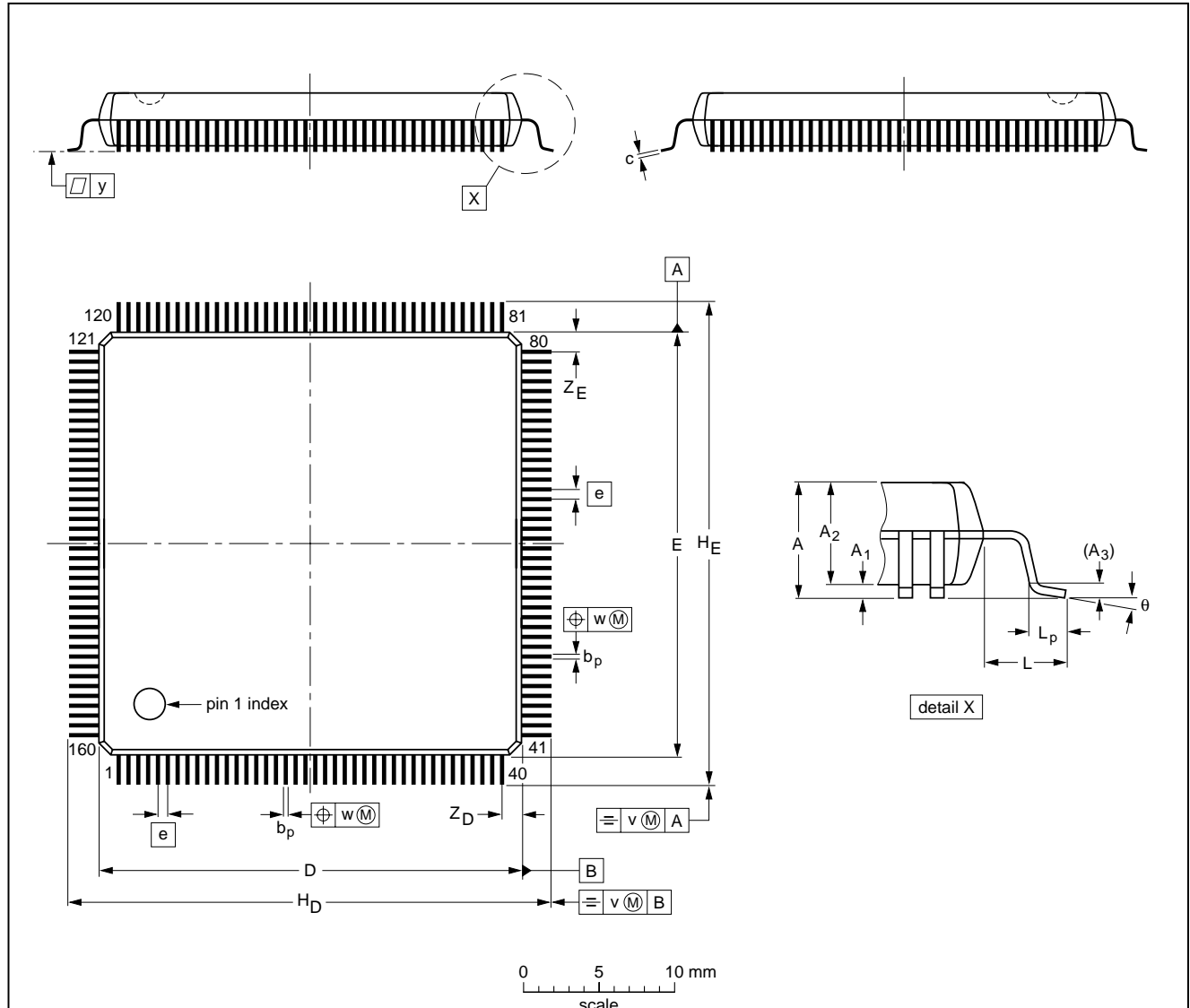
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PACKAGE OUTLINE

QFP160: plastic quad flat package;
160 leads (lead length 1.95 mm); body 28 x 28 x 3.4 mm; high stand-off height

SOT322-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A1 | A2 | A3 | bp | c | D ⁽¹⁾ | E ⁽¹⁾ | e | HD | HE | L | Lp | v | w | y | ZD ⁽¹⁾ | ZE ⁽¹⁾ | θ |
|------|--------|--------------|--------------|------|--------------|--------------|------------------|------------------|------|--------------|--------------|------|------------|-----|------|-----|-------------------|-------------------|----------|
| mm | 3.95 | 0.40 0.25 | 3.70 3.15 | 0.25 | 0.40 0.25 | 0.23 0.13 | 28.1 27.9 | 28.1 27.9 | 0.65 | 32.2 31.6 | 32.2 31.6 | 1.95 | 1.1 0.7 | 0.3 | 0.15 | 0.1 | 1.5 1.1 | 1.5 1.1 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT322-1 | | MO112DD1 | | | | 95-02-04 97-08-04 |

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION

Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

| | |
|---|---|
| Data sheet status | |
| Objective specification | This data sheet contains target or goal specifications for product development. |
| Preliminary specification | This data sheet contains preliminary data; supplementary data may be published later. |
| Product specification | This data sheet contains final product specifications. |
| Limiting values | |
| Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability. | |
| Application information | |
| Where application information is given, it is advisory and does not form part of the specification. | |

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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NOTES

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NOTES

Philips Semiconductors – a worldwide company

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Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

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Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381

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