DATA SHEET

TDA8576T
Class-H high-output voltage level line driver

Product specification
Supersedes data of 1997 Feb 26
File under Integrated Circuits, IC01

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Philips
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FEATURES

- Output voltage swing larger than supply voltage
- High supply voltage ripple rejection
- Low distortion
- Low noise
- ESD protected on all pins.

GENERAL DESCRIPTION

The TDA8576T is a two channel class-H high-output voltage line driver for use in car audio applications.
The line driver operates as a non-inverting amplifier with a gain of 6 dB and a single-ended output. Due to the class-H voltage lifting principle the voltage swing over the load is more than the supply voltage.

With a supply voltage of 9 V the output voltage swing over the load will be more than 14 V (peak-to-peak).
The TDA8576T is available in a SO16 package.

Line drivers are necessary in car audio systems in which the power amplifiers are driven by long cables.
The signal-to-noise ratio of these car audio systems is improved by using the TDA8576T class-H high-output level line driver. The high-output level of TDA8576T enables a reduction of the gain of the power amplifier resulting in an improvement of the power amplifier performance.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage		6	9	12	V
I_{CC}	supply current	V_{CC} = 9 V	–	14	20	mA
G_v	voltage gain		5	6	7	dB
$V_{o(rms)}$	maximum output voltage (RMS value)	THD = 0.1%	5.0	5.3	–	V
SVRR	supply voltage ripple rejection		40	65	–	dB
THD	total harmonic distortion	$V_{o(rms)}$ = 3 V; f = 1 kHz	–	0.005	–	%
V_{no}	noise output voltage		–	5	–	μV
$\|Z_o\|$	output impedance		–	–	10	Ω

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8576T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

BLOCK DIAGRAM

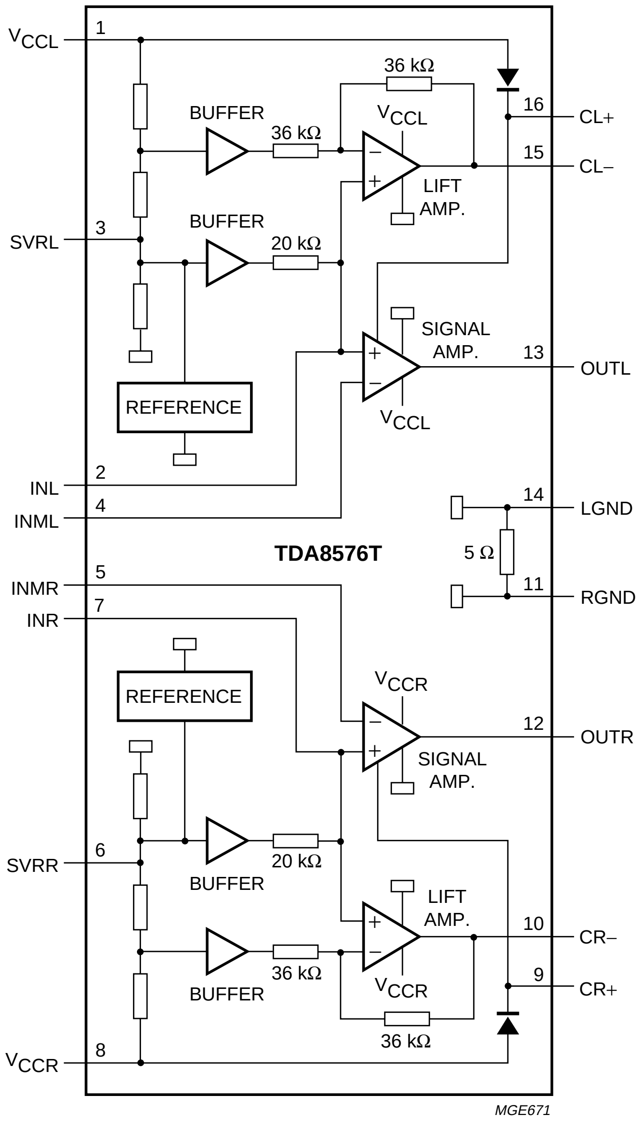


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
V_{CCL}	1	supply voltage left channel
INL	2	input voltage left channel
SVRL	3	SVRR left channel
INML	4	inverting input left channel
INMR	5	inverting input right channel
SVRR	6	SVRR right channel
INR	7	input voltage right channel
V_{CCR}	8	supply voltage right channel
CR+	9	lift capacitor (+) right channel
CR–	10	lift capacitor (–) right channel
RGND	11	ground right channel
OUTR	12	output voltage right channel
OUTL	13	output voltage left channel
LGND	14	ground left channel
CL–	15	lift capacitor (–) left channel
CL+	16	lift capacitor (+) left channel

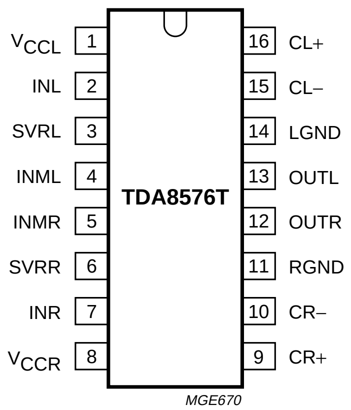


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Lift amplifier

The lift amplifier, referred to as LIFT AMP. in Fig.1, is used as a non-inverting amplifier with a voltage gain of 6 dB set by an internal feedback network. If the output voltage of the signal amplifier is low, the external lift capacitor is recharged by the lift amplifier. As soon as the output voltage of the signal amplifier increases above $0.87 \times V_{CC}$ the lift amplifier switches the voltage of the lift capacitor in series with the supply voltage $V_{CC.}$ The voltage at the positive side of the lift capacitor is referred to as lifted supply voltage.

Signal amplifier

The signal amplifier, referred to as SIGNAL AMP. in Fig.1, is used as a non-inverting amplifier. The voltage gain G_v is set by the feedback resistors according to the formula:

$$G_v = 1 + \frac{R_2}{R_1}$$

and should be set to 6 dB. The LIFT AMP. and SIGNAL AMP. must have equal voltage gain G_v.

The rail-to-rail output stage of the signal amplifier uses the lifted supply voltage to increase the output voltage swing. The DC output level is set to $\approx 0.87 \times V_{CC}$. The maximum peak-to-peak output voltage of the signal amplifier is calculated with the formula:

$$V_{o(p-p)(max)} \approx 2 \times (0.87V_{CC} - 0.4)$$

Buffers

The buffers prevent loading of the internal voltage divider network made by a series connection of resistors. For a good supply voltage ripple rejection this internal voltage divider network has to be decoupled by an external capacitor.

Reference

This circuit supplies all currents needed in the device.

LIMITING VALUES

In accordance with the Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage	operating	–	12	V
I_{ORM}	repetitive peak output current		–	20	mA
T_{amb}	ambient temperature		–40	+85	°C
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	+150	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	110	K/W

DC CHARACTERISTICS

V_{CC} = 9 V; R_L = 10 kΩ; T_{amb} = 25 °C; in accordance with application diagram (see Fig.3).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	supply voltage	V_i = 0 V	6	9	12	V
I_{CC}	supply current		–	14	20	mA
V_O	DC output voltage	note 1	–	7.8	–	V

Note

1. The DC output voltage with respect to ground is ≈0.87 × V_{CC}.

AC CHARACTERISTICS

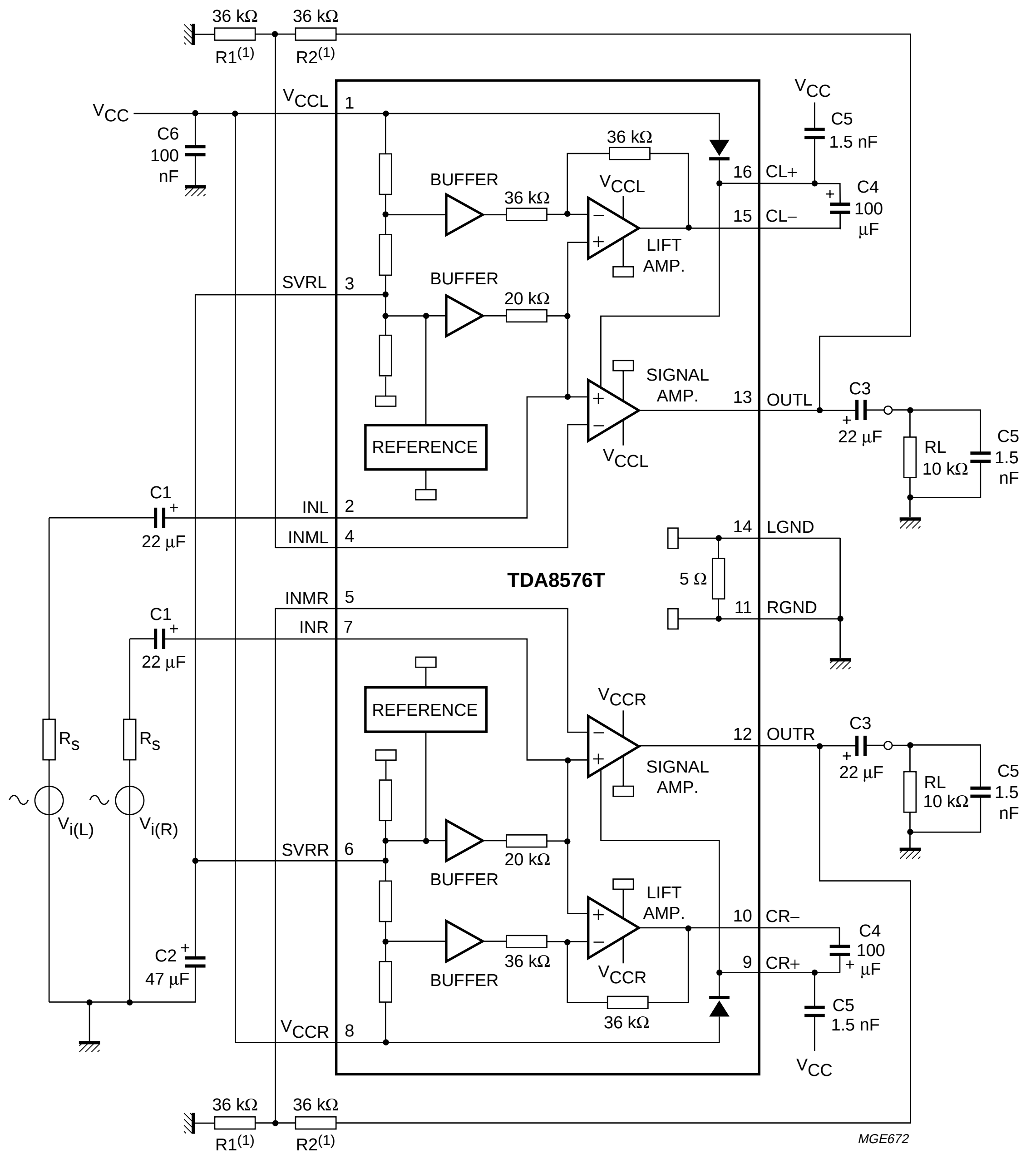
V_{CC} = 9 V; R_L = 10 kΩ; f = 1 kHz; T_{amb} = 25 °C; in accordance with application diagram (see Fig.3); note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
G_v	voltage gain		5	6	7	dB
$\lvert\Delta G_v\rvert$	channel unbalance		–	–	0.5	dB
α_{cs}	channel separation	R_s = 600 Ω; $V_{o(rms)}$ = 1 V; note 1	80	90	–	dB
f_{lr}	low frequency roll-off	–1 dB; note 2	–	–	5	Hz
f_{hr}	high frequency roll-off	–1 dB	20	–	–	kHz
$\lvert Z_i\rvert$	input impedance		14	20	28	kΩ
$\lvert Z_o\rvert$	output impedance		–	–	10	Ω
$V_{o(max)(rms)}$	maximum output voltage (RMS value)	THD + N = 0.1%	5.0	5.3	–	V
V_{no}	noise input voltage	unweighted; note 3	–	7	9	μV
		A-weighted; note 4	–	5	–	μV
THD + N	total harmonic distortion plus noise	f = 1 kHz; V_O = 3 V_{rms}; note 5	–	0.005	0.01	%
		f = 17 Hz to 20 kHz; note 6	–	0.01	–	%
SVRR	supply voltage ripple rejection	note 7	40	65	–	dB
		f = 20 Hz to 20 kHz; note 8	–	55	–	dB

Notes

1. The channel separation is determined by the parasitic capacitance between the inverting input left channel (pin 4) and the inverting input right channel (pin 5). The PCB layout has a major contribution to the parasitic capacitance. To obtain best results the PCB tracks to pin 4 and pin 5 should be separated as much as possible.
2. The frequency response is externally fixed by the input coupling capacitors.
3. Noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz with a source resistor R_s = 600 Ω.
4. Noise output voltage is measured in a bandwidth of 20 Hz to 20 kHz with an A-weighted filter with a source resistor R_s = 600 Ω.
5. Distortion is measured at a frequency of 1 kHz using an A-weighted filter.
6. Distortion is measured at an output voltage of 3.0 V (RMS) at frequencies between 17 Hz and 20 kHz.
7. Ripple rejection is measured at the output, using a source resistor R_s = 600 Ω and a ripple amplitude of 100 mV (RMS) at a frequency of 1 kHz.
8. Ripple rejection is measured at the output, using a source resistor R_s = 600 Ω and a ripple amplitude of 100 mV (RMS) at frequencies between 20 Hz and 20 kHz.

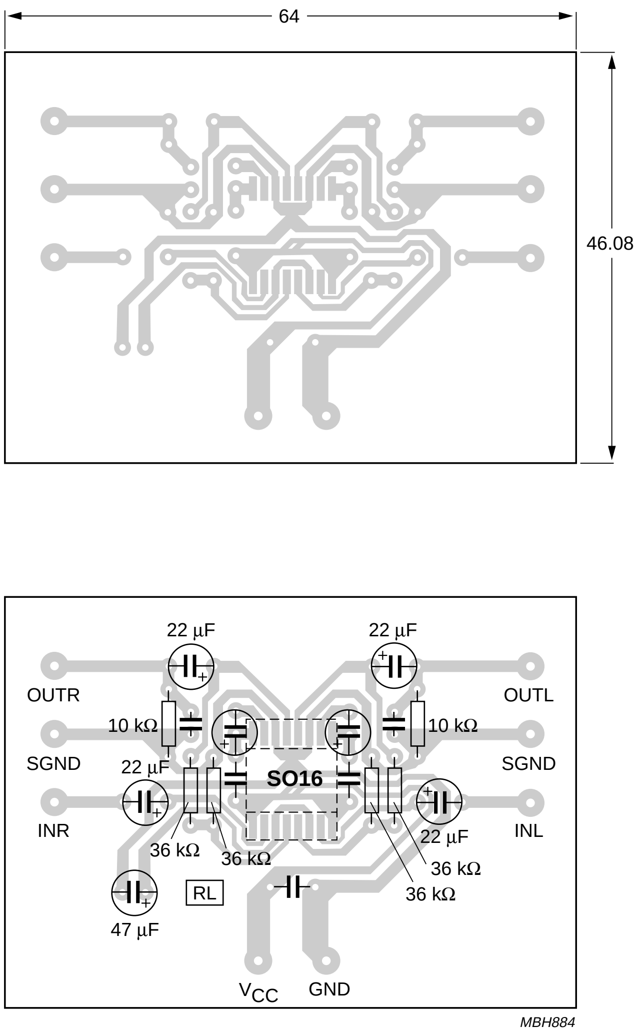
APPLICATION INFORMATION



(1) R1and R2 should have a tolerance of ≤ 1%.

Fig.3 Application diagram.

Printed Circuit Board (PCB) layout



Dimensions in mm.
IC mounted on track side, additional components mounted on component side.
Tracks viewed from component side.

Fig.4 Recommended PCB-layout.

Application characteristics

V_{CC} = 9 V; R_l = 10 kΩ; T_{amb} = 25 °C; 80 kHz filter.

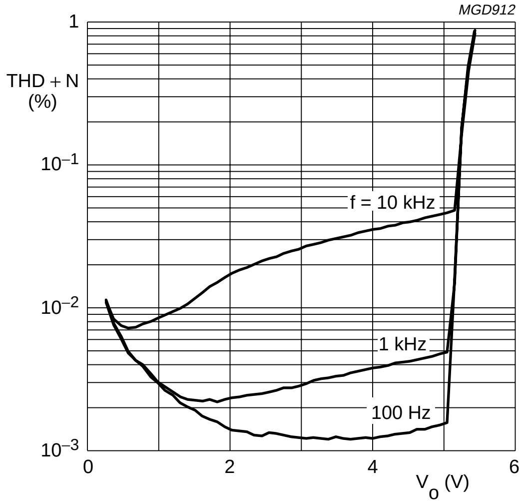


Fig.5 Total harmonic distortion plus noise as a function of V_o.

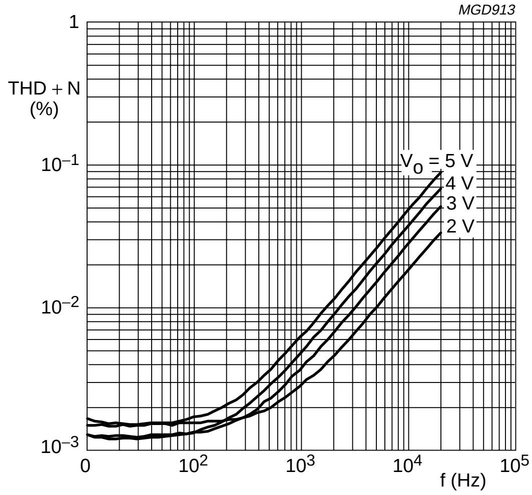


Fig.6 Total harmonic distortion plus noise as a function of frequency.

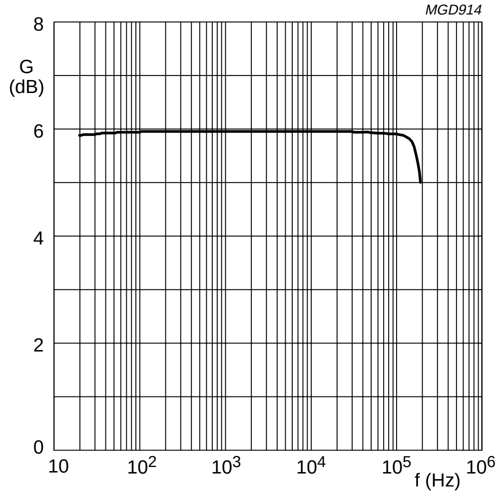


Fig.7 Total circuit gain as a function of frequency.

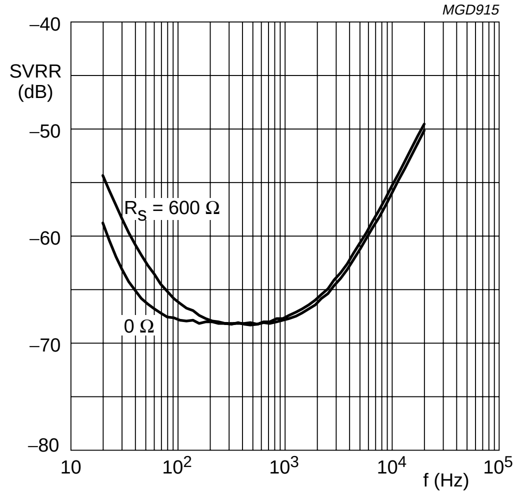


Fig.8 Supply voltage ripple rejection as a function of frequency.

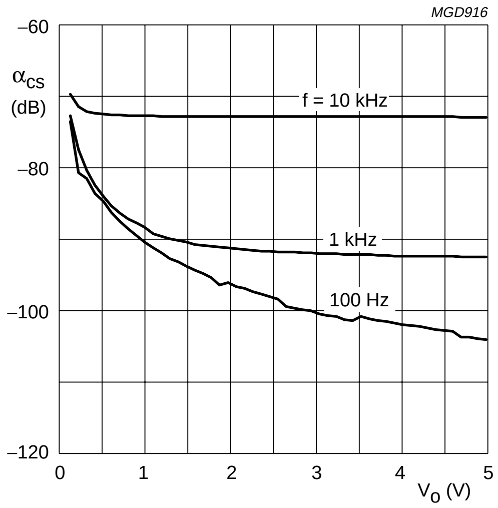


Fig.9 Channel separation as a function of V_o.

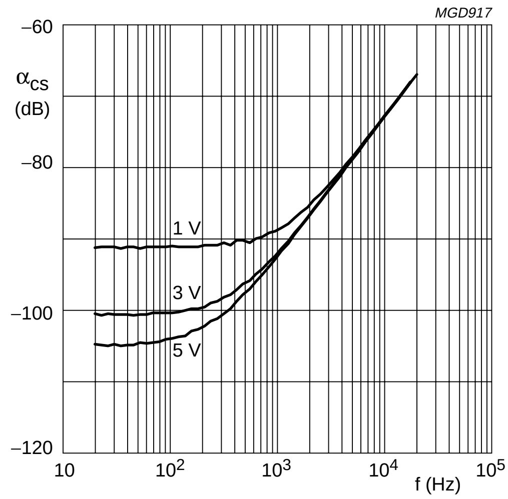
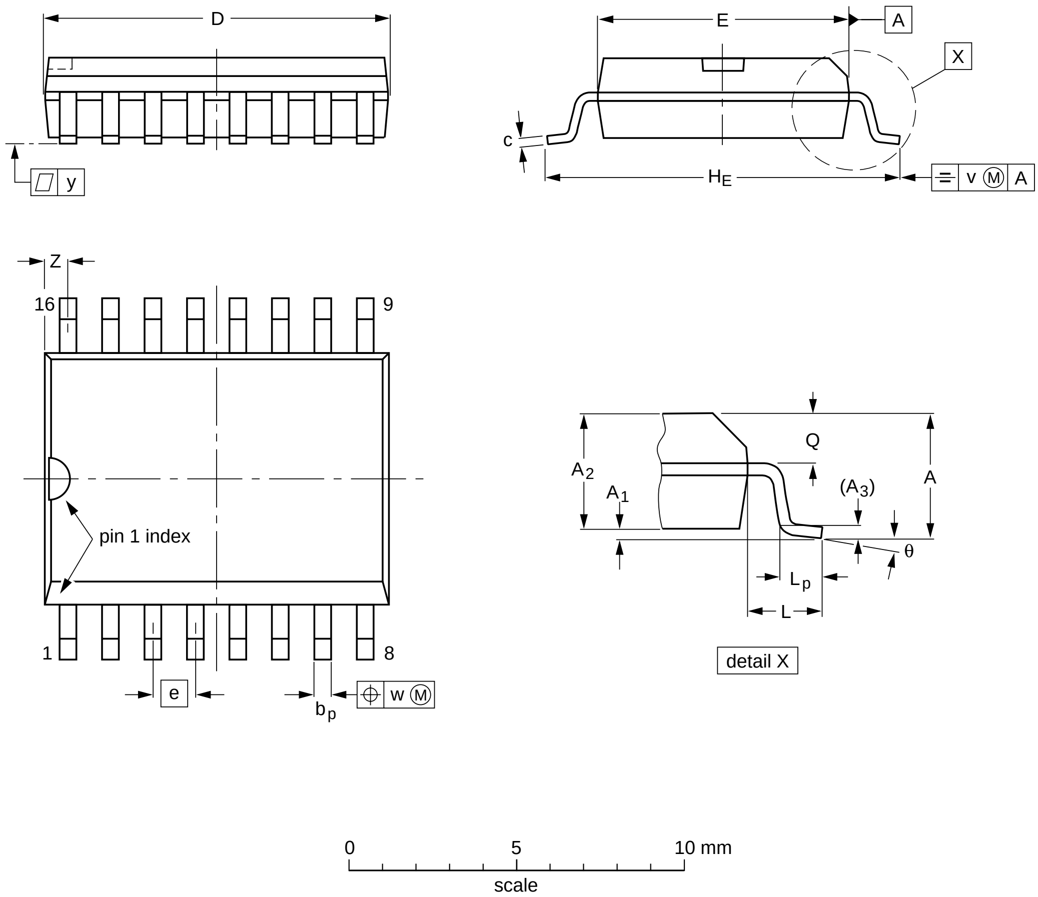


Fig.10 Channel separation as a function of frequency.

PACKAGE OUTLINE

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~95-01-24~~ 97-05-22

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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