

DATA SHEET

TDA8768

**12-bit high-speed Analog-to-Digital
Converter (ADC)**

Preliminary specification
Supersedes data of 1998 Feb 25
File under Integrated Circuits, IC02

1998 Aug 26

12-bit high-speed Analog-to-Digital Converter (ADC)

TDA8768

FEATURES

- 12-bit resolution
- Sampling rate up to 55 MHz
- –3 dB bandwidth of 190 MHz
- 5 V power supplies
- Binary or twos-complement CMOS outputs
- In-range CMOS-compatible output
- TTL-CMOS compatible static digital inputs
- 3 to 5 V CMOS-compatible digital outputs
- Differential clock input; Positive Emitter Coupled Logic (PECL)-compatible
- Power dissipation 325 mW (typical)
- Low analog input capacitance (typical 2 pF), no buffer amplifier required
- Integrated sample-and-hold amplifier
- Differential analog input
- External amplitude range control
- Voltage controlled regulator included.

APPLICATIONS

- High-speed analog-to-digital conversion for
 - Video signal digitizing
 - High Definition TV (HDTV)
 - Imaging (camera scanner)
 - Medical imaging
 - Telecommunication
 - Base-station receiver.

GENERAL DESCRIPTION

The TDA8768 is a bipolar 12-bit Analog-to-Digital Converter (ADC) optimized for telecommunications and professional imaging. It converts the analog input signal into 12-bit binary coded digital words at a maximum sampling rate of 55 MHz. All static digital inputs (SH, \overline{CE} and OTC) are TTL and CMOS compatible and all outputs are CMOS compatible. A sine wave clock input signal can also be used.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	33	tbf	mA
I_{CCD}	digital supply current		–	30	tbf	mA
I_{CCO}	output supply current	$f_{CLK} = 4 \text{ MHz}; f_i = 400 \text{ kHz}$	–	3.2	tbf	mA
INL	integral non-linearity	$f_{CLK} = 4 \text{ MHz}; f_i = 400 \text{ kHz}$	–	± 2.0	± 4.5	LSB
DNL	differential non-linearity	$f_{CLK} = 4 \text{ MHz}; f_i = 400 \text{ kHz}$	–	± 0.6	± 1.0	LSB
$f_{CLK(max)}$	maximum clock frequency					
	TDA8768H/4		40	–	–	MHz
	TDA8768H/5		55	–	–	MHz
P_{tot}	total power dissipation		–	325	tbf	mW

ORDERING INFORMATION

TYPE NUMBER	PACKAGE			SAMPLING FREQUENCY (MHz)
	NAME	DESCRIPTION	VERSION	
TDA8768H/4	QFP44	plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm	SOT307-2	40
TDA8768H/5				55

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BLOCK DIAGRAM

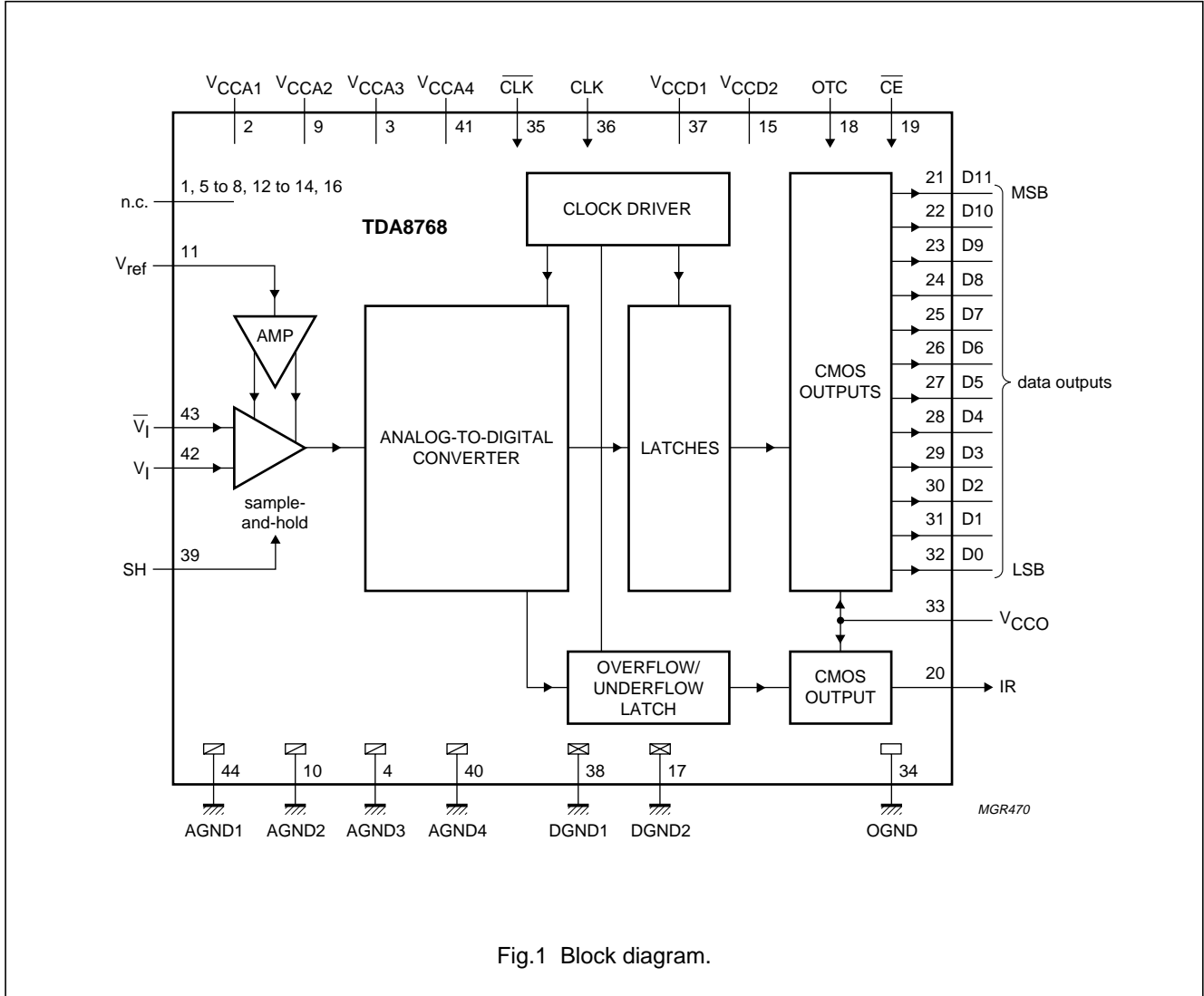


Fig.1 Block diagram.

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PINNING

SYMBOL	PIN	DESCRIPTION
n.c.	1	not connected
V _{CCA1}	2	analog supply voltage 1 (+5 V)
V _{CCA3}	3	analog supply voltage 3 (+5 V)
AGND3	4	analog ground 3
n.c.	5	not connected
n.c.	6	not connected
n.c.	7	not connected
n.c.	8	not connected
V _{CCA2}	9	analog supply voltage 2 (+5 V)
AGND2	10	analog ground 2
V _{ref}	11	reference voltage input
n.c.	12	not connected
n.c.	13	not connected
n.c.	14	not connected
V _{CCD2}	15	digital supply voltage 2 (+5 V)
n.c.	16	not connected
DGND2	17	digital ground 2
OTC	18	control input twos complement output; active HIGH
$\overline{\text{CE}}$	19	chip enable input (CMOS level; active LOW)
IR	20	in-range output
D11	21	data output; bit 11 (MSB)
D10	22	data output; bit 10

SYMBOL	PIN	DESCRIPTION
D9	23	data output; bit 9
D8	24	data output; bit 8
D7	25	data output; bit 7
D6	26	data output; bit 6
D5	27	data output; bit 5
D4	28	data output; bit 4
D3	29	data output; bit 3
D2	30	data output; bit 2
D1	31	data output; bit 1
D0	32	data output; bit 0 (LSB)
V _{CCO}	33	output supply voltage (3 to 5.25 V)
OGND	34	output ground
$\overline{\text{CLK}}$	35	complementary clock input; active LOW
CLK	36	clock input
V _{CCD1}	37	digital supply voltage 1 (+5 V)
DGND1	38	digital ground 1
SH	39	sample-and-hold enable input (CMOS level; active HIGH)
AGND4	40	analog ground 4
V _{CCA4}	41	analog supply voltage 4 (+5 V)
V _I	42	positive analog input voltage
\overline{V}_I	43	negative analog input voltage
AGND1	44	analog ground 1

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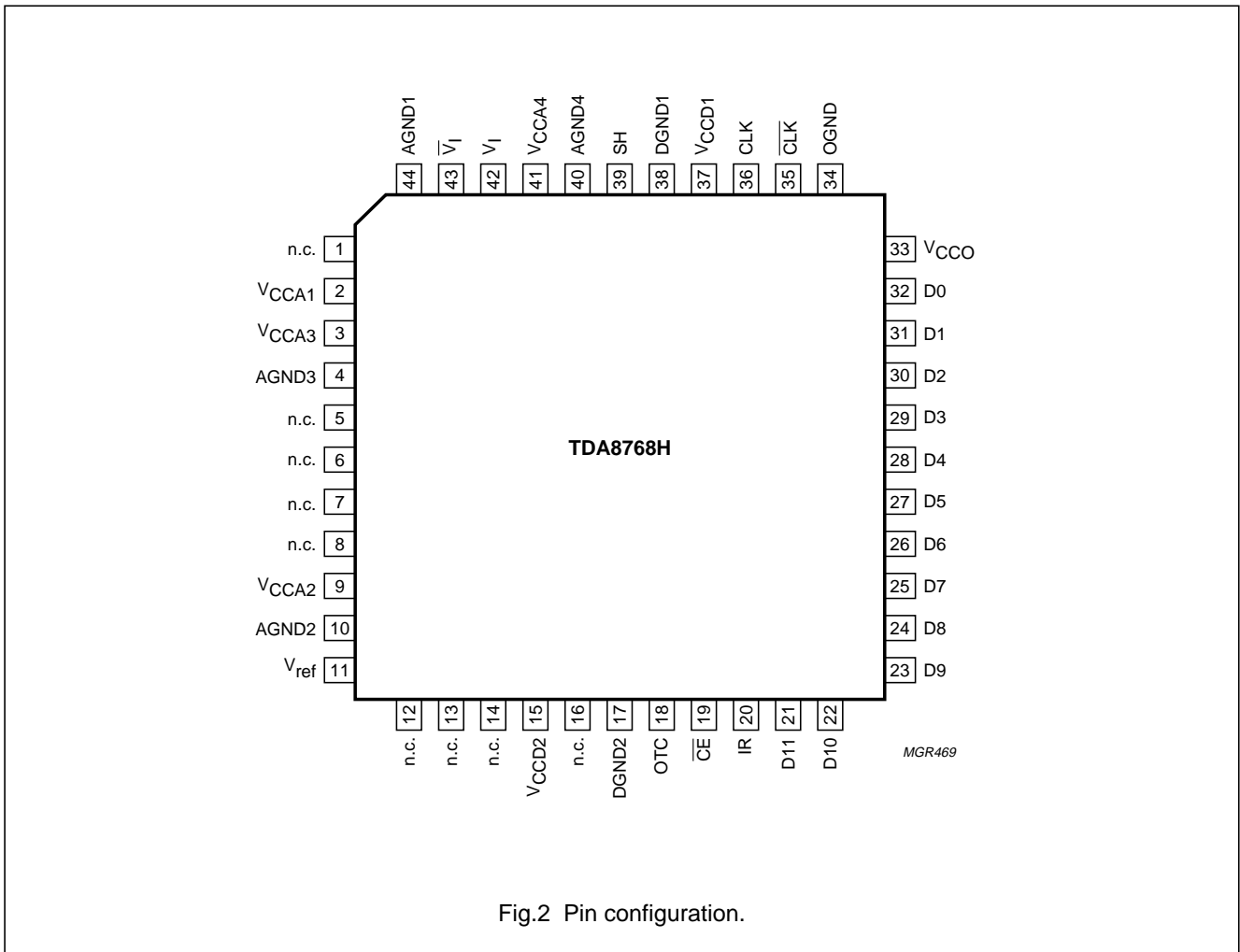


Fig.2 Pin configuration.

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LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CCA}	analog supply voltage	note 1	-0.3	+7.0	V
V_{CCD}	digital supply voltage	note 1	-0.3	+7.0	V
V_{CCO}	output supply voltage	note 1	-0.3	+7.0	V
ΔV_{CC}	supply voltage difference				
	$V_{CCA} - V_{CCD}$		-1.0	+1.0	V
	$V_{CCD} - V_{CCO}$		-1.0	+4.0	V
	$V_{CCA} - V_{CCO}$		-1.0	+4.0	V
V_I	input voltage at pins 42 and 43	referenced to AGND	0.3	V_{CCA}	V
$V_{i(p-p)}$	input voltage at pins 35 and 36 for differential clock drive (peak-to-peak value)		-	V_{CCD}	V
I_O	output current		-	10	mA
T_{stg}	storage temperature		-55	+150	°C
T_{amb}	operating ambient temperature		-10	+85	°C
T_j	junction temperature		-	150	°C

Note

- The supply voltages V_{CCA} , V_{CCD} and V_{CCO} may have any value between -0.3 V and +7.0 V provided that the supply voltage differences ΔV_{CC} are respected.

HANDLING

Inputs and outputs are protected against electrostatic discharges in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling integrated circuits.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	75	K/W

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CHARACTERISTICS

$V_{CCA} = V_2$ to V_{44} , V_9 to V_{10} , V_3 to V_4 and V_{41} to $V_{40} = 4.75$ to 5.25 V; $V_{CCD} = V_{37}$ to V_{38} and V_{15} to $V_{17} = 4.75$ to 5.25 V; $V_{CCO} = V_{33}$ to $V_{34} = 3.0$ to 5.25 V; AGND and DGND shorted together; $T_{amb} = 0$ to 70 °C; typical values measured at $V_{CCA} = V_{CCD} = 5$ V and $V_{CCO} = 3.3$ V, $T_{amb} = 25$ °C, $V_{I(p-p)} - \bar{V}_{I(p-p)} = 2.0$ V and $C_L = 10$ pF; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{CCA}	analog supply voltage		4.75	5.0	5.25	V
V_{CCD}	digital supply voltage		4.75	5.0	5.25	V
V_{CCO}	output supply voltage		3.0	3.3	5.25	V
I_{CCA}	analog supply current		–	33	45	mA
I_{CCD}	digital supply current		–	30	37	mA
I_{CCO}	output supply current	$f_{CLK} = 4$ MHz; $f_i = 400$ kHz	–	3.2	tbf	mA
		$f_{CLK} = 40$ MHz; $f_i = 4.43$ MHz	–	11	tbf	mA
Inputs						
CLK and \overline{CLK} (REFERENCED TO DGND)						
V_{IL}	LOW-level input voltage	$V_{CCD} = 5$ V; note 1	3.19	–	3.52	V
V_{IH}	HIGH-level input voltage	$V_{CCD} = 5$ V; note 1	3.83	–	4.12	V
I_{IL}	LOW-level input current	V_{CLK} or $V_{\overline{CLK}} = 3.19$ V	–10	–	–	μ A
I_{IH}	HIGH-level input current	V_{CLK} or $V_{\overline{CLK}} = 3.83$ V	–	–	10	μ A
Z_i	input impedance	$f_{CLK} = 40$ MHz	2	–	–	k Ω
C_i	input capacitance	$f_{CLK} = 40$ MHz	–	–	2	pF
$\Delta V_{CLK(p-p)}$	differential AC input voltage (peak-to-peak value) for switching ($V_{CLK} - V_{\overline{CLK}}$)	DC voltage level = 2.5 V	0.5	–	2.0	V
OTC, SH and \overline{CE} (REFERENCED TO DGND); see Tables 1 and 2						
V_{IL}	LOW-level input voltage		0	–	0.8	V
V_{IH}	HIGH-level input voltage		2.0	–	V_{CCD}	V
I_{IL}	LOW-level input current	$V_{IL} = 0.8$ V	–20	–	–	μ A
I_{IH}	HIGH-level input current	$V_{IH} = 2.0$ V	–	–	+20	μ A
V_I and \bar{V}_I (REFERENCED TO AGND); $V_{REF} = V_{CCA} - 1.825$ V; see Table 1						
I_{IL}	LOW-level input current		–	10	–	μ A
I_{IH}	HIGH-level input current		–	10	–	μ A
R_i	input resistance	$f_i = 4.43$ MHz	100	–	–	k Ω
C_i	input capacitance	$f_i = 4.43$ MHz	–	–	2	pF
$V_{I(CM)}$	common mode input voltage	$V_I = \bar{V}_I$; output code 2047 $V_{CCA} = 5$ V	tbf	3.6	tbf	V
		$V_{CCA} = 4.75$ V	tbf	3.35	tbf	V
		$V_{CCA} = 5.25$ V	tbf	3.85	tbf	V

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Voltage controlled regulator input V_{ref} (referenced to AGND); note 2						
$V_{ref(FS)}$	full-scale fixed voltage	$V_{CCA} = 5\text{ V}$	–	3.175	–	V
I_{ref}	input current		–	0.5	10	μA
$V_{I(p-p)} - \bar{V}_{I(p-p)}$	input voltage amplitude (peak-to-peak value)	$V_{ref} = V_{CCA} - 1.825\text{ V}$	–	2.0	–	V
Outputs (referenced to OGND)						
DIGITAL OUTPUTS D11 TO D0 AND IR (REFERENCED TO OGND)						
V_{OL}	LOW-level output voltage	$I_{OL} = 2\text{ mA}$	0	–	0.5	V
V_{OH}	HIGH-level output voltage	$I_{OH} = -0.4\text{ mA}$	$V_{CCO} - 0.5$	–	V_{CCO}	V
I_o	output current in 3-state	output level between 0.5 V and V_{CCO}	–20	–	+20	μA
Switching characteristics						
CLOCK FREQUENCY f_{CLK} ; see Fig.3						
$f_{CLK(min)}$	minimum clock frequency	SH = HIGH	–	–	2	MHz
$f_{CLK(max)}$	maximum clock frequency TDA8768H/4 TDA8768H/5		40	–	–	MHz
			55	–	–	MHz
t_{CLKH}	clock pulse width HIGH		8.5	–	–	ns
t_{CLKL}	clock pulse width LOW		8.5	–	–	ns
Analog signal processing; 50% clock duty factor; $V_I - \bar{V}_I = 2.0\text{ V}$; $V_{ref} = V_{CCA} - 1.825\text{ V}$; see Table 1						
LINEARITY						
INL	integral non-linearity	$f_{CLK} = 4\text{ MHz}$; $f_i = 400\text{ kHz}$	–	± 2.0	± 4.5	LSB
DNL	differential non-linearity	$f_{CLK} = 4\text{ MHz}$; $f_i = 400\text{ kHz}$; no missing code	–	± 0.6	± 1.0	LSB
E_{offset}	offset error	$V_{CCA} = V_{CCD} = V_{CCO} = 5\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_I = \bar{V}_I$; output code = 2047	tbf	–11	tbf	mV
$E_{G(FS)}$	gain error amplitude (full scale); spread from device to device	$V_{CCA} = V_{CCD} = V_{CCO} = 5\text{ V}$; $T_{amb} = 25\text{ }^\circ\text{C}$; $V_{I(p-p)} - \bar{V}_{I(p-p)} = 2.0\text{ V}$	–5	–	+5	%
BANDWIDTH ($f_{CLK} = 55\text{ MHz}$); note 3						
B	analog bandwidth	–3 dB; full scale input	tbf	190	–	MHz
HARMONICS ($f_{CLK} = 40\text{ MHz}$)						
$h_{fund(FS)}$	fundamental harmonics (full scale)	$f_i = 4.43\text{ MHz}$	–	–	0	dB
$h_{tot(FS)}$	harmonics (full scale); all components second harmonic third harmonic					
			–	–75	–	dB
			–	–70	–	dB
THD	total harmonic distortion	$f_i = 4.43\text{ MHz}$; note 4	–	–66	–	dB

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SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THERMAL NOISE						
$N_{th(rms)}$	thermal noise (RMS value)	grounded input; $f_{CLK} = 40$ MHz	–	0.25	tbf	LSB
SPURIOUS FREE DYNAMIC RANGE						
DR_{sf}	spurious free dynamic range	$f_i = 4.43$ MHz	tbf	69	–	dB
		$f_i = 10$ MHz	tbf	tbf	–	dB
		$f_i = 20$ MHz	tbf	tbf	–	dB
SIGNAL-TO-NOISE RATIO; note 5						
S/N	signal-to-noise ratio	without harmonics; $f_{CLK} = 40$ MHz; $f_i = 4.43$ MHz	–	67	–	dB
EFFECTIVE NUMBER OF BITS; note 5						
N_{bit}	effective number of bits TDA8768H/4 ($f_{CLK} = 40$ MHz)	$f_i = 4.43$ MHz	–	10.3	–	bits
		$f_i = 10$ MHz	–	tbf	–	bits
		$f_i = 15$ MHz	–	tbf	–	bits
	effective number of bits TDA8768H/5 ($f_{CLK} = 55$ MHz)	$f_i = 4.43$ MHz	–	9.9	–	bits
		$f_i = 10$ MHz	–	tbf	–	bits
		$f_i = 15$ MHz	–	tbf	–	bits
		$f_i = 20$ MHz	–	tbf	–	bits
INTERMODULATION; note 6						
TTIR	two-tone intermodulation rejection	$f_{CLK} = 40$ MHz	tbf	66	–	dB
d_3	third order intermodulation distortion	$f_{CLK} = 40$ MHz	tbf	67	–	dB
BIT ERROR RATE						
BER	bit error rate	$f_{CLK} = 40$ MHz; $f_i = 4.43$ MHz; $V_1 = \pm 16$ LSB at code 2047	–	10^{-15}	tbf	times/ sample
Timing ($C_L = 10$ pF); see Fig.3 and note 7						
$t_{d(s)}$	sampling delay time		–	–	2	ns
t_h	output hold time		4	–	–	ns
t_d	output delay time	$V_{CCO} = 5.25$ V	–	10	15	ns
		$V_{CCO} = 3.0$ V		13	18	ns
3-state output delay times; see Fig.4						
t_{dZH}	enable HIGH		–	14	18	ns
t_{dZL}	enable LOW		–	16	20	ns
t_{dHZ}	disable HIGH		–	16	20	ns
t_{dLZ}	disable LOW		–	14	18	ns

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Notes

- The circuit has two clock inputs: CLK and $\overline{\text{CLK}}$. There are four modes of operation:
 - PECL mode 1: (DC level varies 1 : 1 with V_{CCD}) CLK and $\overline{\text{CLK}}$ inputs are at differential PECL levels.
 - PECL mode 2: (DC level varies 1 : 1 with V_{CCD}) CLK input is at PECL level and sampling is taken on the falling edge of the clock input signal. A DC level of 3.65 V has to be applied on $\overline{\text{CLK}}$ decoupled to GND via a 100 nF capacitor.
 - PECL mode 3: (DC level varies 1 : 1 with V_{CCD}) $\overline{\text{CLK}}$ input is at PECL level and sampling is taken on the rising edge of the clock input signal. A DC level of 3.65 V has to be applied on CLK decoupled to GND via a 100 nF capacitor.
 - AC driving mode 4: when driving the CLK input directly and with any AC signal of minimum 0.5 V (peak-to-peak value) and with a DC level of 2.5 V, the sampling takes place at the falling edge of the clock signal. When driving the CLK input with the same signal, sampling takes place at the rising edge of the clock signal. It is recommended to decouple the $\overline{\text{CLK}}$ or CLK input to DGND via a 100 nF capacitor.
- It is possible with an external reference connected to pin V_{ref} to adjust the ADC input range. This voltage has to be referenced to V_{CCA} . For $V_{\text{CCA}} - 1.825$ V, the differential input voltage amplitude is 2 V (peak-to-peak value).
- The -3 dB analog bandwidth is determined by the 3 dB reduction in the reconstructed output, the input being a full-scale sine wave.
- THD (total harmonic distortion) is obtained with the addition of the first five harmonics:

$$\text{THD} = 20 \log \frac{F}{\sqrt{(2\text{nd})^2 + (3\text{rd})^2 + (4\text{th})^2 + (5\text{th})^2 + (6\text{th})^2}}$$

where F is the fundamental harmonic referenced at 0 dB for a full-scale sine wave input.

- Effective number of bits are obtained via a Fast Fourier Transform (FFT). The calculation takes into account all harmonics and noise up to half of the clock frequency (Nyquist frequency). Conversion to SNR:
 $\text{SNR} = N_{\text{bit}} \times 6.02 + 1.76$ dB.
- Intermodulation measured relative to either tone with analog input frequencies of 4.43 and 4.53 MHz. The two input signals have the same amplitude and the total amplitude of both signals provides full-scale to the converter (-6 dB below full-scale for each input signal).
 d_3 is the ratio of the RMS value of either input tone to the RMS value of the worst case third order intermodulation product.
- Output data acquisition: the output data is available after the maximum delay of t_d .

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Table 1 Output coding with differential inputs (typical values to AGND); $V_{I(p-p)} - \bar{V}_{I(p-p)} = 2.0\text{ V}$; $V_{\text{ref}} = V_{\text{CCA}} - 1.825\text{ V}$

CODE	$V_{I(p-p)}$	$\bar{V}_{I(p-p)}$	IR	BINARY OUTPUTS	TWOS COMPLEMENT OUTPUTS
				D11 TO D0	D11 TO D0
Underflow	<3.1	>4.1	0	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
0	3.1	4.1	1	0 0 0 0 0 0 0 0 0 0 0 0	1 0 0 0 0 0 0 0 0 0 0 0
1	–	–	1	0 0 0 0 0 0 0 0 0 0 0 1	1 0 0 0 0 0 0 0 0 0 0 1
↓	–	–	↓	↓	↓
2047	3.6	3.6	1	0 1 1 1 1 1 1 1 1 1 1 1	1 1 1 1 1 1 1 1 1 1 1 1
↓	–	–	↓	↓	↓
4094	–	–	1	1 1 1 1 1 1 1 1 1 1 1 0	0 1 1 1 1 1 1 1 1 1 1 0
4095	4.1	3.1	1	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1
Overflow	>4.1	<3.1	0	1 1 1 1 1 1 1 1 1 1 1 1	0 1 1 1 1 1 1 1 1 1 1 1

Table 2 Mode selection

OTC	$\overline{\text{CE}}$	D0 TO D11 AND IR
0	0	binary; active
1	0	twos complement; active
X ⁽¹⁾	1	high impedance

Note

- X = don't care.

Table 3 Sample-and-hold selection

SH	SAMPLE-AND-HOLD
1	active
0	inactive; tracking mode

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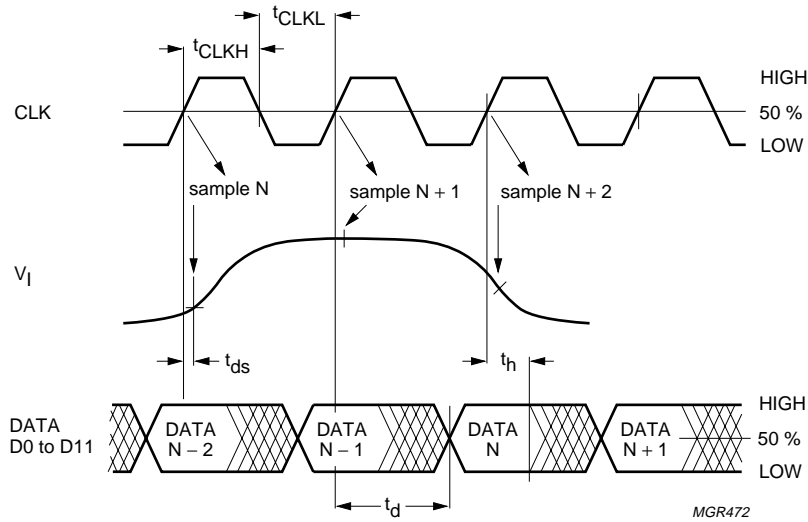
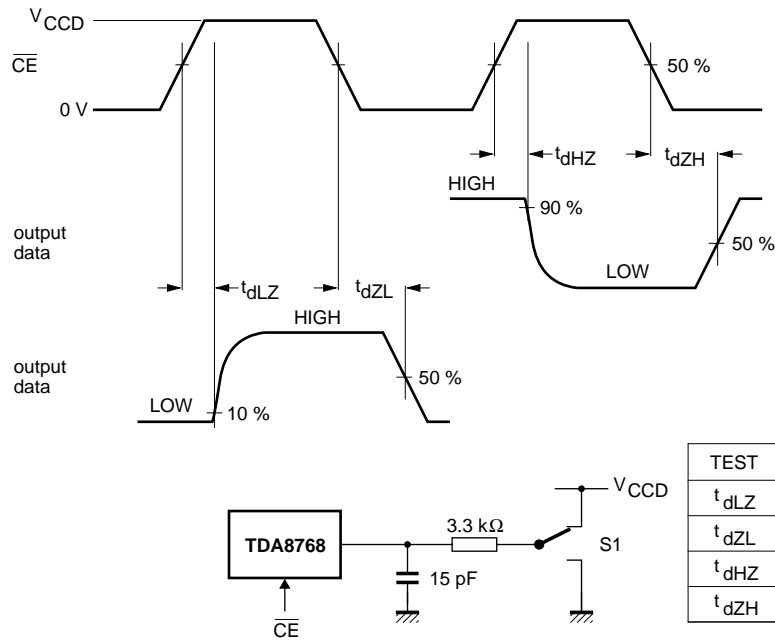


Fig.3 Timing diagram.



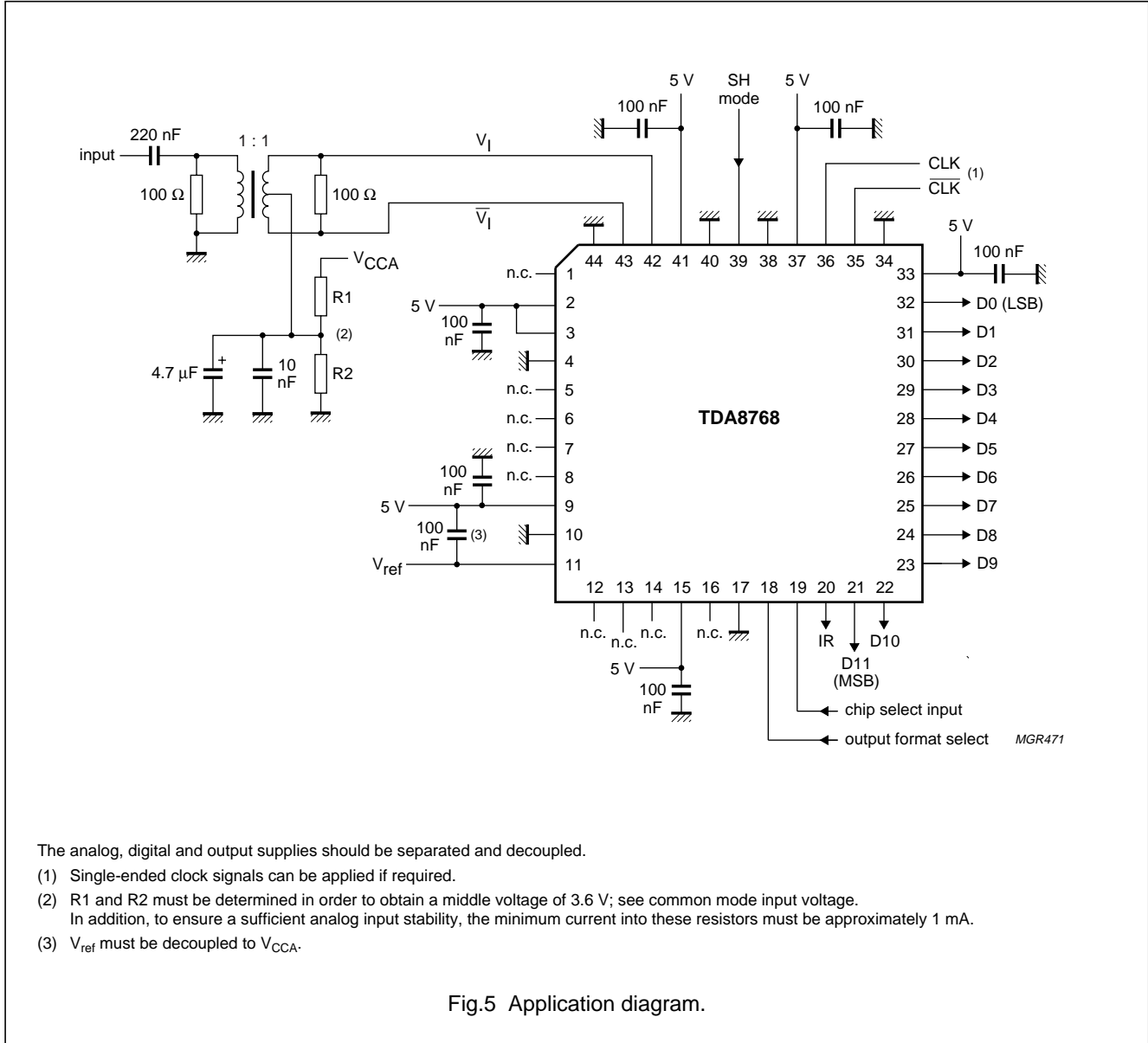
$f_{\overline{CE}} = 100 \text{ kHz}$.

Fig.4 Timing diagram and test conditions of 3-state output delay time.

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APPLICATION INFORMATION



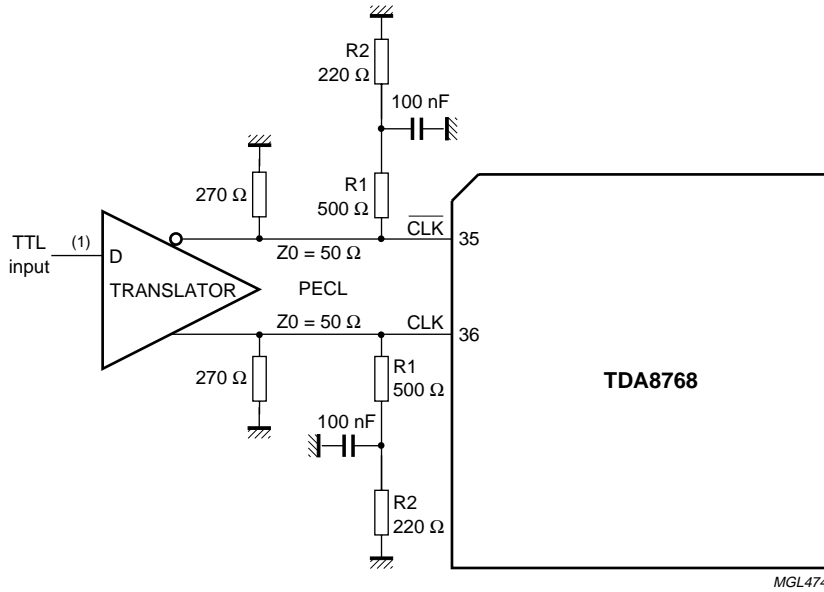
The analog, digital and output supplies should be separated and decoupled.

- (1) Single-ended clock signals can be applied if required.
- (2) R1 and R2 must be determined in order to obtain a middle voltage of 3.6 V; see common mode input voltage. In addition, to ensure a sufficient analog input stability, the minimum current into these resistors must be approximately 1 mA.
- (3) V_{ref} must be decoupled to V_{CCA}.

Fig.5 Application diagram.

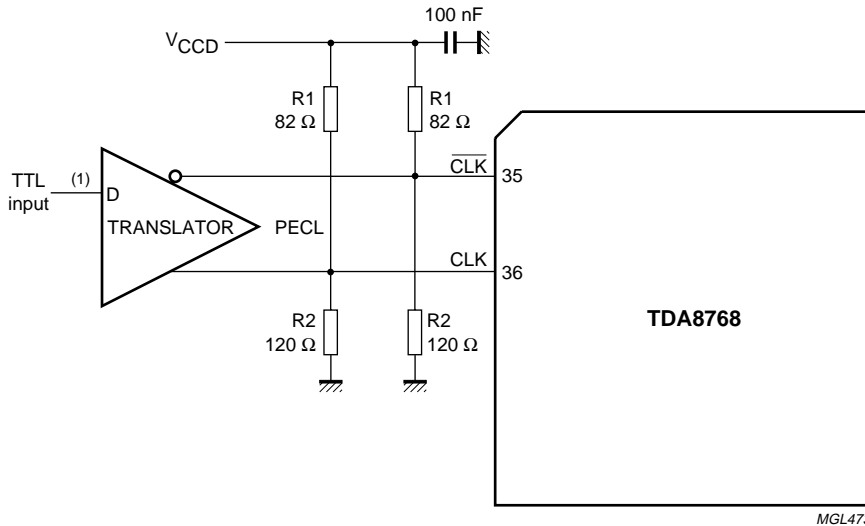
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If the clock lines are more than 1 inch long they must be matched. In fact, the 27 Ω resistor will be changed by the series connection of R1 and R2, with R1 = Z_0 placed close to pins CLK and CLK. (1) 50 Ω matched line (Z_0 , L).

Fig.6 Application diagram for differential clock input (PECL-compatible) using a TTL to PECL translator.



The value of R1 and R2 must be chosen in order to meet the following relations:

$$3\text{ V} = \frac{V_{\text{CCD}} \times R2}{R1 + R2} \text{ and } Z0 = \frac{R1 \times R2}{R1 + R2}$$

(1) 50 Ω matched line (Z_0 , L).

Fig.7 Application diagram for differential clock input (PECL-compatible) using a TTL to PECL translator and Thevenin parallel terminations.

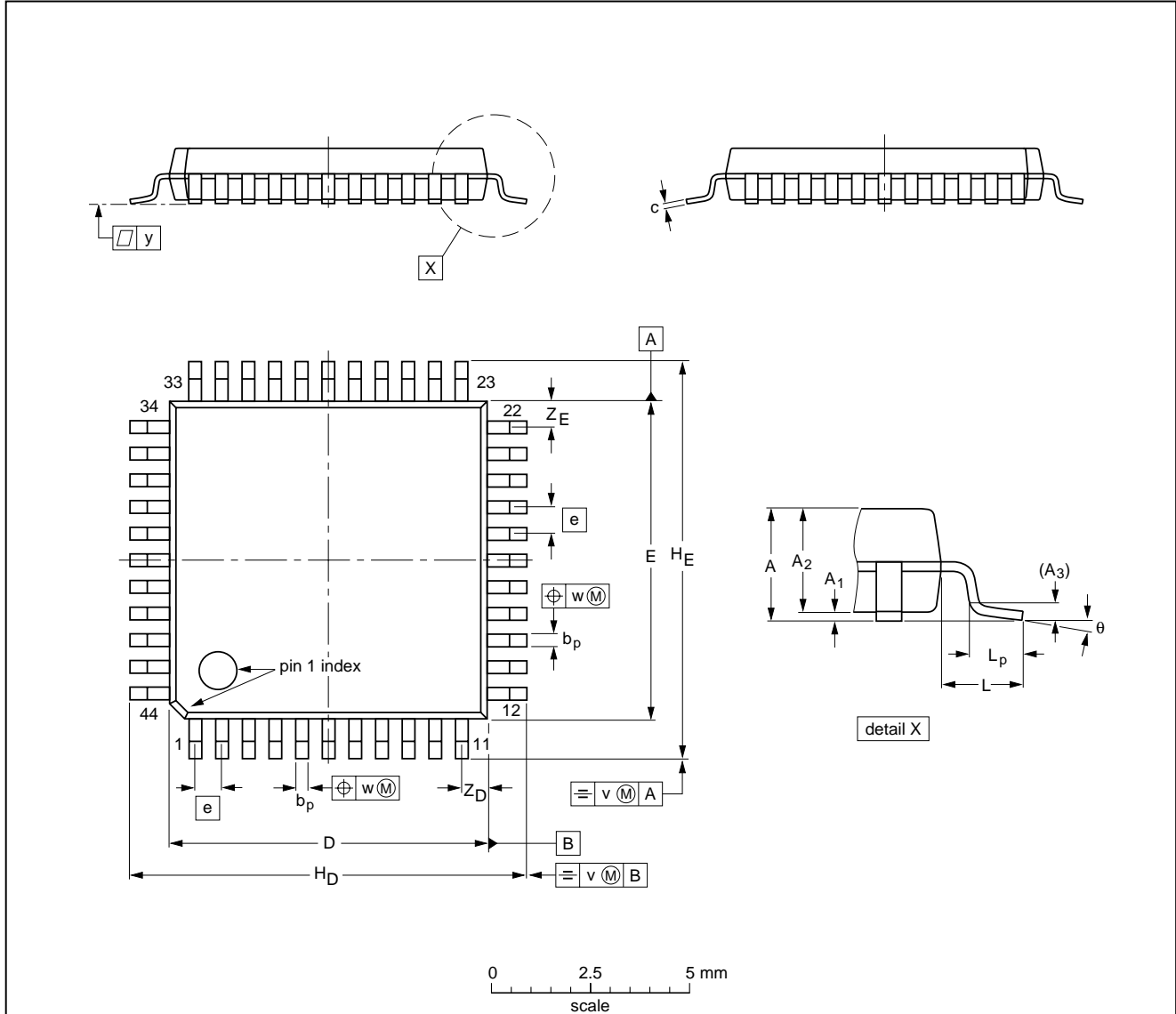
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PACKAGE OUTLINE

QFP44: plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 x 10 x 1.75 mm

SOT307-2



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _D	H _E	L	L _p	v	w	y	Z _D ⁽¹⁾	Z _E ⁽¹⁾	θ
mm	2.10	0.25 0.05	1.85 1.65	0.25	0.40 0.20	0.25 0.14	10.1 9.9	10.1 9.9	0.8	12.9 12.3	12.9 12.3	1.3	0.95 0.55	0.15	0.15	0.1	1.2 0.8	1.2 0.8	10° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT307-2						95-02-04 97-08-01

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

12-bit high-speed Analog-to-Digital Converter (ADC)

TDA8768

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

12-bit high-speed Analog-to-Digital
Converter (ADC)

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NOTES

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NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 160 1010, Fax. +43 160 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 0044

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor, 254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025, Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division, Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510, Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762, Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2865, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 625 344, Fax. +381 11 635 777

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: <http://www.semiconductors.philips.com>

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