INTEGRATED CIRCUITS

DATA SHEET

UMA1022M
Low cost dual frequency synthesizer for radio telephones

Product specification
Supersedes data of 1998 May 15
File under Integrated Circuits, IC17

1998 Dec 09

Philips
Semiconductors

PHILIPS

Low cost dual frequency synthesizer for radio telephones

UMA1022M

FEATURES

- Low phase noise
- Low current from 3 V supply
- Fully programmable dividers
- 3-line serial interface bus
- Input reference buffer configurable as an oscillator with external crystal resonator
- Wide compliance voltage charge pump outputs
- Two power-down input control pins.

APPLICATIONS

- 900 MHz and 2 GHz digital radio telephones
- Portable battery-powered radio equipment.

GENERAL DESCRIPTION

The UMA1022M BICMOS device integrates prescalers, programmable dividers, a crystal oscillator/buffer and phase comparators to implement two phase-locked loops. The device is designed to operate from 3 NiCd or a single LiIon cell in pocket phones, or from an external 3 V supply.

The synthesizers operate at RF input frequencies up to 2.1 GHz and 550 MHz. All divider ratios are supplied via a 3-wire serial programming bus. The reference divider uses a common, fully programmable part and a separate subdivider section. In this way the comparison frequencies are related to each other allowing optimum isolation between charge pump pulses.

Separate power and ground pins are provided to the analog (charge pump, prescaler) and digital (CMOS) circuits. An independent supply for the crystal oscillator section allows maximum frequency stability. The ground leads should be externally short-circuited to prevent large currents flowing across the die and thus causing damage. V_{DD} and V_{DDX} must be at the same potential. V_{CCA} and V_{CCB} must be equal to each other and equal to or greater than V_{DD} (e.g. V_{DD} = 3 V and V_{CCA} = 5.5 V for wider VCO control voltage range).

The charge pump currents (phase detector gain) are fixed by internal resistances and controlled by the serial interface. Only passive loop filters are necessary; the charge pumps function within a wide voltage compliance range to improve the overall system performance.

Suitable pin layout is chosen to minimize coupling and interference between signals entering or leaving the chip.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	digital supply voltage	$V_{CCA} = V_{CCB} \geq V_{DD}$	2.7	3.0	5.5	V
V_{CCA}, V_{CCB}	analog supply voltages	$V_{CCA} = V_{CCB} \geq V_{DD}$	2.7	3.0	5.5	V
V_{DDX}	crystal reference supply voltage	$V_{DDX} = V_{DD}$	2.7	3.0	5.5	V
I_{tot}	all supply currents ($I_{DD} + I_{CCA} + I_{CCB} + I_{DDX}$) in active mode	$\overline{E}$ = 1; $V_{CCA} = V_{CCB}$ = 3.0 V; $V_{DDX} = V_{DD}$ = 3.0 V				
		XON = 0	–	14.65	–	mA
		XON = 1	–	15.9	–	mA
$I_{tot(pd)}$	total supply currents in power-down mode		–	40	–	µA
f_{RF}	RF input frequency		300	–	2100	MHz
f_{IF}	IF input frequency	$V_{CCA} = V_{CCB} \leq 4.0$ V	50	–	550	MHz
			50	–	400	MHz
f_{xtal}	crystal reference oscillator frequency		3	–	20	MHz
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
T_{amb}	operating ambient temperature		–30	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UMA1022M	SSOP20	plastic shrink small outline package; 20 leads; body width 4.4 mm	SOT266-1

BLOCK DIAGRAM

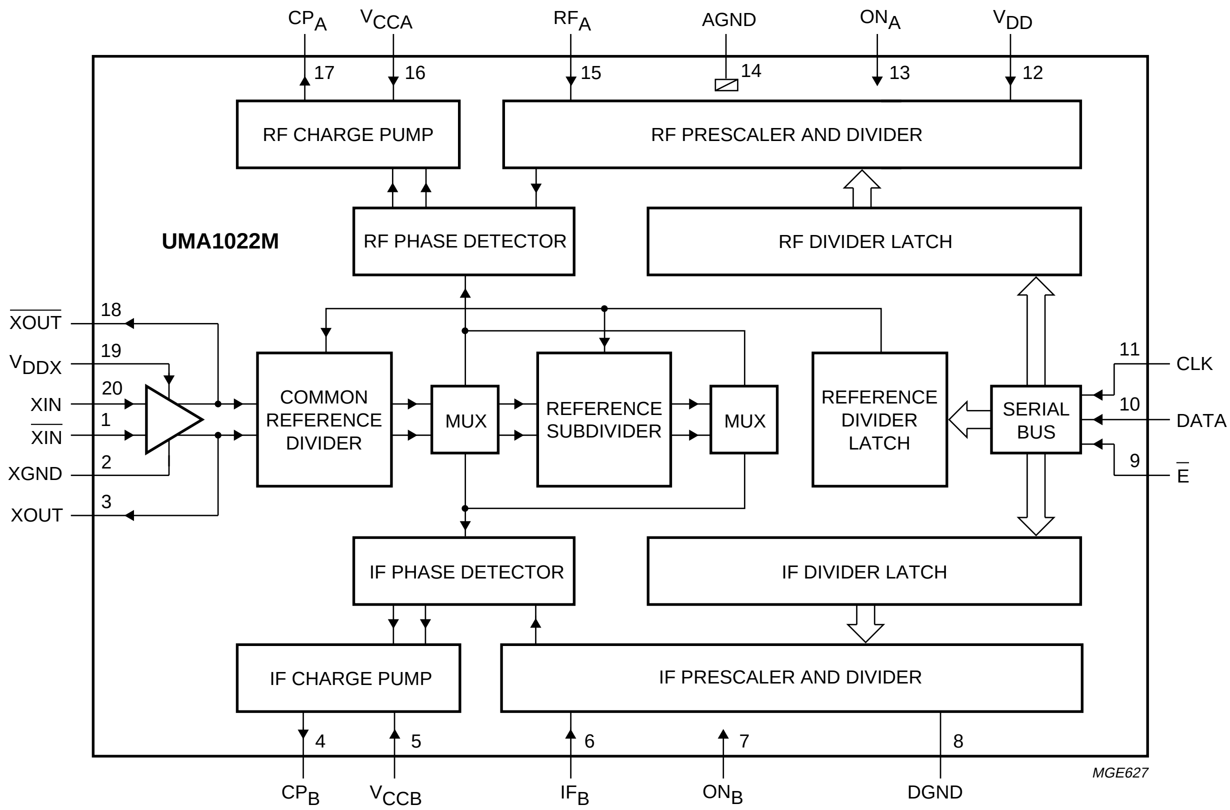


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{XIN}$	1	inverting crystal reference input
XGND	2	ground for crystal oscillator circuits
XOUT	3	crystal oscillator buffer output
CP_B	4	IF synthesizer charge pump output
V_{CCB}	5	analog supply to IF synthesizer
IF_B	6	IF VCO main divider input
ON_B	7	IF power-on input; ON_B = HIGH means IF synthesizer is active
DGND	8	digital circuits ground
$\overline{E}$	9	programming bus enable input
DATA	10	programming bus data input
CLK	11	programming bus clock input
V_{DD}	12	digital circuits supply voltage
ON_A	13	RF power-on input; ON_A = HIGH means RF synthesizer is active
AGND	14	analog circuits ground
RF_A	15	RF VCO main divider input
V_{CCA}	16	analog supply to RF synthesizer
CP_A	17	RF synthesizer charge pump output
$\overline{XOUT}$	18	inverting oscillator buffer output
V_{DDX}	19	supply voltage to crystal oscillator circuits
XIN	20	non-inverting crystal reference input

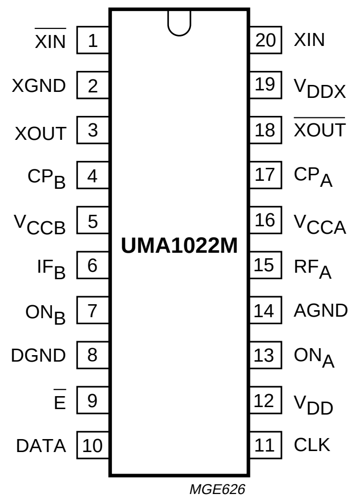


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Main dividers

The main dividers are clocked at pin RF_A by the RF oscillator signal and at pin IF_B by the IF oscillator signal. The inputs are AC coupled through external capacitors. Input impedances are high, dominated by parasitic package capacitances, so matching is off-chip.
The sensitive dividers operate with signal levels from 35 to 225 mV (RMS), at frequencies up to 2.1 GHz (RF part) and up to 550 MHz (IF part). Both include programmable bipolar prescalers followed by CMOS counters. The RF main divider allows programmable ratios from 512 to 65535; the IF blocks accept values between 128 and 16383.

Crystal oscillator

A fully differential low-noise amplifier/buffer is integrated providing outputs to drive other circuits, and to build a crystal oscillator; only needed are an external resonance circuit and tuning elements (temperature compensation). A bus controlled power-down mode disables the low-noise amplifier to reduce current if not needed.

The normal differential input pins drive a clock buffer to provide edges to the programmable reference divider at frequencies up to 20 MHz. The inputs are AC coupled through external capacitors, and operate with signals down to 35 mV (RMS) and up to 0.5 V (RMS).

Various crystal oscillator structures can be built using the amplifier. By coupling one output back to the appropriate input through the resonator, and decoupling the other input to ground, the second output becomes available to deliver the reference frequency to other circuits.

Reference dividers

A first common divider circuit produces an output frequency for RF or IF synthesizer phase comparison, depending on the P/A bit. It drives a second independent divider, which delivers the reference edge to the IF or RF synthesizer phase comparator. When P/A is logic 1, the output of the subdivider is connected to the RF phase comparator, whereas the output of the common divider is connected to the IF phase detector.

The phase comparators run at related frequencies with a controlled phase difference to avoid interference when in-lock. The common 10-bit section permits divide ratios from 8 to 1023; the second subdivider allows phase comparison frequency ratios between 1 and 16. Table 2 indicates how to program the corresponding bits to get the wanted ratio.

Phase comparators

The phase detectors are driven by the output edges selected by the main and reference dividers. Each generates lead and lag signals to control the appropriate charge pump. The pumps output current pulses appear at pins CP_A (RF synthesizer) and CP_B (IF synthesizer). The current pulse duration is at least equal to the difference in time of arrival of the edges from the two dividers. If the main divider edge arrives first, CP_A or CP_B sink current. If the reference divider edge arrives first, CP_A or CP_B source current. For correct PLL operation the VCOs need to have a positive frequency/voltage control slope.

The currents at CP_A and CP_B are programmed via the serial bus as multiples of an internally-set reference current. The passage into power-down mode is synchronized with respect to the phase detector to prevent output current pulses being interrupted. Additional circuitry is included to ensure that the gain of the phase comparators remains linear even for small phase errors.

Serial programming bus

A simple 3-line unidirectional serial bus is used to program the circuit. The 3 lines are DATA, clock (CLK) and enable ($\overline{E}$). The data sent to the device is loaded in bursts framed by $\overline{E}$. Programming clock edges and their appropriate data bits are ignored until $\overline{E}$ goes active LOW. The programmed information is loaded into the addressed latch when $\overline{E}$ returns HIGH. During normal operation, $\overline{E}$ should be kept HIGH. Only the last 19 bits serially clocked into the device are retained within the programming register.

Additional leading bits are ignored, and no check is made on the number of clock pulses. The NMOS-rich design uses virtually no current when the bus is inactive; power-up is initiated when enable is taken LOW, and power-down occurs a short time after enable returns HIGH. Bus activity is allowed when either synthesizer is active or in power-down (ON_A and ON_B inputs LOW) mode. Fully static CMOS registers retain programmed data whatever the power-down state, as long as the supply voltage is present.

Data format

The leading bits (dt15 to dt0) make up the data field, while the trailing three bits (ad2 to ad0) comprise an address field. The UMA1022M uses 4 of the 8 available addresses. The data format is shown in Table 1. The first bit entered is dt15, the last bit is ad0. For the divider ratios, the first bits entered (P0 and R0) are the Least Significant Bits (LSB). **This is different from previous Philips synthesizers.**

The trailing address bits are decoded on the rising edge of $\overline{E}$. This produces an internal load pulse to store the data in the addressed latch. To avoid erroneous divider ratios, the load pulse is not allowed during data reads by the frequency dividers. This condition is guaranteed by respecting a minimum $\overline{E}$ pulse width after data transfer.The test register bits should not normally be programmed active (HIGH); normal operation requires them set LOW. When the supply voltage is established an internal power-up initialization pulse is generated to preconfigure the circuit state. Production testing does not verify that all bits are preconfigured correctly.

Power-down mode

The RF and IF synthesizers are **on** when respectively the input signal ON_A and ON_B are HIGH. When turned **on**, the dividers and phase detector are synchronized to avoid random phase errors. When turned **off**, the phase detector is synchronized to avoid interrupting charge pump pulses. The UMA1022M has a very low current consumption in the power-down mode.

Table 1 Bit allocation; note 1

FIRST IN							REGISTER BIT ALLOCATION											LAST IN
DATA FIELD																ADDRESS		
dt15	**dt14**	**dt13**	**dt12**	**dt11**	**dt10**	**dt9**	**dt8**	**dt7**	**dt6**	**dt5**	**dt4**	**dt3**	**dt2**	**dt1**	**dt0**	**ad2**	**ad1**	**ad0**
Test bits[2]				CPI	S/D	XON[3]	X	X	X	X	P/A[4]	REFDIV2[5]				0	1	1
P0[6]	RF synthesizer main divider coefficient														P15	0	0	0
X	X	X	X	X	X	R0[6]	reference divider coefficient								R9	0	0	1
X	X	A0[6]	IF synthesizer main divider coefficient												A13	0	1	0

Notes

1. X = don't care.
2. The test bits (at address 011) should not be programmed with any other value except all zeros for normal operation.
3. Bit XON = power-on of crystal oscillator low-noise amplifier; logic 1 turns **on** circuit block.
4. Bit P/A = 1 selects the output of the reference subdivider to the RF synthesizer and the output of the common reference divider to the IF synthesizer.
5. The coefficient REFDIV2 (4 bits) selects the phase comparison ratio (1 to 16) between IF and RF synthesizers (see Table 2).
6. P0 is the LSB of the RF main divider coefficient; R0 is the LSB of the reference divider coefficient; A0 is the LSB of the IF main divider.

Table 2 Programming the coefficient REFDIV2 for reference subdivider

dt3 (LSB)	dt2	dt1	dt0 (MSB)	REFDIV2
0	0	0	0	1
1	0	0	0	2
0	1	0	0	3
1	1	0	0	4
0	0	1	0	5
1	0	1	0	6
0	1	1	0	7
1	1	1	0	8
0	0	0	1	9
1	0	0	1	10
0	1	0	1	11
1	1	0	1	12
0	0	1	1	13
1	0	1	1	14
0	1	1	1	15
1	1	1	1	16

Table 3 RF and IF synthesizer nominal charge pump currents (gain)

CPI	SINGLE/DOUBLE	I_{CPA} (μA)	I_{CPB} (μA)
0	0	470	470
0	1	840	840
1	0	1410	470
1	1	2480	840

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}, V_{DDX}	digital and crystal reference supply voltages	–0.3	+5.5	V
V_{CCA}, V_{CCB}	analog charge pump supply voltages	–0.3	+5.5	V
$V_C - V_D$	difference in voltage between analog and digital supplies	–0.3	+5.5	V
V_n	voltage			
	at pins 7, 9, 10, 11 and 13	–0.3	V_{DD} + 0.3	V
	at pins 1, 3, and 20	–0.3	V_{DDX} + 0.3	V
	at pins 4 and 6	–0.3	V_{CCB} + 0.3	V
	at pins 15 and 17	–0.3	V_{CCA} + 0.3	V
ΔV_{GND}	difference in voltage between any of DGND, AGND and XGND (these pins should be connected together)	–0.3	+0.3	V
P_{tot}	total power dissipation	–	120	mW
T_{stg}	IC storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature	–30	+85	°C
$T_{j(max)}$	maximum junction temperature	–	150	°C

HANDLING

All pins withstand class 1 ESD test in accordance with *“EIA/JESD22-A114-A”* electrostatic discharge (ESD) sensitivity testing Human Body Model (HBM).

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	in free air	120	K/W

CHARACTERISTICS

All values refer to the typical measurement circuit; T_{amb} = 25 °C; V_{DD} = V_{DDX} = 2.7 to 5.5 V; V_{CCA} = V_{CCB} = 2.7 to 5.5 V; V_{CCA} = V_{CCB} ≥ V_{DD}; unless otherwise specified. Characteristics for which only a typical value is given are not tested.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies; pins 5, 12, 16 and 19						
V_{DD}, V_{DDX}	digital and crystal reference supply voltages	V_{DD} = V_{DDX}; V_{CCA} = V_{CCB} ≥ V_{DD}	2.7	3.0	5.5	V
V_{CCA}, V_{CCB}	charge pump supply voltages	V_{CCA} = V_{CCB} ≥ V_{DD}	2.7	3.0	5.5	V
I_{DD}	synthesizer digital supply current	V_{DD} = 3 V; $\overline{E}$ = 1; ON_A and ON_B = 1	–	1.5	2.1	mA
I_{DDX1}	reference block supply current	V_{DDX} = 3 V; XON = 0	–	0.25	0.4	mA
I_{DDX2}	crystal oscillator and buffer currents	V_{DDX} = 3 V; XON = 1	–	1.5	1.8	mA
I_{CCA}	RF synthesizer charge pump and prescaler supply currents	V_{CCA} = 3 V; ON_A and ON_B = 1	–	8.1	9.8	mA
I_{CCB}	IF synthesizer charge pump and prescaler supply currents	V_{CCB} = 3 V; ON_A and ON_B = 1	–	4.8	5.7	mA
$I_{tot(pd)}$	total supply currents ($I_{CCA(pd)}$ + $I_{DD(pd)}$ + $I_{CCB(pd)}$ + $I_{DDX(pd)}$) in power-down mode	$\overline{E}$ = V_{DD}; CLK and DATA = 0 V or V_{DD}; ON_A and ON_B = 0; XON = 0	–	40	80	µA
RF main divider input; pin 15						
f_{RF}	RF input frequency		300	–	2100	MHz
$V_{RF(rms)}$	AC-coupled input signal level (RMS value)	f_{RF} = 600 to 2100 MHz	35	–	225	mV
		f_{RF} = 300 to 600 MHz	70	–	225	mV
R_m	main divider ratio		512	–	65535	
Z_i	input impedance (real part)	f_{RF} = 2 GHz	–	60	–	Ω
C_i	pin input capacitance		–	2	–	pF
IF main divider input; pin 6						
f_{IF}	IF input frequency	V_{CCA} = V_{CCB} ≤ 4.0 V	50	–	550	MHz
			50	–	400	MHz
$V_{IF(rms)}$	AC-coupled input signal level (RMS value)	f_{IF} = 150 to 550 MHz	35	–	225	mV
		f_{IF} = 100 to 150 MHz	50	–	225	mV
		f_{IF} = 50 to 100 MHz	100	–	225	mV
R_m	main divider ratio		128	–	16383	
Z_i	input impedance (real part)	f_{IF} = 400 MHz	–	60	–	Ω
C_i	pin input capacitance		–	2	–	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Synthesizers reference divider input; pins 1 and 20						
f_{xtal}	crystal reference oscillator frequency		3	–	20	MHz
$V_{xtal(rms)}$	sinusoidal input signal level between pins 1 and 20 (RMS value)	single-ended;				
		f_{xtal} = 6 to 20 MHz	35	–	250	mV
		f_{xtal} = 3 to 6 MHz	70	–	250	mV
		differential;				
		f_{xtal} = 6 to 20 MHz	70	–	500	mV
		f_{xtal} = 3 to 6 MHz	140	–	500	mV
R_{refc}	common reference division ratio		8	–	1023	
R_{refa}	reference subdivider division ratio		1	–	16	
Z_i	input impedance (real part) per pin	f_{xtal} = 10 MHz; XON = 1	–	4	–	kΩ
C_i	typical pin input capacitance		–	2	–	pF
NF	small signal differential input noise figure	matched to a 4 kΩ source; XON = 1	–	4.5	–	dB
Phase detectors						
f_{PCmax}	maximum loop comparison frequency		–	2000	–	kHz
Charge pump outputs; pins 4 and 17						
V_{CPA}	output voltage compliance range; RF synthesizer		0.4	–	V_{CCA} – 0.4	V
V_{CPB}	output voltage compliance range; IF synthesizer		0.4	–	V_{CCB} – 0.4	V
$I_{ocp(err)}$	charge pump output current error	note 1	–25	–	+25	%
I_{match}	sink-to-source current matching		–	±5	–	%
I_{Lcp}	charge pump **off** leakage current	$V_{CPA} = \frac{1}{2}V_{CCA}$; $V_{CPB} = \frac{1}{2}V_{CCB}$	–5	±1	+5	nA
Phase noise						
N_{900}	RF synthesizer's contribution to close-in phase noise of 0.9 GHz VCO signal inside closed-loop bandwidth	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–86	–	dBc/Hz
N_{1800}	RF synthesizer's contribution to close-in phase noise of 1.8 GHz VCO signal inside closed-loop bandwidth	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 200 kHz	–	–80	–	dBc/Hz
N_{180}	IF synthesizer's contribution 180 MHz VCO signal inside closed-loop bandwidth	f_{xtal} = 13 MHz; V_{xtal} = 0 dBm; f_{PC} = 1000 kHz	–	–104	–	dBc/Hz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Interface logic input signal levels; pins 7, 9, 10, 11 and 13						
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	–	V_{DD} + 0.3	V
V_{IL}	LOW-level input voltage		–0.3	–	$0.3V_{DD}$	V
I_{bias}	input bias current	logic 1 or logic 0	–5	–	+5	μA
C_i	input capacitance		–	2	–	pF
Low noise crystal oscillator amplifier output signals; pins 3 and 18						
Z_o	differential output impedance (real part)	f_{xtal} = 10 MHz	–	2	–	kΩ
V_{XOUT}, V_{XOUTN}	DC output voltage		–	2.29	–	V
$G_{v(diff)}$	small signal differential voltage gain	XON = 1; f_{xtal} = 10 MHz	18	20	22	dB
$V_{o(p-p)}$	limiting differential output voltage swing (peak-to-peak value)	XON = 1	–	2	–	V
$\Delta f/f(V_{DDX})$	frequency stability as a function of supply voltage change (referenced to initial frequency)	V_{DDX} = 3 V ±5%; note 2	–	±0.25	–	ppm
System specification						
$FTRF_{IF}$	RF frequency and close harmonics feedthrough to IF frequency	note 3	–	70	–	dBc
$FTIF_{RF}$	IF frequency and close harmonics feedthrough to RF frequency	note 3	–	50	–	dBc

Notes

1. Conditions: $0.4 < V_{CPA} < (V_{CCA} - 0.4)$ and $0.4 < V_{CPB} < (V_{CCB} - 0.4)$.
2. This value is directly dependent on the external resonator quality factor. Only guaranteed for the application circuit which is given in Fig.5.
3. Only guaranteed on the Philips application board.

SERIAL BUS TIMING CHARACTERISTICS

$V_{DD} = V_{DDX} = V_{CCA} = V_{CCB} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	input rise time	–	10	40	ns
t_f	input fall time	–	10	40	ns
T_{cy}	clock period	100	–	–	ns
Enable programming; $\overline{E}$					
t_{START}	delay to rising clock edge	100	–	–	ns
t_{END}	delay from last falling clock edge	20	–	–	ns
$t_{W(min)}$	minimum inactive pulse width	1500(1)	–	–	ns
$t_{SU;\overline{E}}$	enable set-up time to next clock edge	20	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	input data to clock set-up time	20	–	–	ns
$t_{HD;DAT}$	input data to clock hold time	20	–	–	ns

Note

1. The minimum pulse width ($t_{W(min)}$) can be smaller than 1.5 µs when the following conditions are fulfilled:

   a) Main divider input frequency $f_{RF} > \frac{383}{t_{W(min)}}$

   b) Reference divider input frequency $f_{xtal} > \frac{3}{t_{W(min)}}$

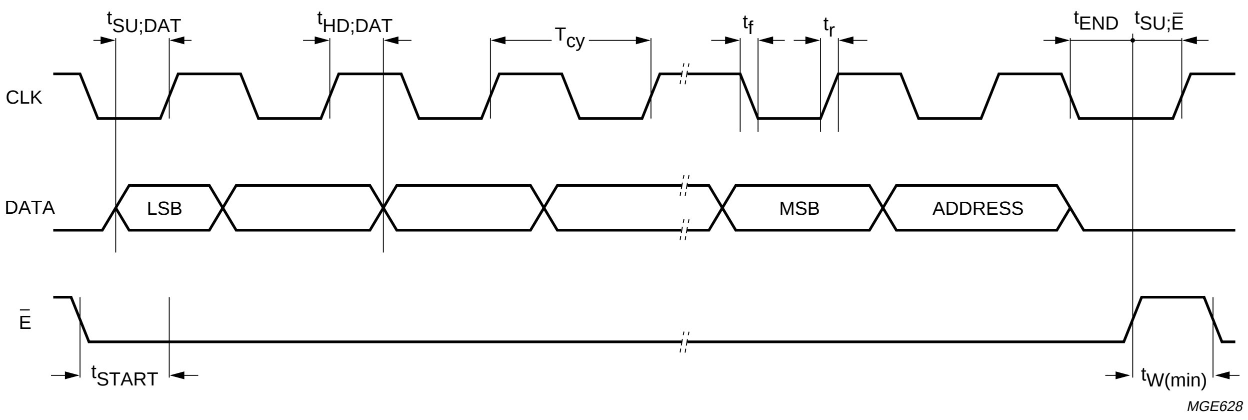


Fig.3 Serial bus timing diagram.

AC TIMING CHARACTERISTICS

$V_{DD} = V_{DDX} = V_{CCA} = V_{CCB} = 3$ V; $T_{amb} = 25$ °C; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{PUP}	delay for initial power-up	–	400	–	µs
t_{PDWN}	time for power-down from $\overline{E} = 0$ ($ON_A/ON_B = 0$)	–	100	–	µs
t_{START}	time to turn-on either the RF or IF synthesizer from ON_A/ON_B	–	50	–	µs
t_{END}	time to turn-off either the RF or IF synthesizer from ON_A/ON_B	–	70	–	µs
t_{SEND}	waiting time before sending data on the serial bus	15000	–	–	µs

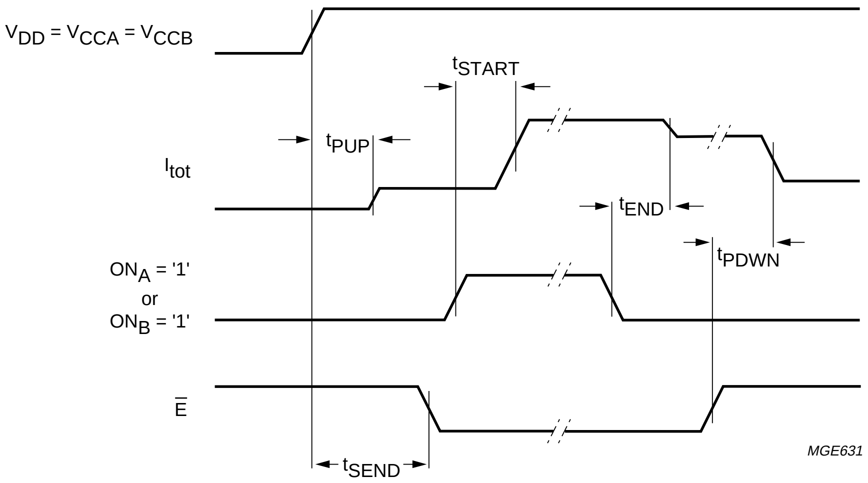
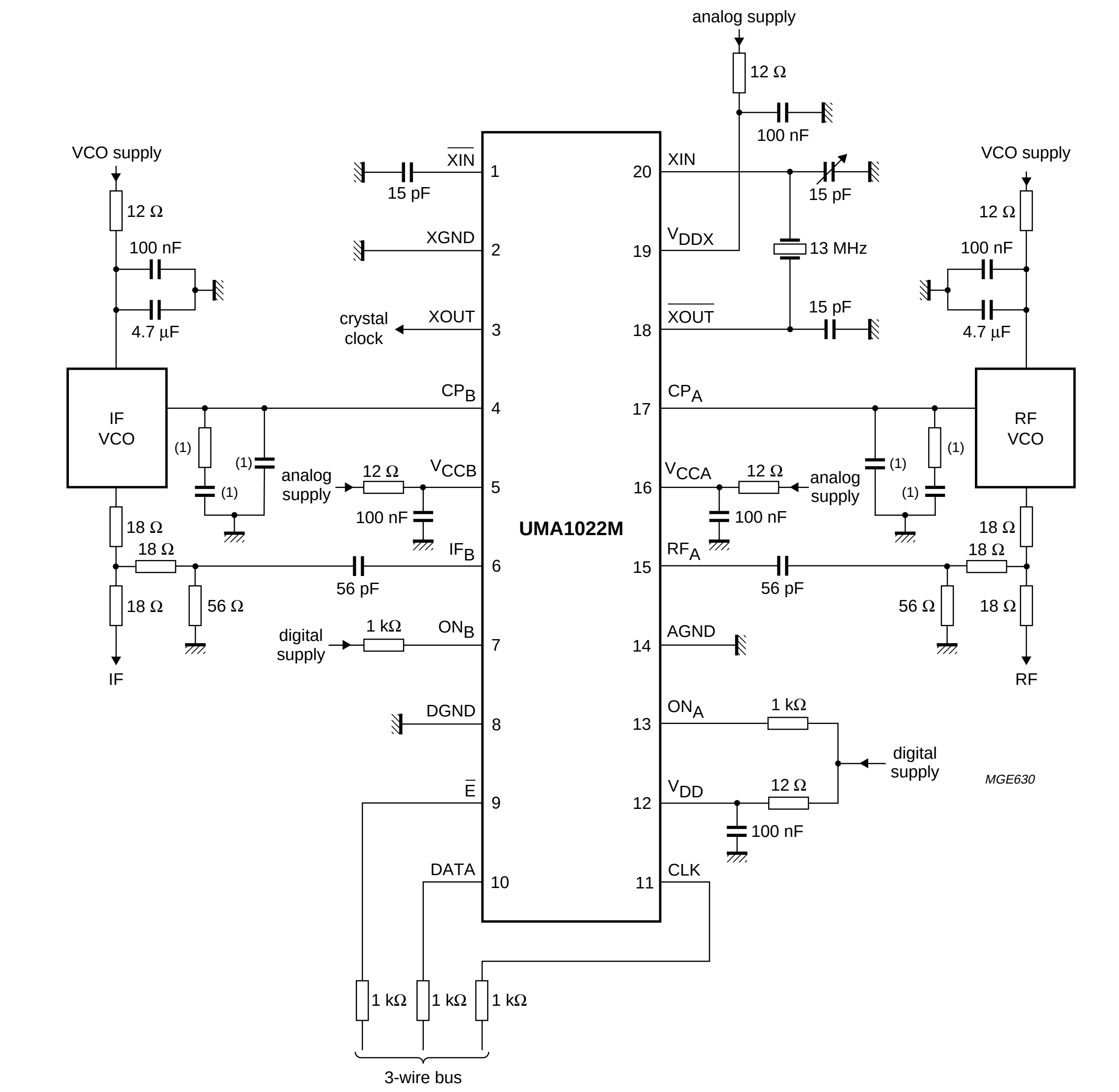


Fig.4 AC timing characteristics.

APPLICATION INFORMATION



(1) Loop filter values depend on the application.

Fig.5 Typical test and application diagram.

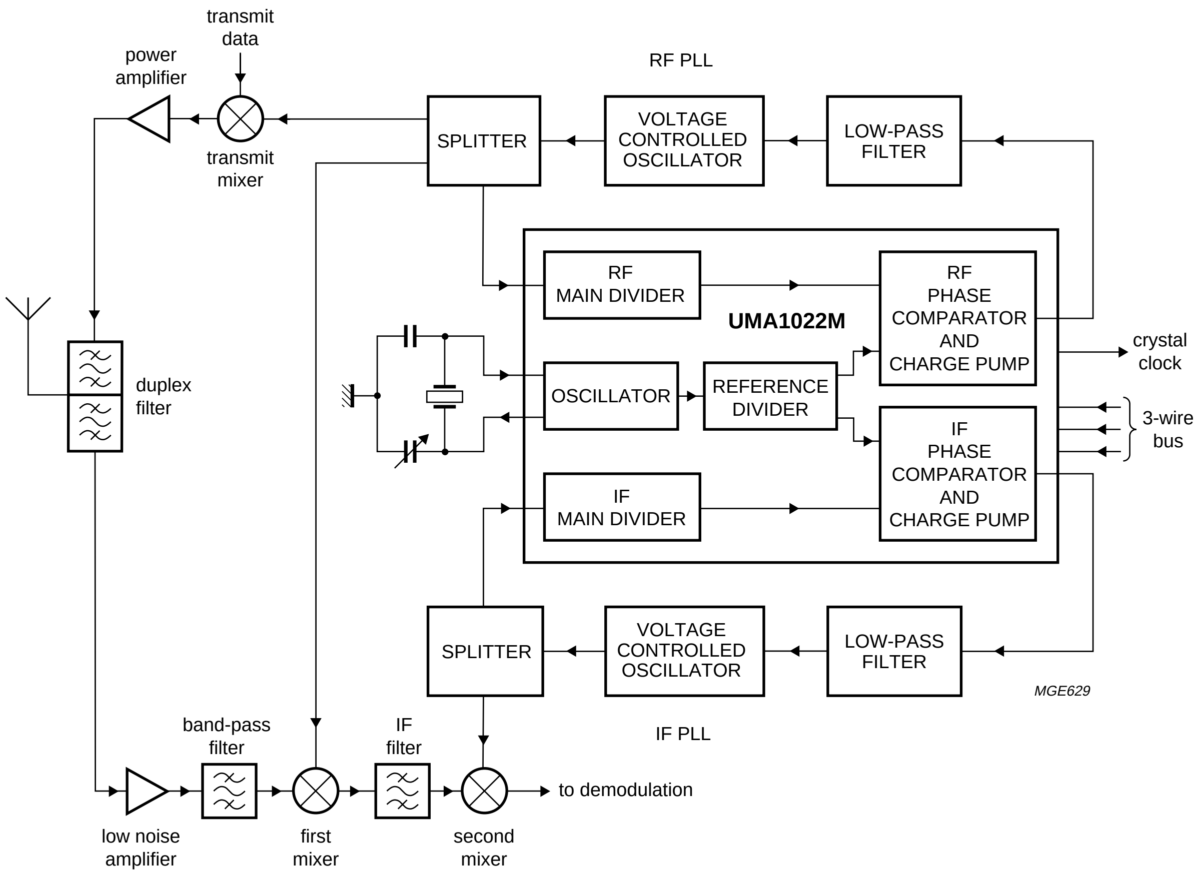
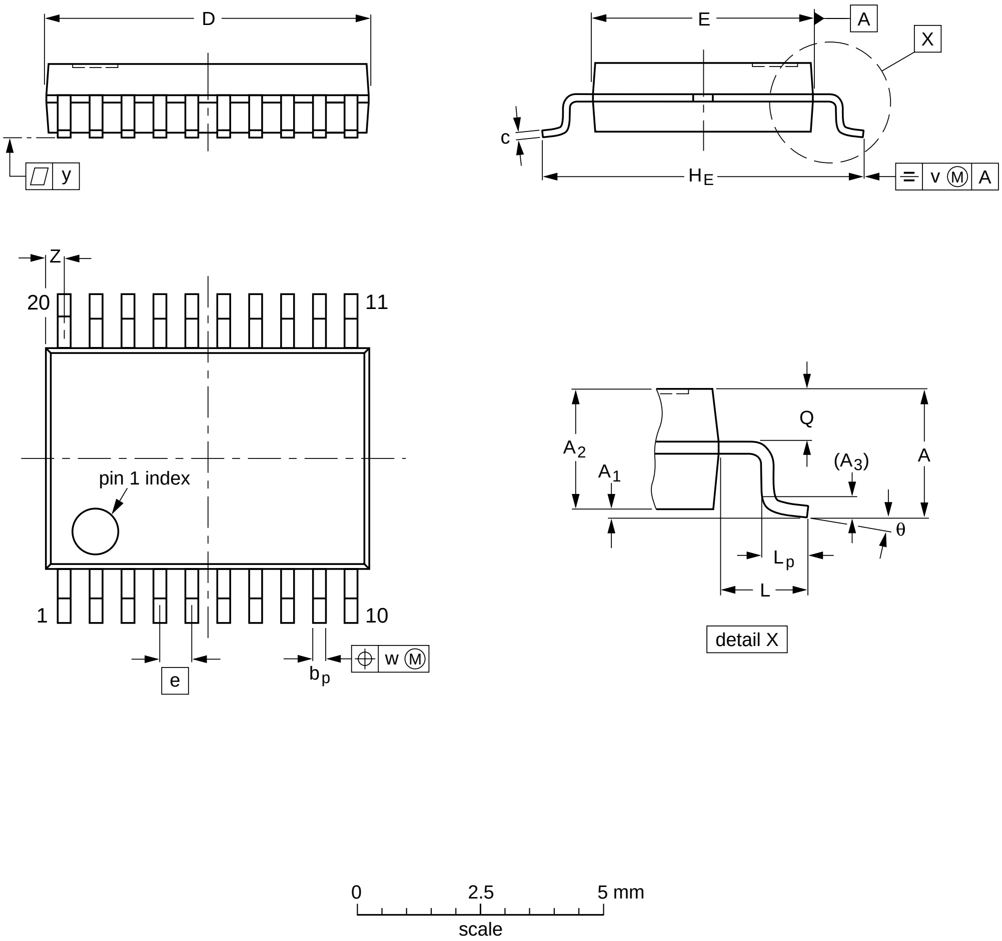


Fig.6 Application block diagram.

PACKAGE OUTLINE

SSOP20: plastic shrink small outline package; 20 leads; body width 4.4 mm **SOT266-1**

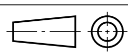


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0	1.4 1.2	0.25	0.32 0.20	0.20 0.13	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES					EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ				
SOT266-1							~~90-04-05~~ 95-02-25

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, SQFP	not suitable	suitable
HLQFP, HSQFP, HSOP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *“Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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