

TrenchMOS™ transistor Logic level FET

BUK9614-55

GENERAL DESCRIPTION

N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

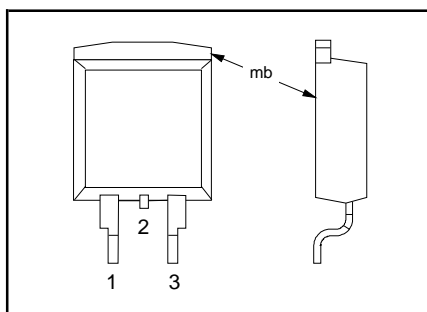
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	68	A
P_{tot}	Total power dissipation	142	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 5 V$	14	mΩ

PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20 k\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	$T_{mb} = 25\text{ °C}$	-	68	A
I_D	Drain current (DC)	$T_{mb} = 100\text{ °C}$	-	48	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\text{ °C}$	-	240	A
P_{tot}	Total power dissipation	$T_{mb} = 25\text{ °C}$	-	142	W
T_{stg}, T_j	Storage & operating temperature	-	-55	175	°C

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage	Human body model (100 pF, 1.5 kΩ)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	1.05	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

TrenchMOS™ transistor

Logic level FET

BUK9614-55

STATIC CHARACTERISTICS

T_j = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	Drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.25 mA; T _j = -55°C	55 50	- -	- -	V V
V _{GS(TO)}	Gate threshold voltage	V _{DS} = V _{GS} ; I _D = 1 mA T _j = 175°C T _j = -55°C	1.0 0.5 -	1.5 - -	2.0 - 2.3	V V V
I _{DSS}	Zero gate voltage drain current	V _{DS} = 55 V; V _{GS} = 0 V; T _j = 175°C	-	0.05	10	μA
I _{GSS}	Gate source leakage current	V _{GS} = ±5 V; V _{DS} = 0 V T _j = 175°C	-	0.02	500	μA
±V _{(BR)GSS}	Gate-source breakdown voltage	I _G = ±1 mA; T _j = 175°C	10	-	10	μA V
R _{DS(ON)}	Drain-source on-state resistance	V _{GS} = 5 V; I _D = 25 A T _j = 175°C	- -	12 -	14 30	mΩ mΩ

DYNAMIC CHARACTERISTICS

T_{mb} = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g _{fs}	Forward transconductance	V _{DS} = 25 V; I _D = 25 A	30	65	-	S
C _{iss}	Input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz	-	2900	3800	pF
C _{oss}	Output capacitance		-	500	600	pF
C _{riss}	Feedback capacitance		-	240	330	pF
t _{d on}	Turn-on delay time	V _{DD} = 30 V; I _D = 25 A; V _{GS} = 5 V; R _G = 10 Ω	-	35	50	ns
t _r	Turn-on rise time		-	95	145	ns
t _{d off}	Turn-off delay time		-	130	180	ns
t _f	Turn-off fall time		-	60	80	ns
L _d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L _s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25°C unless otherwise specified

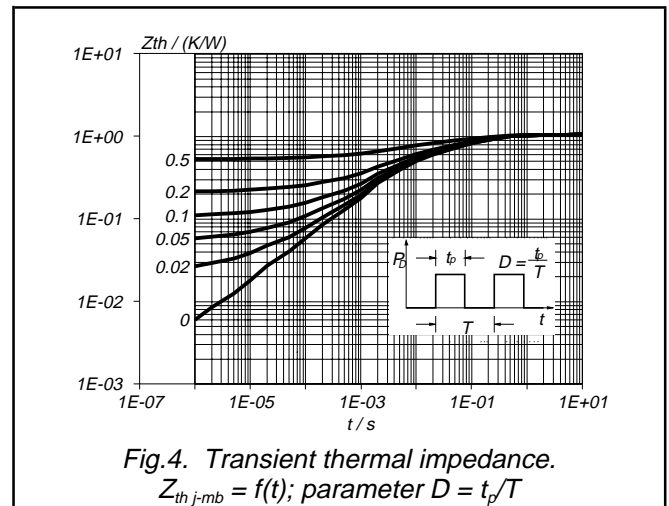
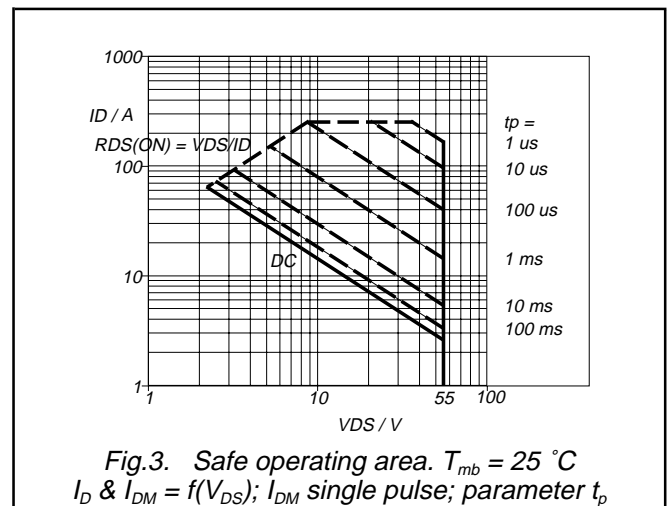
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I _{DR}	Continuous reverse drain current		-	-	68	A
I _{DRM}	Pulsed reverse drain current		-	-	240	A
V _{SD}	Diode forward voltage	I _F = 25 A; V _{GS} = 0 V	-	0.95	1.2	V
		I _F = 65 A; V _{GS} = 0 V	-	1.0	-	V
t _{rr}	Reverse recovery time	I _F = 65 A; -dI _F /dt = 100 A/μs;	-	57	-	ns
Q _{rr}	Reverse recovery charge	V _{GS} = -10 V; V _R = 30 V	-	0.14	-	μC

TrenchMOS™ transistor
Logic level FET

BUK9614-55

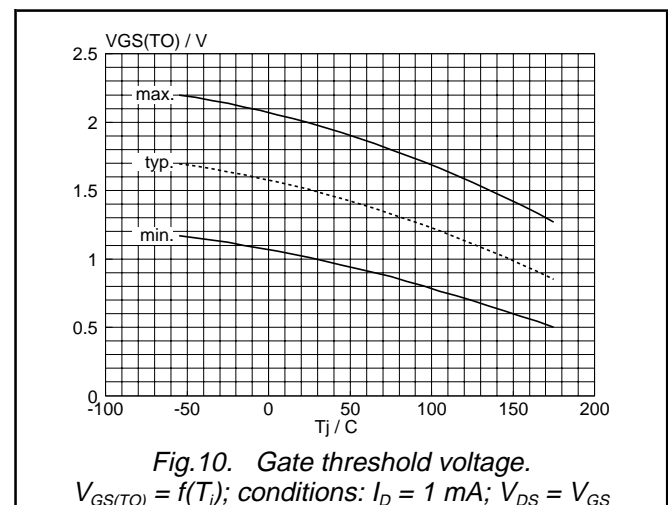
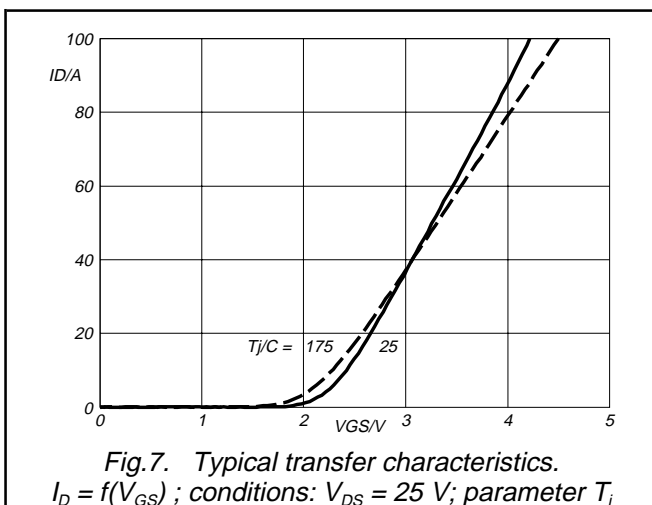
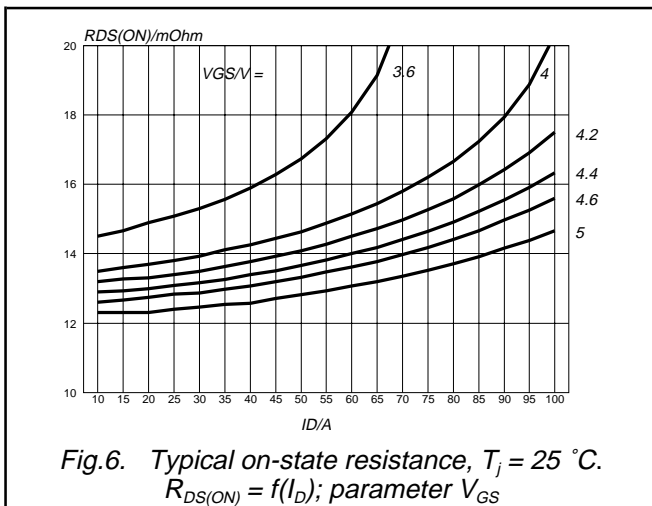
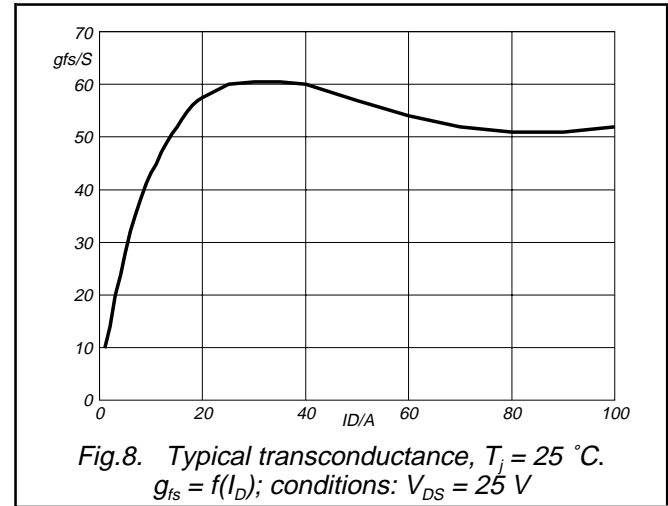
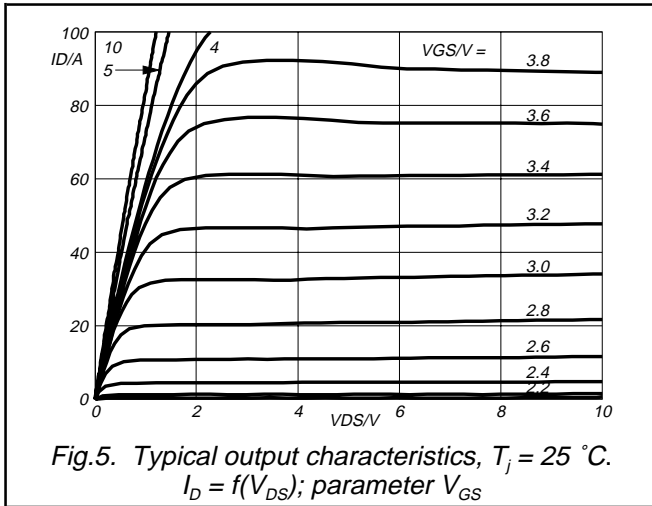
AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 65 \text{ A}; V_{DD} \leq 25 \text{ V}; V_{GS} = 5 \text{ V}; R_{GS} = 50 \Omega; T_{mb} = 25 \text{ }^\circ\text{C}$	-	-	200	mJ



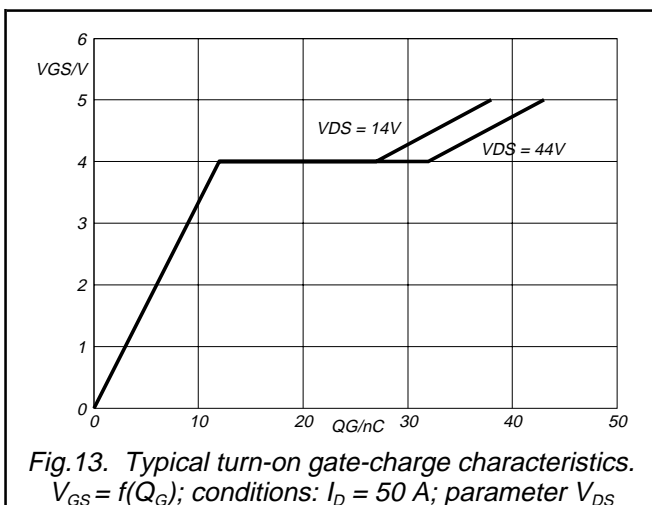
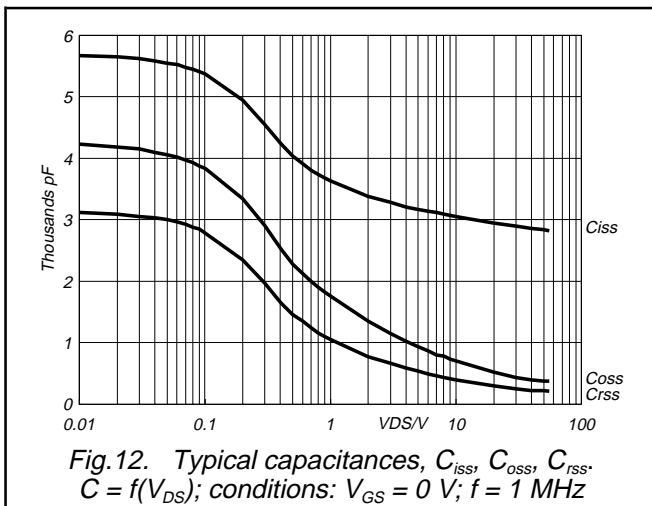
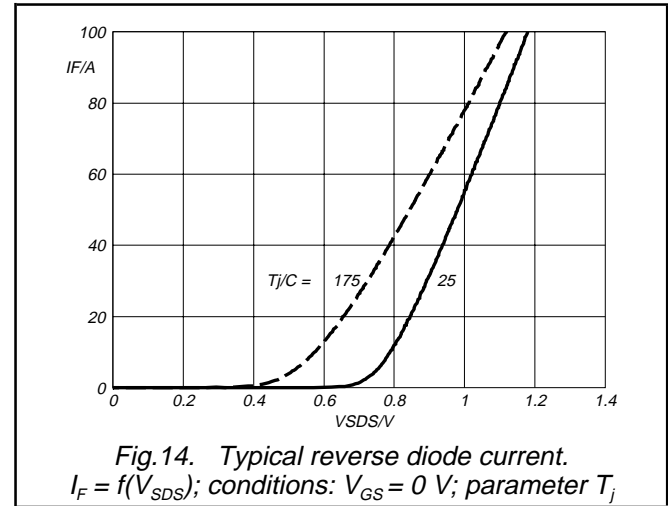
TrenchMOS™ transistor
Logic level FET

BUK9614-55



TrenchMOS™ transistor
Logic level FET

BUK9614-55



TrenchMOS™ transistor
Logic level FET

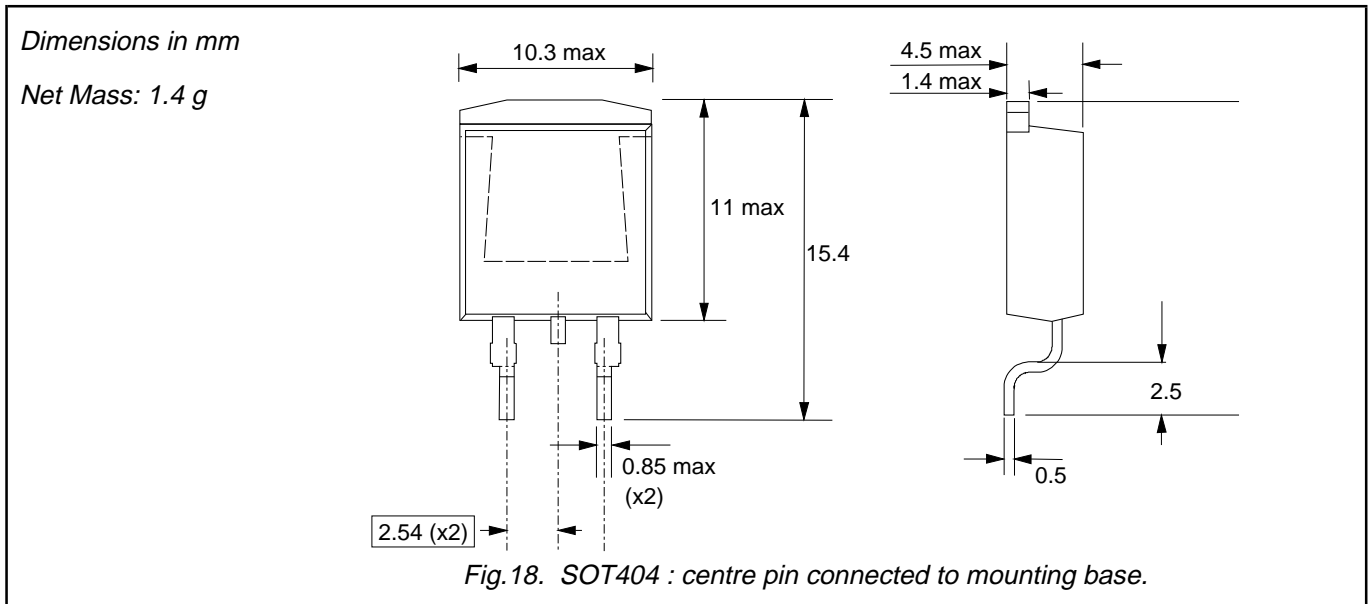
BUK9614-55



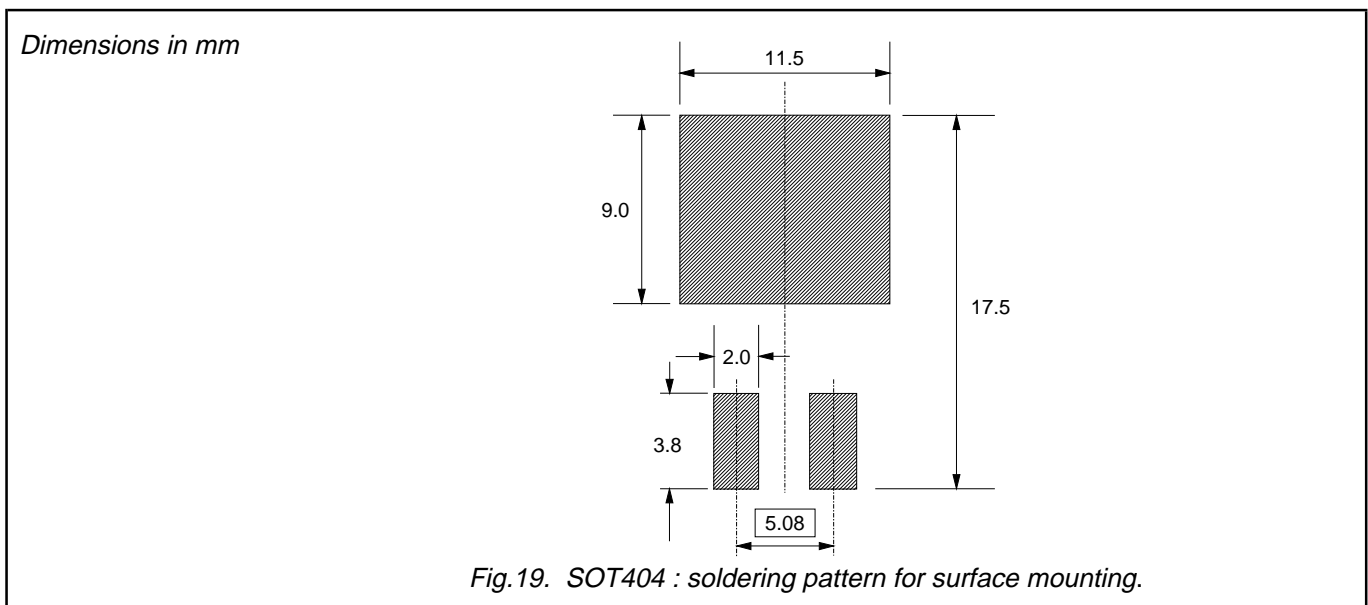
TrenchMOS™ transistor
Logic level FET

BUK9614-55

MECHANICAL DATA



MOUNTING INSTRUCTIONS



Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

TrenchMOS™ transistor

Logic level FET

BUK9614-55

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
© Philips Electronics N.V. 1998	
All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.	
The information presented in this document does not form part of any quotation or contract, it is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent or other industrial or intellectual property rights.	

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.