

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT243

Quad bus transceiver; 3-state

Product specification
File under Integrated Circuits, IC06

December 1990

Quad bus transceiver; 3-state

74HC/HCT243

FEATURES

- Non-inverting 3-state outputs
- 2-way asynchronous data bus communication
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT243 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT243 are quad bus transceivers featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

They are designed for 4-line asynchronous 2-way data communications between data buses.

The output enable inputs (\overline{OE}_A and OE_B) can be used to isolate the buses.

The "243" is similar to the "242" but has non-inverting (true) outputs.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n	C _L = 15 pF; V _{CC} = 5 V	6	11	ns
C _I	input capacitance		3.5	3.5	pF
C _{I/O}	input/output capacitance		10	10	pF
C _{PD}	power dissipation capacitance per transceiver	notes 1 and 2	26	34	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

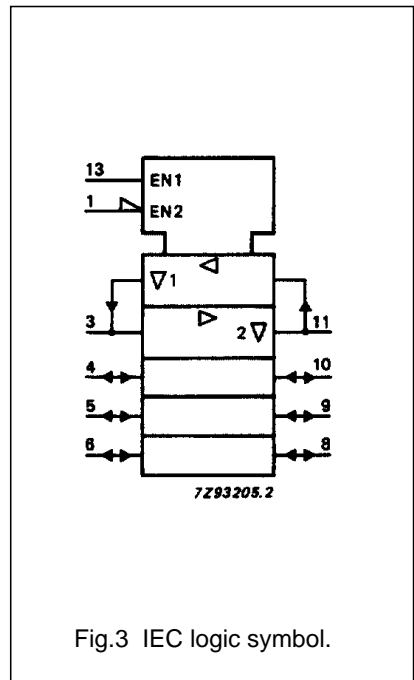
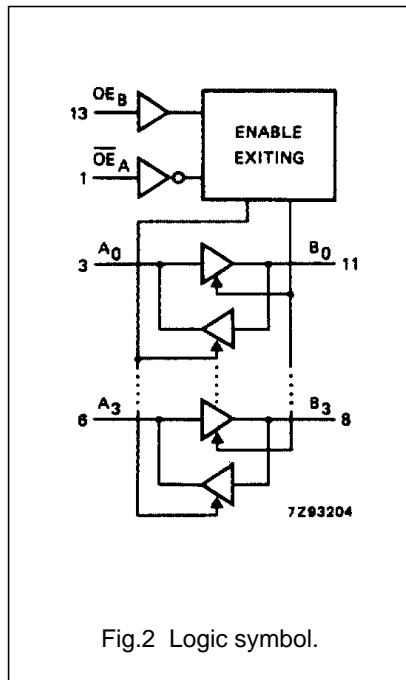
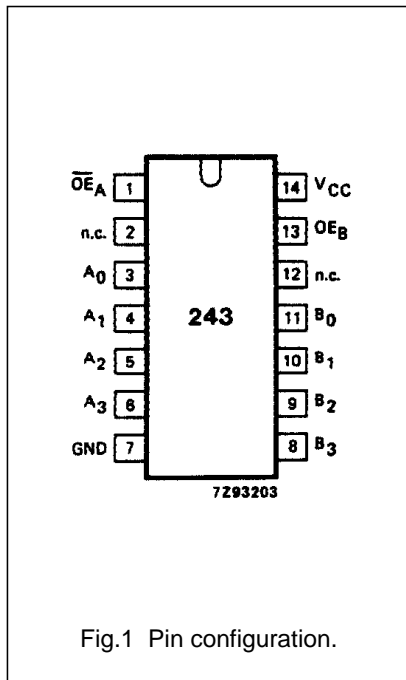
See "74HC/HCT/HCU/HCMOS Logic Package Information".

Quad bus transceiver; 3-state

74HC/HCT243

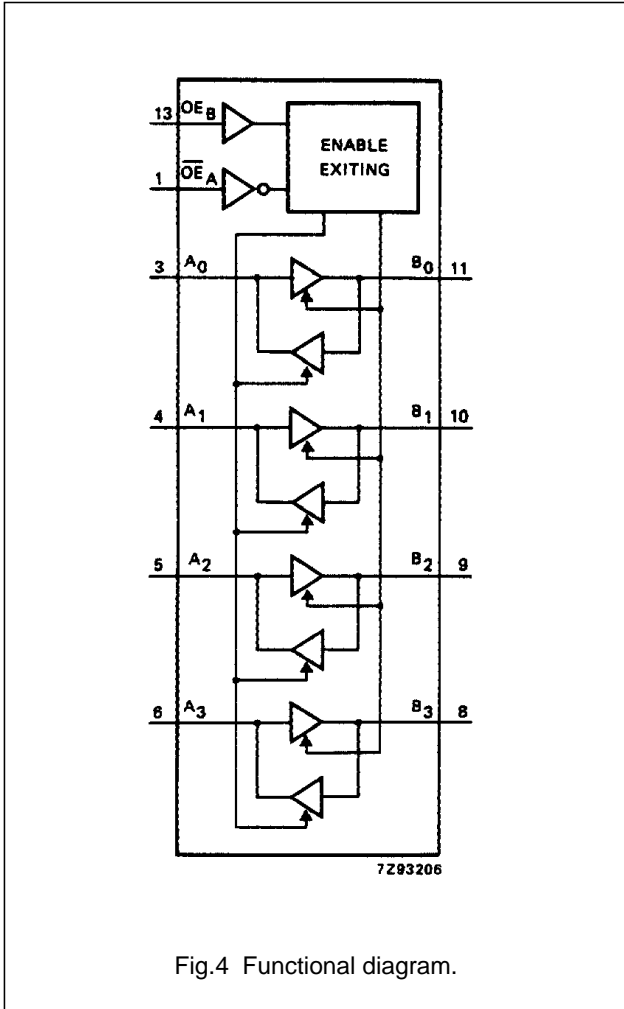
PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	\overline{OE}_A	output enable input (active LOW)
2, 12	n.c.	not corrected
3, 4, 5, 6	A ₀ to A ₃	data inputs/outputs
7	GND	ground (0 V)
11, 10, 9, 8	B ₀ to B ₃	data inputs/outputs
13	OE_B	output enable input
14	V _{CC}	positive supply voltage



Quad bus transceiver; 3-state

74HC/HCT243



FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
\overline{OE}_A	OE_B	A_n	B_n
L	L	inputs	$B = A$
H	L	Z	Z
L	H	Z	Z
H	H	$A = B$	inputs

Notes

1. H = HIGH voltage level
 L = LOW voltage level
 Z = high impedance OFF-state

Quad bus transceiver; 3-state

74HC/HCT243

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		22 8 6	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.5
t _{PZH} / t _{PZL}	3-state output enable time OE _A to A _n or B _n ; OE _B to A _n or B _n		50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Figs 6 and 7
t _{PHZ} / t _{PLZ}	3-state output disable time OE _A to A _n or B _n ; OE _B to A _n or B _n		61 22 18	165 33 28		205 41 35		250 50 43	ns	2.0 4.5 6.0	Figs 6 and 7
t _{THL} / t _{TLH}	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5

Quad bus transceiver; 3-state

74HC/HCT243

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	1.10
B _n	1.10
\overline{OE}_A	1.00
\overline{OE}_B	1.00

AC CHARACTERISTICS FOR 74HCT

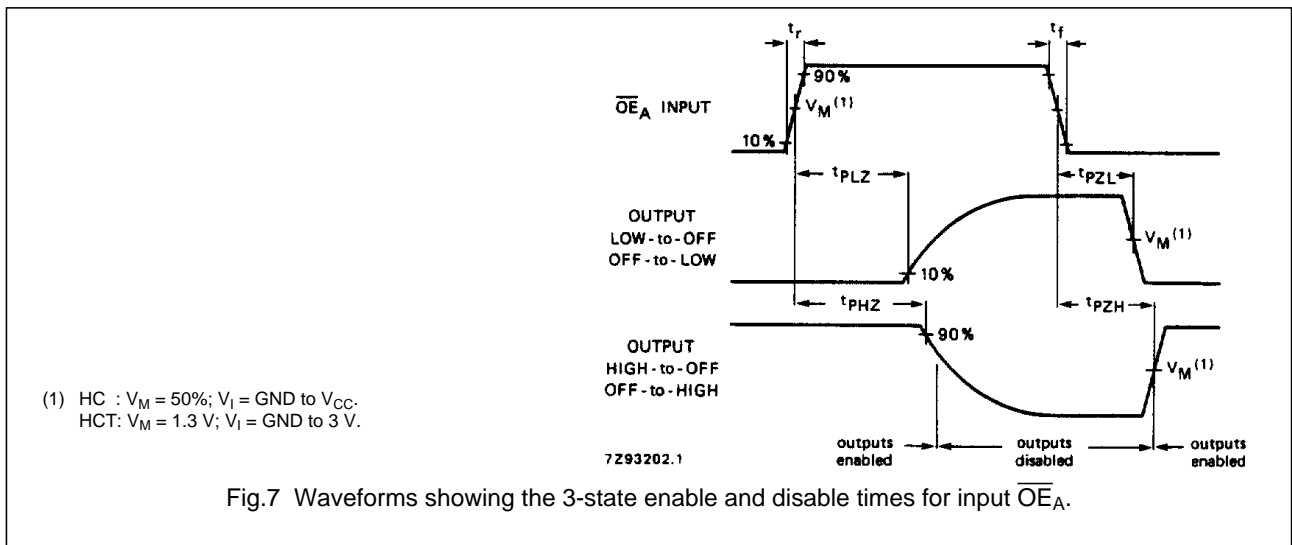
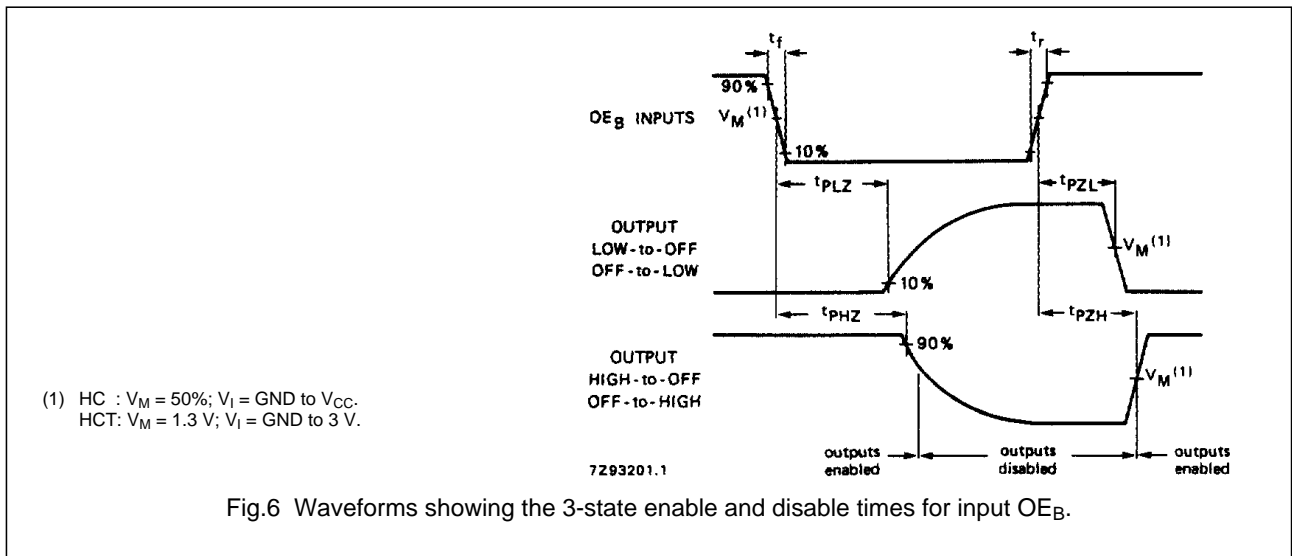
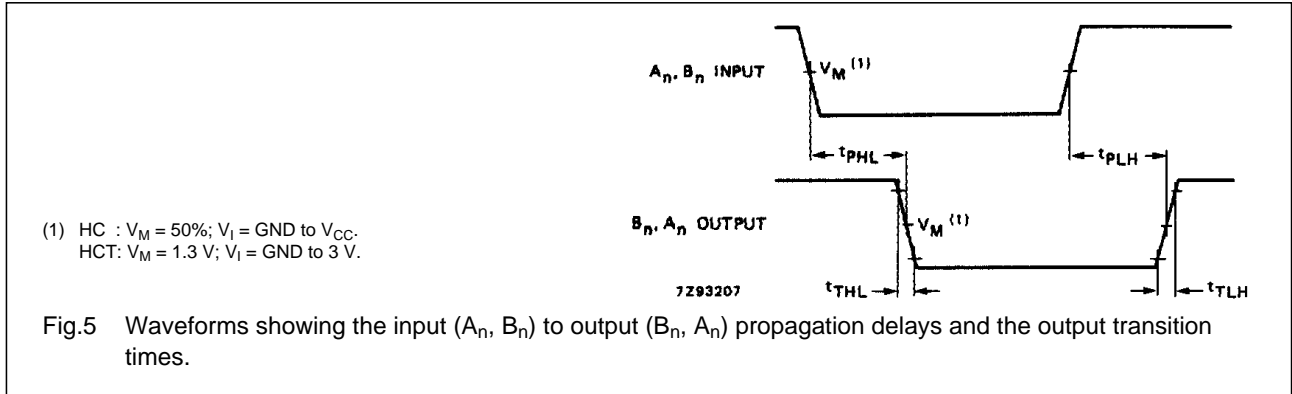
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} (V)	WAVEFORMS
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay A _n to B _n ; B _n to A _n		13	22		28		33	ns	4.5	Fig.5	
t _{PZH} / t _{PZL}	3-state output enable time \overline{OE}_A to A _n or B _n ; \overline{OE}_B to A _n or B _n		18	34		43		51	ns	4.5	Figs 6 and 7	
t _{PHZ} / t _{PLZ}	3-state output disable time \overline{OE}_A to A _n or B _n ; \overline{OE}_B to A _n or B _n		23	35		44		53	ns	4.5	Figs 6 and 7	
t _{THL} / t _{TLH}	output transition time		5	12		15		18	ns	4.5	Fig.5	

Quad bus transceiver; 3-state

74HC/HCT243

AC WAVEFORMS



Quad bus transceiver; 3-state

74HC/HCT243

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.