DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT283

4-bit binary full adder with fast carry

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

4-bit binary full adder with fast carry 74HC/HCT283

FEATURES

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT283 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT283 add two 4-bit binary words (A_n plus B_n) plus the incoming carry. The binary sum appears on the sum outputs (Σ_1 to Σ_4) and the out-going carry (C_{OUT}) according to the equation:

$C_{IN} + (A_1 + B_1) + 2(A_2 + B_2) + +4(A_3 + B_3) + 8(A_4 + B_4) =$
$= \Sigma_1 + 2\Sigma_2 + 4\Sigma_3 + 8\Sigma_4 + 16C_{OUT}$

Where (+) = plus.

Due to the symmetry of the binary add function, the “283” can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic); see function table. In case of all active LOW operands the results Σ_1 to Σ_4 and C_{OUT} should be interpreted also as active LOW. With active HIGH inputs, C_{IN} must be held LOW when no “carry in” is intended. Interchanging inputs of equal weight does not affect the operation, thus C_{IN}, A_1, B_1 can be assigned arbitrarily to pins 5, 6, 7, etc.

See the “583” for the BCD version.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	C_{IN} to Σ_1		16	15	ns
	C_{IN} to Σ_2		18	21	ns
	C_{IN} to Σ_3		20	23	ns
	C_{IN} to Σ_4		23	27	ns
	A_n or B_n to Σ_n		21	25	ns
	C_{IN} to C_{OUT}		20	23	ns
	A_n or B_n to C_{OUT}		20	24	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	88	92	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

See *"74HC/HCT/HCU/HCMOS Logic Package Information"*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4, 1, 13, 10	Σ_1 to Σ_4	sum outputs
5, 3, 14, 12	A_1 to A_4	A operand inputs
6, 2, 15, 11	B_1 to B_4	B operand inputs
7	C_{IN}	carry input
8	GND	ground (0 V)
9	C_{OUT}	carry output
16	V_{CC}	positive supply voltage

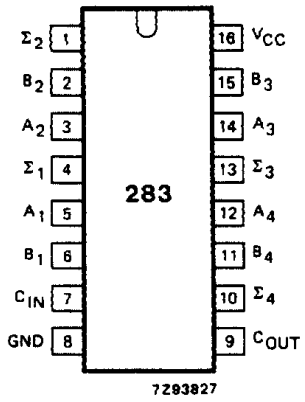

Fig.1 Pin configuration.

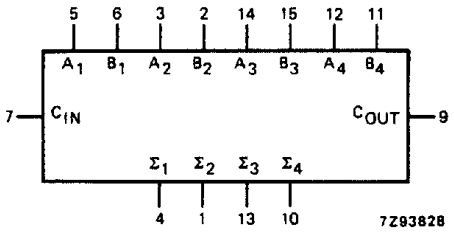

Fig.2 Logic symbol.

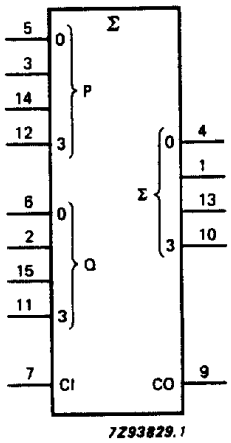

Fig.3 IEC logic symbol.

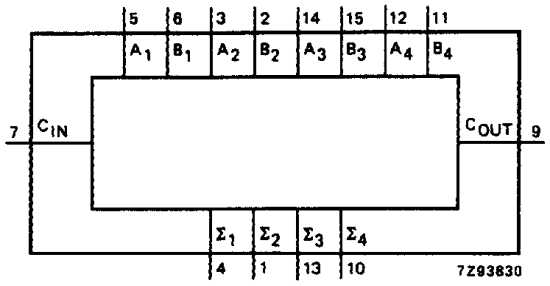

Fig.4 Functional diagram.

FUNCTION TABLE

PINS	C_{IN}	A_1	A_2	A_3	A_4	B_1	B_2	B_3	B_4	Σ_1	Σ_2	Σ_3	Σ_4	C_{OUT}	**EXAMPLE**(2)
logic levels	L	L	H	L	H	H	L	L	H	H	H	L	L	H	
active HIGH	0	0	1	0	1	1	0	0	1	1	1	0	0	1	(3)
active LOW	1	1	0	1	0	0	1	1	0	0	0	1	1	0	(4)

Note

1. H = HIGH voltage level
   L = LOW voltage level
2. **example**

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 1001
 1010
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10011
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3. for active HIGH, example = (9 + 10 = 19)
4. for active LOW, example = (carry + 6 + 5 = 12)

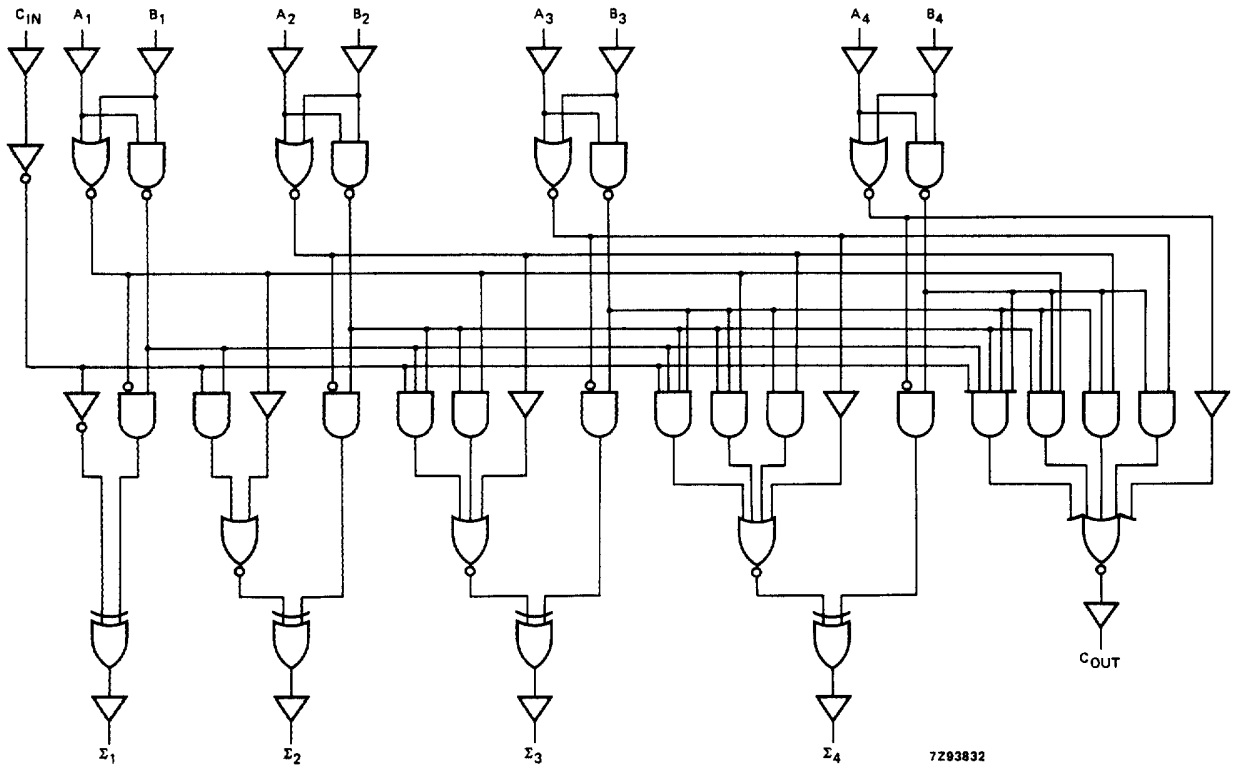


Fig.5 Logic diagram.

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_1		52 19 15	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_2		58 21 17	180 36 31		225 45 38		270 54 46	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_3		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_4		74 27 22	230 46 39		290 58 49		345 69 59	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_n		69 25 20	210 42 36		265 53 45		315 63 54	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to C_{OUT}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to C_{OUT}		63 23 18	195 39 33		245 49 42		295 59 50	ns	2.0 4.5 6.0	Fig.6
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

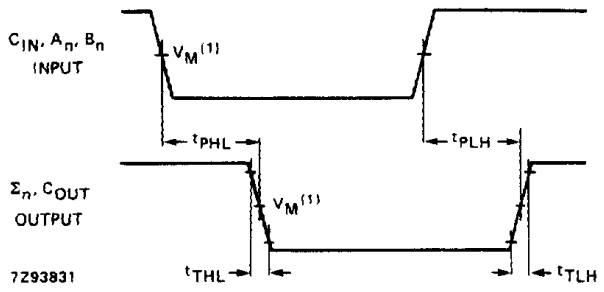
INPUT	UNIT LOAD COEFFICIENT
C_{IN}	1.50
B_2, A_2, A_1	1.00
B_1	0.40
B_4, A_4, A_3, B_3	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			–40 to +85		–40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_1		18	31		39		47	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_2		25	43		54		65	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_3		27	46		58		69	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to Σ_4		31	53		66		80	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to Σ_n		29	49		61		74	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay C_{IN} to C_{OUT}		27	46		58		69	ns	4.5	Fig.6
t_{PHL}/ t_{PLH}	propagation delay A_n or B_n to C_{OUT}		28	48		60		72	ns	4.5	Fig.6
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.6 Waveforms showing the inputs (C_{IN}, A_n, B_n) to the outputs (Σ_n, C_{OUT}) propagation delays and the output transition times.

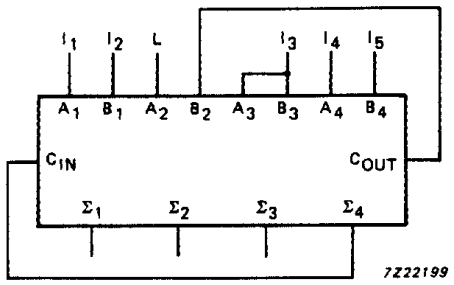


Fig.9 5-input encoder.

Notes to Figs 7 to 10

Figure 7 shows a 3-bit adder using the “283”. Tying the operand inputs of the fourth adder (A_3, B_3) LOW makes Σ_3 dependent on, and equal to, the carry from the third adder. Based on the same principle, Figure 8 shows a method of dividing the “283” into a 2-bit and 1-bit adder. The third stage adder (A_2, B_2, Σ_2) is used simply as means of transferring the carry into the fourth stage (via A_2 and B_2) and transferring the carry from the second stage on Σ_2. Note that as long as long as A_2 and B_2 are the same, HIGH or LOW, they do not influence Σ_2. Similarly, when A_2 and B_2 are the same, the carry into the third stage does not influence the carry out of the third stage. Figure 9 shows a method of implementing a 5-input encoder, where the inputs are equally weighted. The outputs Σ_0, Σ_1 and Σ_2 produce a binary number equal to the number inputs (I_1 to I_5) that are HIGH. Figure 10 shows a method of implementing a 5-input majority gate. When three or more inputs (I_1 to I_5) are HIGH, the output M_5 is HIGH.

APPLICATION INFORMATION

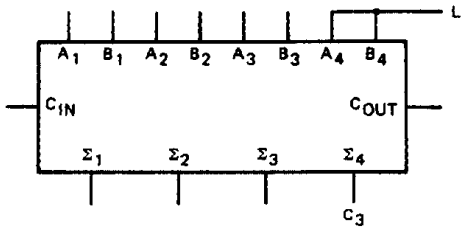


Fig.7 3-bit adder.

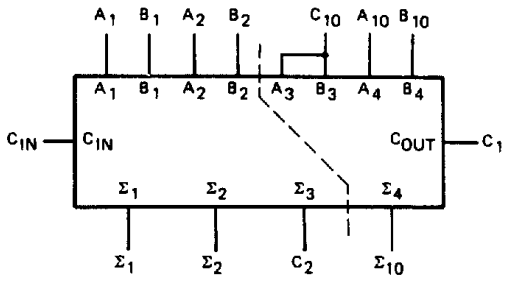


Fig.8 2-bit and 1-bit adder.

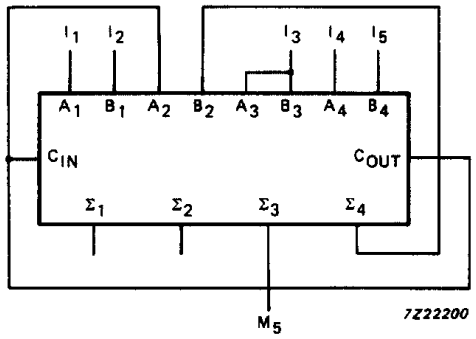


Fig.10 5-input majority gate.

PACKAGE OUTLINES

See *“74HC/HCT/HCU/HCMOS Logic Package Outlines”*.