

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT377

Octal D-type flip-flop with data enable; positive-edge trigger

Product specification  
File under Integrated Circuits, IC06

December 1990

# Octal D-type flip-flop with data enable; positive-edge trigger

## 74HC/HCT377

### FEATURES

- Ideal for addressable register applications
- Data enable for address and data synchronization applications
- Eight positive-edge triggered D-type flip-flops
- See “273” for master reset version
- See “373” for transparent latch version
- See “374” for 3-state version
- Output capability: standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT377 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT377 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. A common clock (CP) input loads all flip-flops simultaneously when the data enable ( $\bar{E}$ ) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q<sub>n</sub>) of the flip-flop.

The  $\bar{E}$  input must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	13	14	ns
f <sub>max</sub>	maximum clock frequency		77	53	MHz
C <sub>I</sub>	input capacitance		3.5	3.5	pF
C <sub>PD</sub>	power dissipation capacitance per flip-flop	notes 1 and 2	20	20	pF

### Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

2. For HC the condition is V<sub>I</sub> = GND to V<sub>CC</sub>  
For HCT the condition is V<sub>I</sub> = GND to V<sub>CC</sub> – 1.5 V

### ORDERING INFORMATION

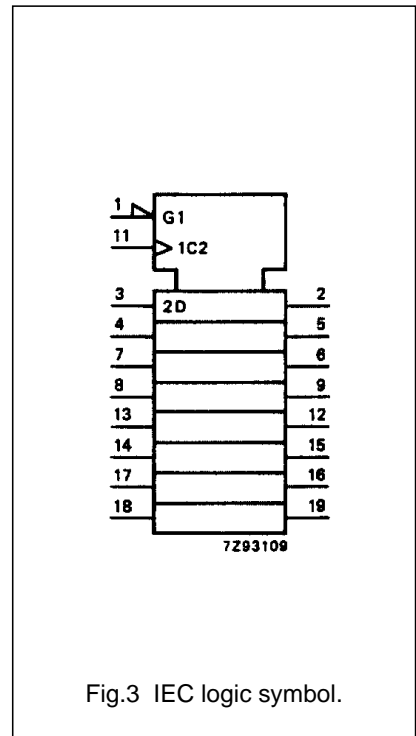
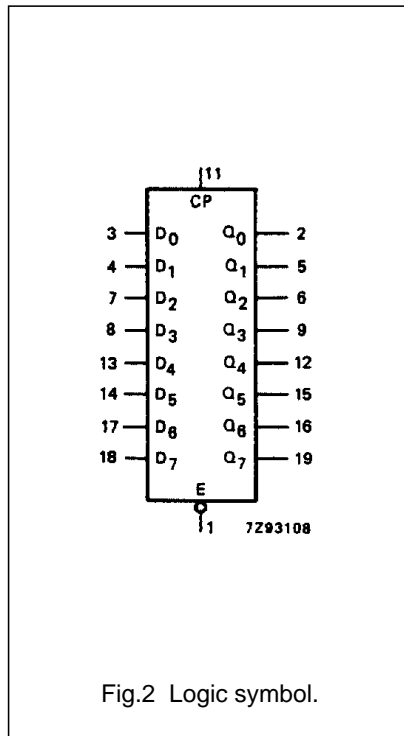
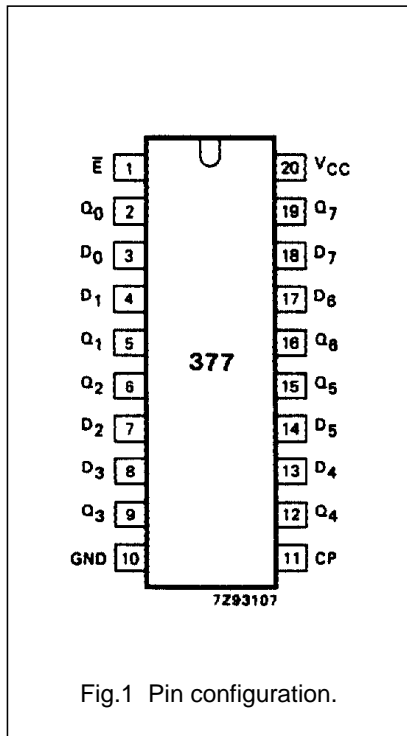
See “74HC/HCT/HCU/HCMOS Logic Package Information”.

Octal D-type flip-flop with data enable;  
positive-edge trigger

74HC/HCT377

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\bar{E}$	data enable input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q <sub>0</sub> to Q <sub>7</sub>	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D <sub>0</sub> to D <sub>7</sub>	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V <sub>CC</sub>	positive supply voltage



Octal D-type flip-flop with data enable;  
positive-edge trigger

74HC/HCT377

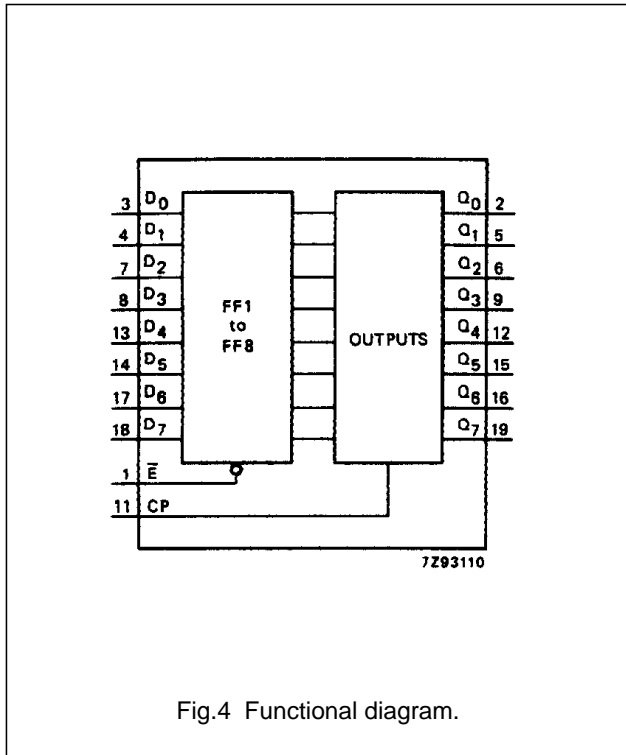


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	CP	$\bar{E}$	$D_n$	$Q_n$
load "1"	↑	l	h	H
load "0"	↑	l	l	L
hold (do nothing)	↑	h	X	no change
	X	H	X	no change

Notes

- H = HIGH voltage level  
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 L = LOW voltage level  
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition  
 ↑ = LOW-to-HIGH CP transition  
 X = don't care

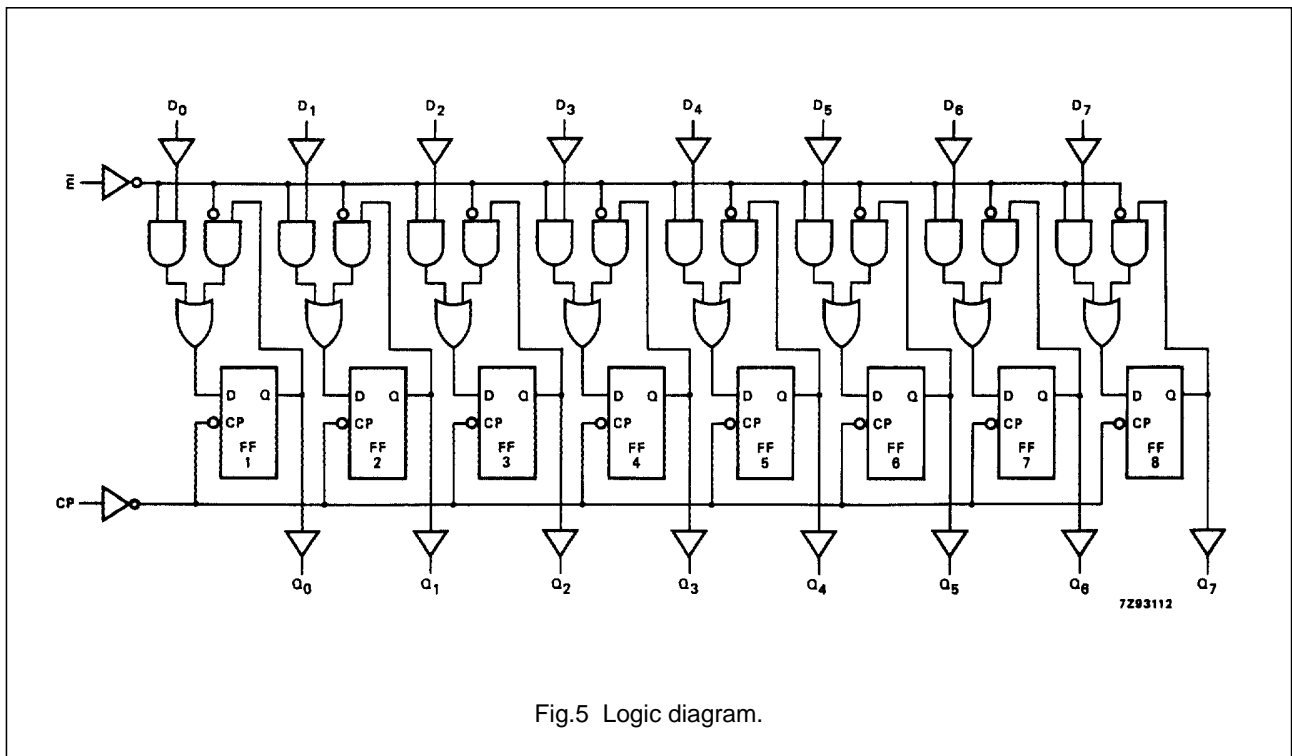


Fig.5 Logic diagram.

# Octal D-type flip-flop with data enable; positive-edge trigger

74HC/HCT377

## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		44 16 13	160 32 27		200 40 34		240 48 41	ns	2.0 4.5 6.0	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10	14 5 4		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t <sub>su</sub>	set-up time $\bar{E}$ to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.7
t <sub>h</sub>	hold time D <sub>n</sub> to CP	3 3 3	-8 -3 -2		3 3 3		3 3 3		ns	2.0 4.5 6.0	Fig.7
t <sub>h</sub>	hold time $\bar{E}$ to CP	4 4 4	-3 -1 -1		4 4 4		4 4 4		ns	2.0 4.5 6.0	Fig.7
f <sub>max</sub>	maximum clock pulse frequency	6 30 35	23 70 83		5 24 28		4 20 24		MHz	2.0 4.5 6.0	Fig.6

# Octal D-type flip-flop with data enable; positive-edge trigger

74HC/HCT377

## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\bar{E}$	1.50
CP	0.50
D <sub>n</sub>	0.20

## AC CHARACTERISTICS FOR 74HCT

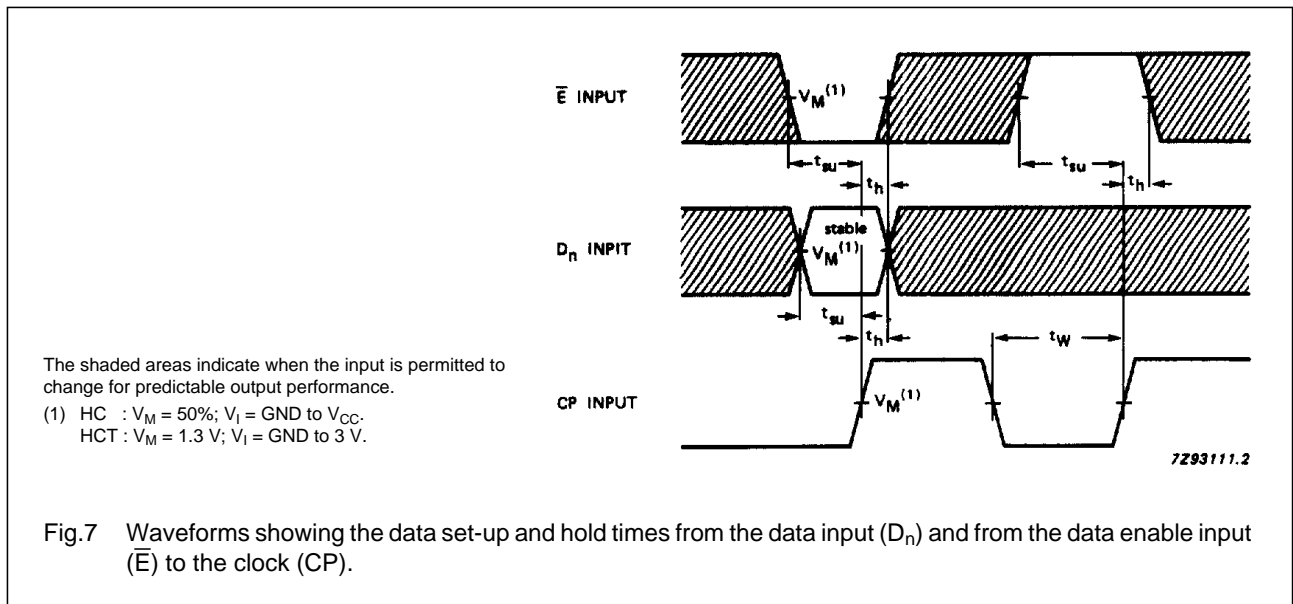
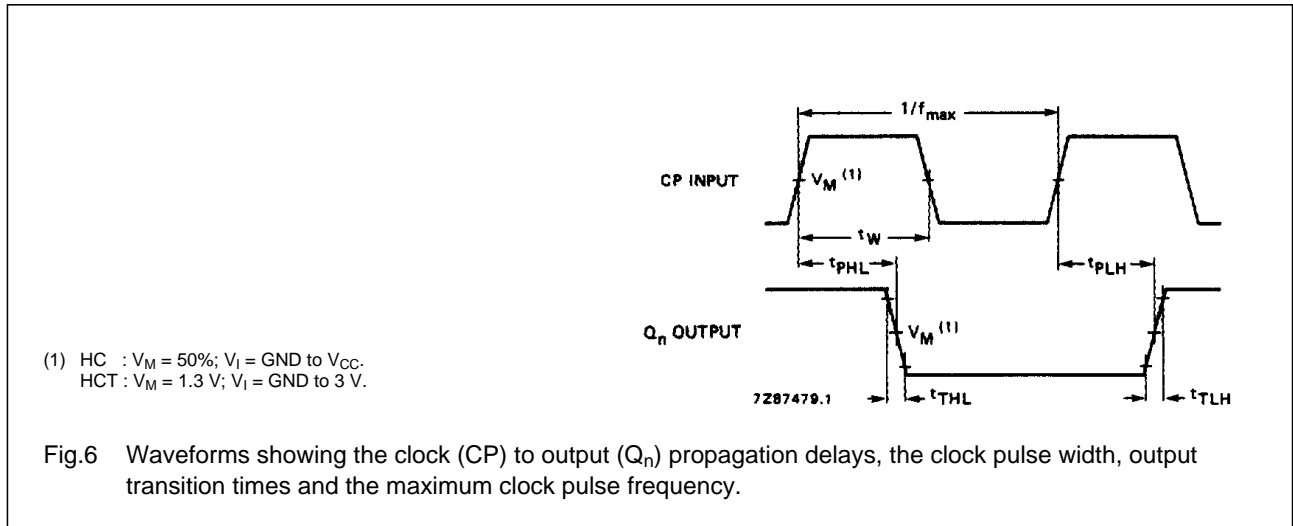
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		17	32		40		48	ns	4.5	Fig.6
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		7	15		19		22	ns	4.5	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	20	8		25		30		ns	4.5	Fig.6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	12	4		15		18		ns	4.5	Fig.7
t <sub>su</sub>	set-up time $\bar{E}$ to CP	22	12		28		33		ns	4.5	Fig.7
t <sub>h</sub>	hold time D <sub>n</sub> to CP	2	-4		2		2		ns	4.5	Fig.7
t <sub>h</sub>	hold time $\bar{E}$ to CP	3	-2		3		3		ns	4.5	Fig.7
f <sub>max</sub>	maximum clock pulse frequency	27	48		22		18		MHz	4.5	Fig.6

Octal D-type flip-flop with data enable;  
positive-edge trigger

74HC/HCT377

AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".