

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC/HCT574

Octal D-type flip-flop; positive edge-trigger; 3-state

Product specification  
File under Integrated Circuits, IC06

December 1990

## Octal D-type flip-flop; positive edge-trigger; 3-state

### 74HC/HCT574

#### FEATURES

- 3-state non-inverting outputs for bus oriented applications
- 8-bit positive edge-triggered register
- Common 3-state output enable input
- Independent register and 3-state buffer operation
- Output capability: bus driver
- $I_{CC}$  category: MSI

#### GENERAL DESCRIPTION

The 74HC/HCT574 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT574 are octal D-type flip-flops featuring separate D-type inputs for each flip-flop and non-inverting 3-state outputs for bus oriented applications. A clock (CP) and an output enable ( $\overline{OE}$ ) input are common to all flip-flops.

The 8 flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition. When  $\overline{OE}$  is LOW, the contents of the 8 flip-flops are available at the outputs.

When  $\overline{OE}$  is HIGH, the outputs go to the high impedance OFF-state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

The "574" is functionally identical to the "564", but has non-inverting outputs.

The "574" is functionally identical to the "374", but has a different pinning.

#### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay CP to $Q_n$	$C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$	14	15	ns
$f_{max}$	maximum clock frequency		123	76	MHz
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per flip-flop	notes 1 and 2	22	25	pF

#### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

#### ORDERING INFORMATION

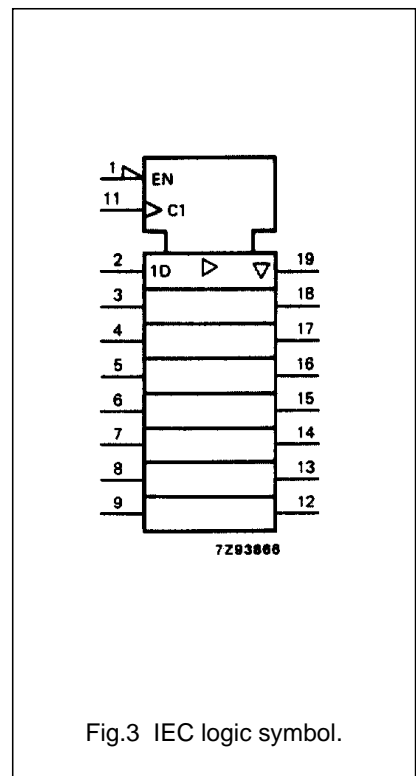
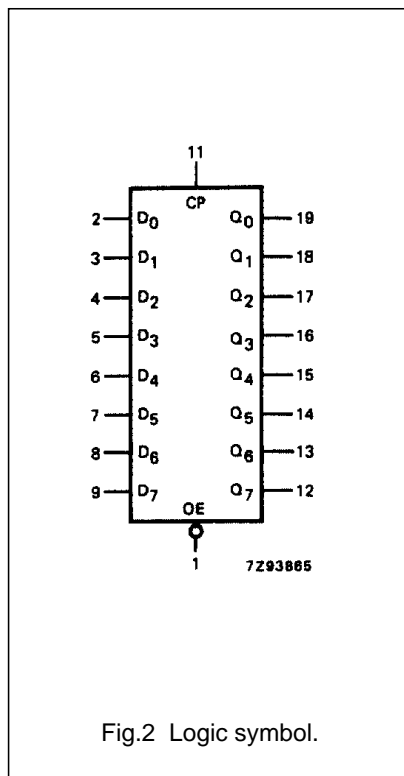
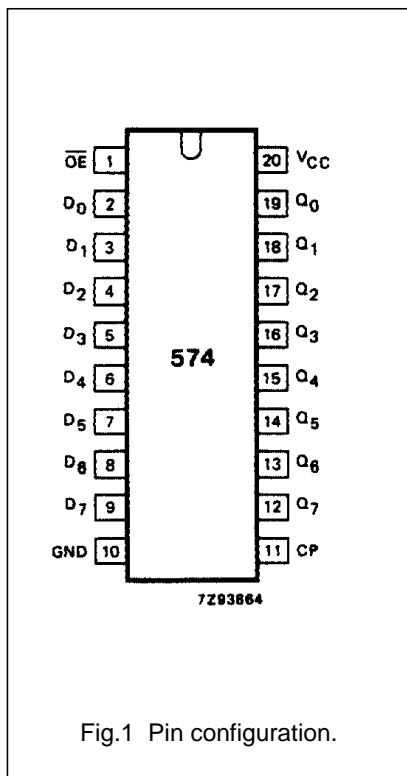
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	3-state output enable input (active LOW)
2, 3, 4, 5, 6, 7, 8, 9	D <sub>0</sub> to D <sub>7</sub>	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
19, 18, 17, 16, 15, 14, 13, 12	Q <sub>0</sub> to Q <sub>7</sub>	3-state flip-flop outputs
20	V <sub>CC</sub>	positive supply voltage



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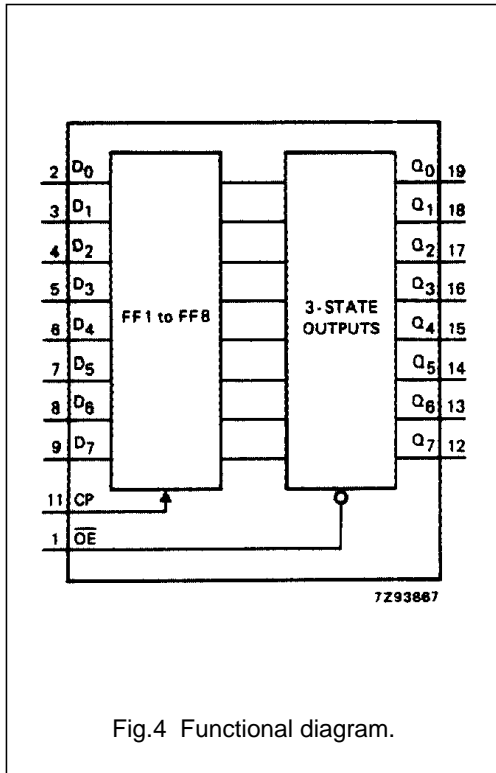


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL FLIP-FLOPS	OUTPUTS Q <sub>0</sub> to Q <sub>7</sub>
	$\overline{OE}$	CP	D <sub>n</sub>		
load and read register	L	↑	l	L	L
	L	↑	h	H	H
load register and disable outputs	H	↑	l	L	Z
	H	↑	h	H	Z

Notes

- H = HIGH voltage level  
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition  
L = LOW voltage level  
l = LOW voltage level on set-up time prior to the LOW-to-HIGH CP transition  
Z = HIGH impedance OFF-state  
↑ = LOW-to-HIGH clock transition

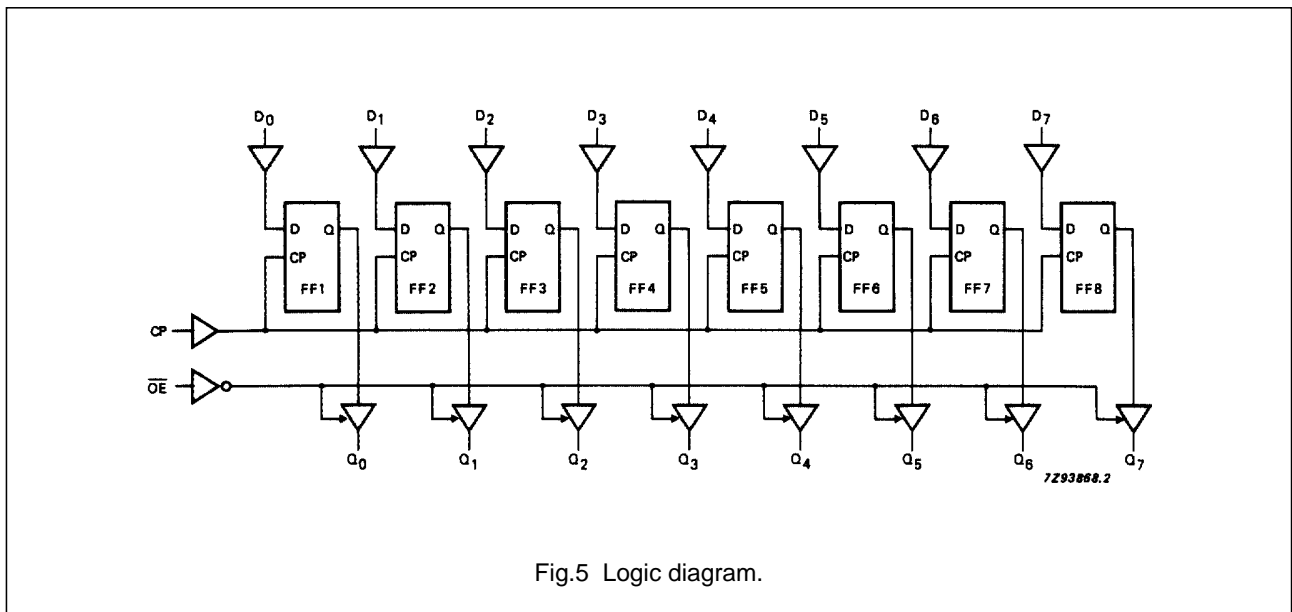


Fig.5 Logic diagram.

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HC							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		47 17 14	150 30 26		190 35 33		225 45 38	ns	2.0 4.5 6.0	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Q <sub>n</sub>		44 16 13	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Q <sub>n</sub>		39 14 11	125 25 21		155 31 26		190 38 32	ns	2.0 4.5 6.0	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.6
t <sub>su</sub>	set-up time D <sub>n</sub> to CP	60 12 10	6 2 2		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.8
t <sub>h</sub>	hold time D <sub>n</sub> to CP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig.8
f <sub>max</sub>	maximum clock pulse frequency	6.0 30 35	37 112 133		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.6

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D <sub>n</sub>	0.5
OE	1.25
CP	1.5

## AC CHARACTERISTICS FOR 74HCT

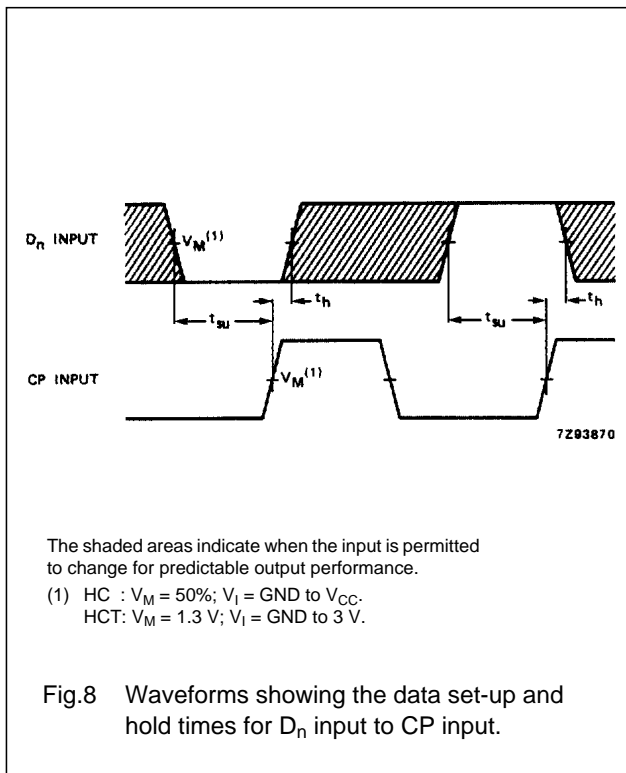
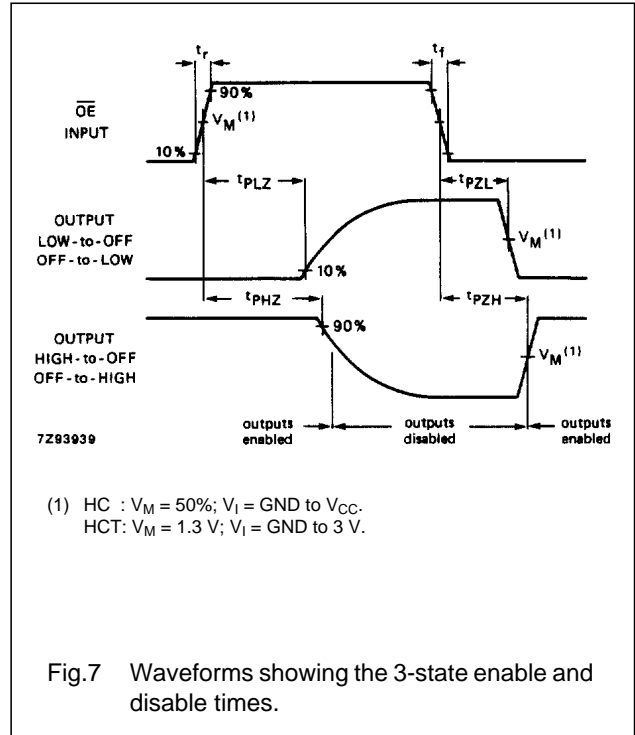
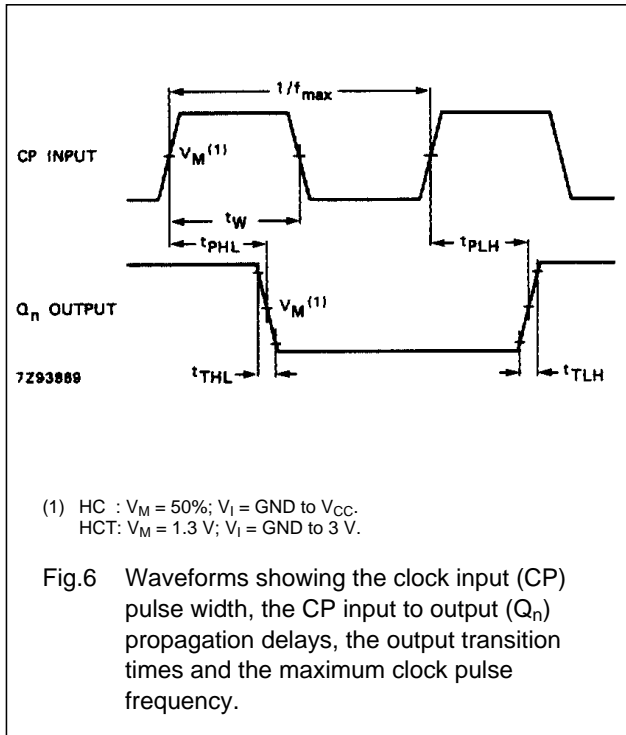
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS		
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay CP to Q <sub>n</sub>		18	33		41		50	ns	4.5	Fig.6
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time $\overline{OE}$ to Q <sub>n</sub>		19	33		41		50	ns	4.5	Fig.7
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time $\overline{OE}$ to Q <sub>n</sub>		16	28		35		42	ns	4.5	Fig.7
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.6
t <sub>W</sub>	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.6
t <sub>SU</sub>	set-up time D <sub>n</sub> to CP	12	3		15		18		ns	4.5	Fig.8
t <sub>H</sub>	hold time D <sub>n</sub> to CP	5	-1		5		5		ns	4.5	Fig.8
f <sub>max</sub>	maximum clock pulse frequency	30	69		24		20		MHz	4.5	Fig.6

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".