

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## 74HC4050

### Hex high-to-low level shifter

Product specification  
File under Integrated Circuits, IC06

December 1990

## Hex high-to-low level shifter

## 74HC4050

## FEATURES

- Output capability: standard
- I<sub>CC</sub> category: SSI

## GENERAL DESCRIPTION

The 74HC4050 is a high-speed Si-gate CMOS device and is pin compatible with the "4050" of the "4000B" series. It is specified in compliance with JEDEC standard no. 7A.

The 74HC4050 provides six non-inverting buffers with a modified input protection structure, which has no diode connected to V<sub>CC</sub>. Input voltages of up to 15 V may

therefore be used. This feature enables the non-inverting buffers to be used as logic level translators, which will convert high level logic to low level logic, while operating from a low voltage power supply. For example 15 V logic ("4000B series") can be converted down to 2 V logic.

The actual input switch level remains related to the V<sub>CC</sub> and is the same as mentioned in the family characteristics.

## APPLICATIONS

- Converting 15 V logic ("4000B" series) down to 2 V logic.

## QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25 °C; t<sub>r</sub> = t<sub>f</sub> = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
			HC	
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay nA to nY	C <sub>L</sub> = 15 pF; V <sub>CC</sub> = 5 V	7	ns
C <sub>I</sub>	input capacitance		3.5	pF
C <sub>PD</sub>	power dissipation capacitance per buffer	note 1	14	pF

## Notes

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f<sub>i</sub> = input frequency in MHz

f<sub>o</sub> = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

V<sub>CC</sub> = supply voltage in V

∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of outputs

## ORDERING INFORMATION

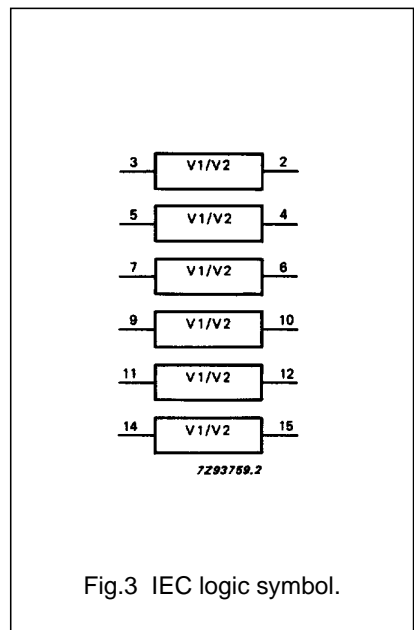
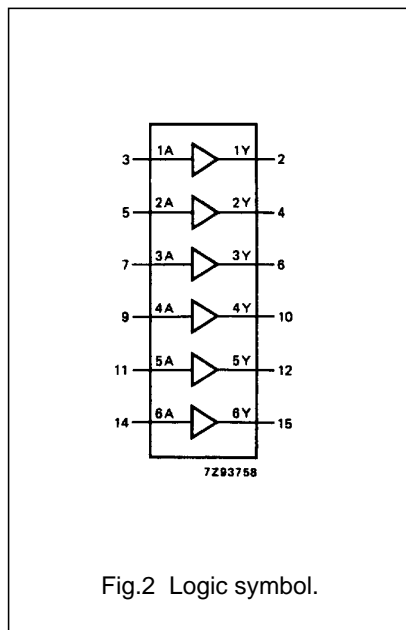
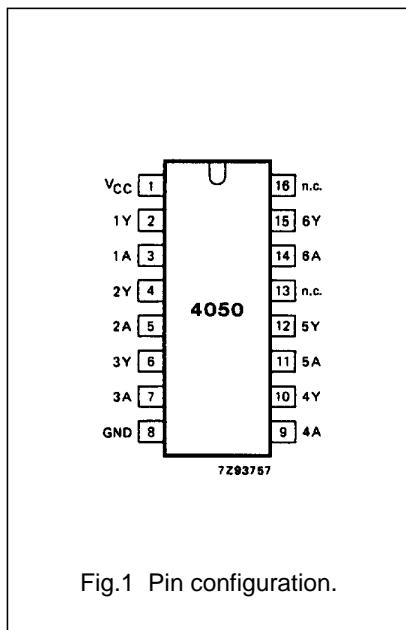
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	V <sub>CC</sub>	positive supply voltage
2, 4, 6, 10, 12, 15	1Y to 6Y	data outputs
3, 5, 7, 9, 11, 14	1A to 6A	data inputs
8	GND	ground (0 V)
13, 16	n.c.	not connected



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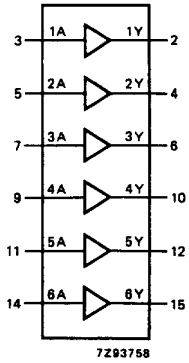


Fig.4 Functional diagram.

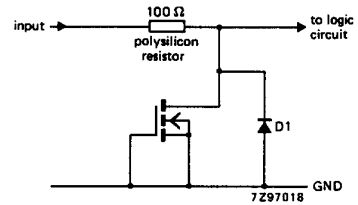


Fig.5 Input protection for HC4050. Single sided thick oxide field effect metal gate transistor as input protection.

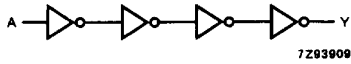


Fig.6 Logic diagram (one level shifter).

FUNCTION TABLE <sup>(1)</sup>

INPUT	OUTPUT
nA	nY
L	L
H	H

Note

- 1. H = HIGH voltage level
- L = LOW voltage level

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**RATINGS**

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+7	V	
$V_{IK}$	DC input voltage range	-0.5	+16	V	
$-I_{IK}$	DC input diode current		20	mA	for $V_I < -0.5$ V
$\pm I_{OK}$	DC output diode current		20	mA	for $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V
$\pm I_O$	DC output source or sink current - standard outputs		25	mA	for $-0.5$ V $< V_O < V_{CC} + 0.5$ V
$\pm I_{CC};$ $\pm I_{GND}$	DC $V_{CC}$ or GND current for types with: - standard outputs		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C 74HC
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	74HC			UNIT	CONDITIONS
		min.	typ.	max.		
$V_{CC}$	DC supply voltage	2.0	5.0	6.0	V	
$V_I$	DC input voltage range	GND	-	15	V	
$T_{amb}$	operating ambient temperature range	-40		+85	°C	see DC and AC characteristics
$T_{amb}$	operating ambient temperature range	-40		+125	°C	
$t_r, t_f$	input rise and fall times		6.0	1000 500 400 650 1000	ns	$V_{CC} = 2.0$ V; $V_{IN} = 2.0$ V $V_{CC} = 4.5$ V; $V_{IN} = 4.5$ V $V_{CC} = 6.0$ V; $V_{IN} = 6.0$ V $V_{CC} = 6.0$ V; $V_{IN} = 10.0$ V $V_{CC} = 6.0$ V; $V_{IN} = 15.0$ V

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**DC CHARACTERISTICS FOR 74HC**

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> (V)	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V <sub>IH</sub>	HIGH level input voltage	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V <sub>IL</sub>	LOW level input voltage		0.7 1.8 2.3	0.5 1.35 1.8		0.5 1.35 1.8	0.5 1.35 1.8		V	2.0 4.5 6.0		
V <sub>OH</sub>	HIGH level output voltage - all outputs	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 20 µA -I <sub>O</sub> = 20 µA -I <sub>O</sub> = 20 µA
V <sub>OH</sub>	HIGH level output voltage - standard outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	-I <sub>O</sub> = 4.0 mA -I <sub>O</sub> = 5.2 mA
V <sub>OL</sub>	LOW level output voltage - all outputs			0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1		V	2.0 4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 20 µA I <sub>O</sub> = 20 µA I <sub>O</sub> = 20 µA
V <sub>OL</sub>	LOW level output voltage - standard outputs			0.26 0.26		0.33 0.33	0.4 0.4		V	4.5 6.0	V <sub>IH</sub> or V <sub>IL</sub>	I <sub>O</sub> = 4.0 mA I <sub>O</sub> = 5.2 mA
± I <sub>I</sub>	input leakage current			0.1		1.0		1.0	µA	6.0	V <sub>CC</sub> or GND	
				0.5		5.0		5.0	µA	2.0 to 6.0	15 V	
I <sub>CC</sub>	quiescent supply current			2.0		20.0		40.0	µA	6.0	15 V or GND	

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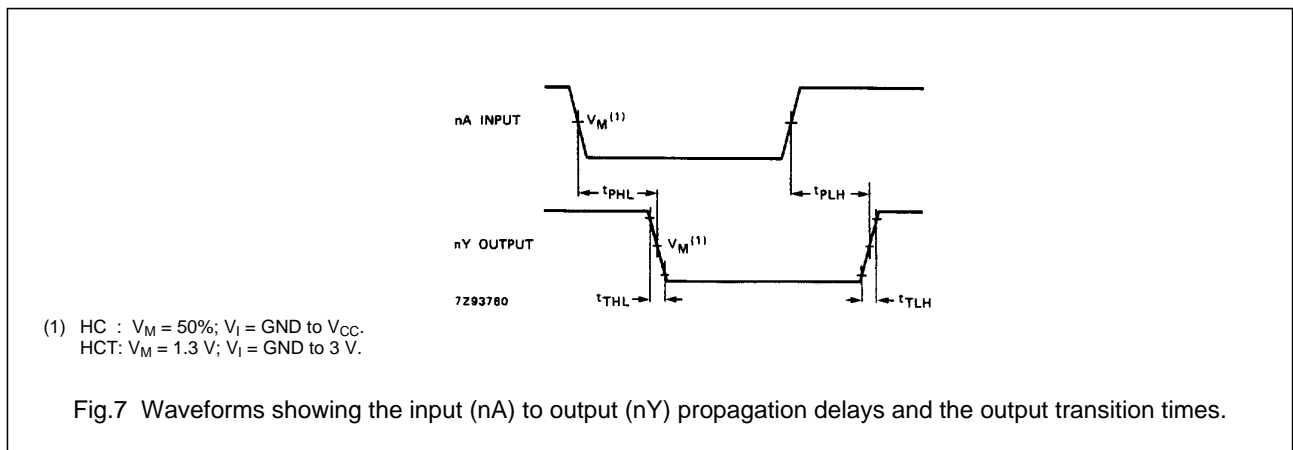
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AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS		
		74HC							$V_{CC}$ (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
$t_{PHL}/t_{PLH}$	propagation delay nA to nY		25 9 7	85 17 14		105 21 18		130 26 22	ns	2.0 4.5 6.0	Fig.7
$t_{THL}/t_{TLH}$	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7

AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".