# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

# HEF4015B
# MSI
## Dual 4-bit static shift register

Product specification
File under Integrated Circuits, IC04

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Philips Semiconductors

PHILIPS

# Dual 4-bit static shift register

# HEF4015B
# MSI

## DESCRIPTION

The HEF4015B is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (D), a clock input (CP), four fully buffered parallel outputs ($O_0$ to $O_3$) and an overriding asynchronous master reset input (MR). Information present on D is shifted to the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. A HIGH on MR clears the register and forces $O_0$ to $O_3$ to LOW, independent of CP and D. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

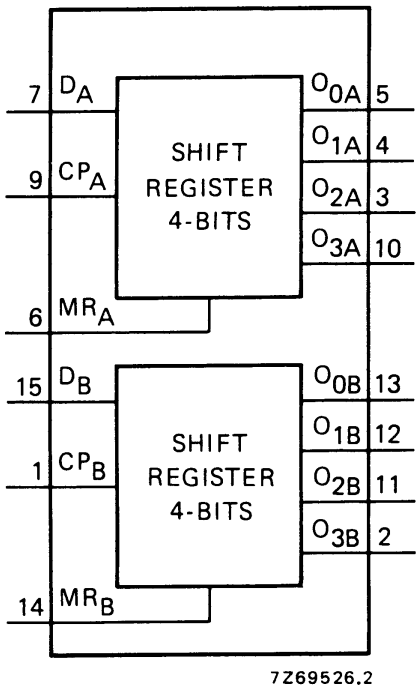


Fig.1 Functional diagram.

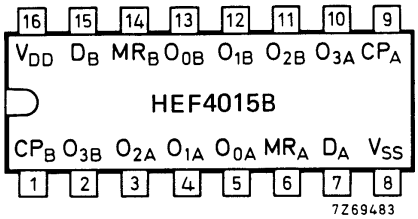


Fig.2 Pinning diagram.

HEF4015BP(N): 16-lead DIL; plastic (SOT38-1)
HEF4015BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
HEF4015BT(D): 16-lead SO; plastic (SOT109-1)
( ): Package Designator North America

## PINNING

| | |
|---|---|
| $D_A$, $D_B$ | serial data input |
| $MR_A$, $MR_B$ | master reset input (active HIGH) |
| $CP_A$, $CP_B$ | clock input (LOW-to-HIGH edge-triggered) |
| $O_{0A}$, $O_{1A}$, $O_{2A}$, $O_{3A}$ | parallel outputs |
| $O_{0B}$, $O_{1B}$, $O_{2B}$, $O_{3B}$ | parallel outputs |

## FAMILY DATA, $I_{DD}$ LIMITS category MSI

See Family Specifications

## APPLICATION INFORMATION

Some examples of applications for the HEF4015B are:

- Serial-to-parallel converter
- Buffer stores
- General purpose register

**LOGIC DIAGRAM** (one register)

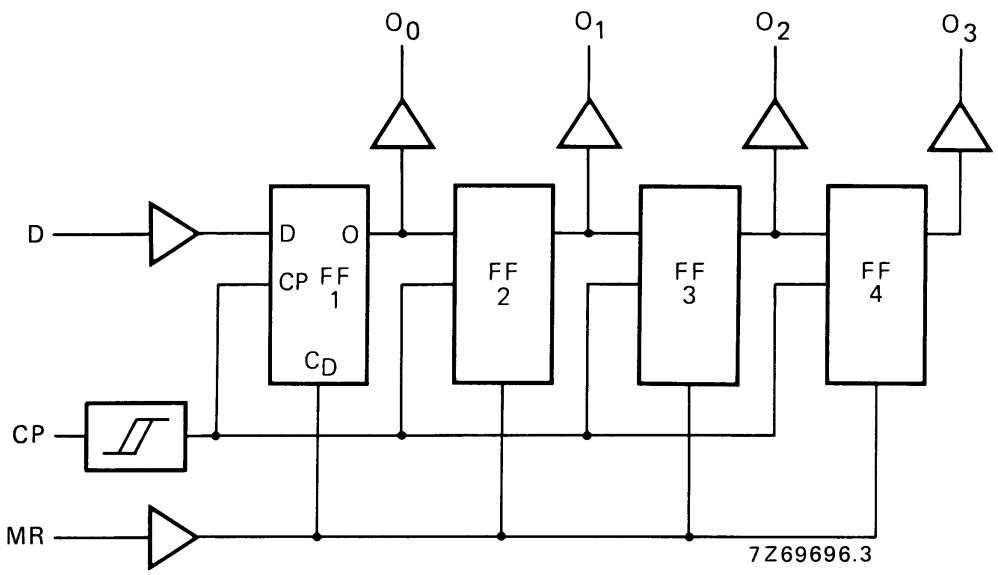


Fig.3 Logic diagram.

**FUNCTION TABLE**

| | INPUTS | | | OUTPUTS | | | |
|---|---|---|---|---|---|---|---|
| **n** | **CP** | **D** | **MR** | **$O_0$** | **$O_1$** | **$O_2$** | **$O_3$** |
| 1 | ↑ | $D_1$ | L | $D_1$ | X | X | X |
| 2 | ↑ | $D_2$ | L | $D_2$ | $D_1$ | X | X |
| 3 | ↑ | $D_3$ | L | $D_3$ | $D_2$ | $D_1$ | X |
| 4 | ↑ | $D_4$ | L | $D_4$ | $D_3$ | $D_2$ | $D_1$ |
| | ↓ | X | L | no change | | | |
| | X | X | H | L | L | L | L |

**Note**

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. ↑ = positive-going transition
5. ↓ = negative-going transition
6. $D_n$ = either HIGH or LOW
7. n = number of clock pulse transitions

**AC CHARACTERISTICS**

$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; $C_L$ = 50 pF; input transition times ≤ 20 ns

| | $V_{DD}$ V | SYMBOL | MIN. | TYP. | MAX. | | TYPICAL EXTRAPOLATION FORMULA |
|---|---|---|---|---|---|---|---|
| Propagation delays | | | | | | | |
| CP → $O_n$ | 5 | | | 130 | 260 | ns | 103 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| | 5 | | | 120 | 240 | ns | 93 ns + (0,55 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{PLH}$ | | 55 | 110 | ns | 44 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 40 | 80 | ns | 32 ns + (0,16 ns/pF) $C_L$ |
| MR → $O_n$ | 5 | | | 105 | 210 | ns | 78 ns + (0,55 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{PHL}$ | | 45 | 90 | ns | 34 ns + (0,23 ns/pF) $C_L$ |
| | 15 | | | 35 | 70 | ns | 27 ns + (0,16 ns/pF) $C_L$ |
| Output transition times | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| HIGH to LOW | 10 | $t_{THL}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| | 5 | | | 60 | 120 | ns | 10 ns + (1,0 ns/pF) $C_L$ |
| LOW to HIGH | 10 | $t_{TLH}$ | | 30 | 60 | ns | 9 ns + (0,42 ns/pF) $C_L$ |
| | 15 | | | 20 | 40 | ns | 6 ns + (0,28 ns/pF) $C_L$ |
| Set-up time | 5 | | 25 | –15 | | ns | see waveforms Figs 4 and 5 |
| D → CP | 10 | $t_{su}$ | 25 | –10 | | ns | |
| | 15 | | 20 | –5 | | ns | |
| Hold time | 5 | | 40 | 20 | | ns | |
| D → CP | 10 | $t_{hold}$ | 20 | 10 | | ns | |
| | 15 | | 15 | 8 | | ns | |
| Minimum clock | 5 | | 60 | 30 | | ns | |
| pulse width; LOW | 10 | $t_{WCPL}$ | 30 | 15 | | ns | |
| | 15 | | 20 | 10 | | ns | |
| Minimum MR | 5 | | 80 | 40 | | ns | |
| pulse width; HIGH | 10 | $t_{WMRH}$ | 30 | 15 | | ns | |
| | 15 | | 24 | 12 | | ns | |
| Recovery time | 5 | | 50 | 20 | | ns | |
| for MR | 10 | $t_{RMR}$ | 30 | 10 | | ns | |
| | 15 | | 20 | 5 | | ns | |
| Maximum clock | 5 | | 7 | 15 | | MHz | |
| pulse frequency | 10 | $f_{max}$ | 15 | 30 | | MHz | |
| | 15 | | 22 | 44 | | MHz | |

| | $V_{DD}$ V | TYPICAL FORMULA FOR P (μW) | |
|---|---|---|---|
| Dynamic power dissipation per package (P) | 5 | $1\,500\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | where |
| | 10 | $6\,300\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | $f_i$ = input freq. (MHz) |
| | 15 | $17\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$ | $f_o$ = output freq. (MHz) |
| | | | $C_L$ = load capacitance (pF) |
| | | | $\sum (f_o C_L)$ = sum of outputs |
| | | | $V_{DD}$ = supply voltage (V) |

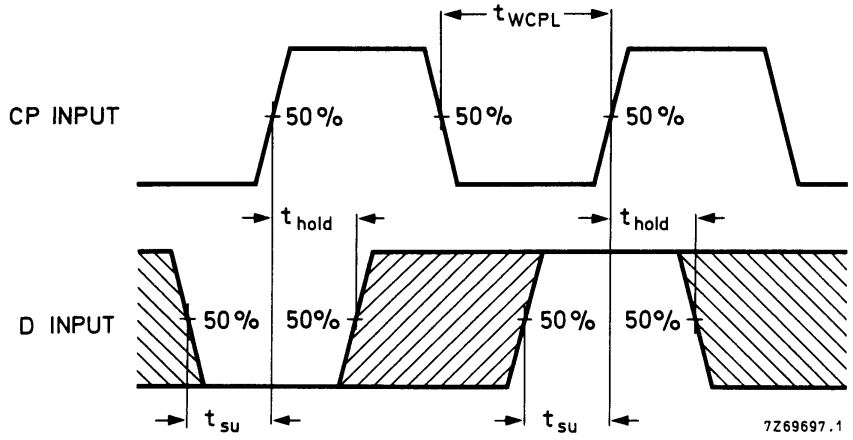


Fig.4 Waveforms showing set-up times, hold times and minimum clock pulse width. Set-up and hold times are shown as positive values but may be specified as negative values.

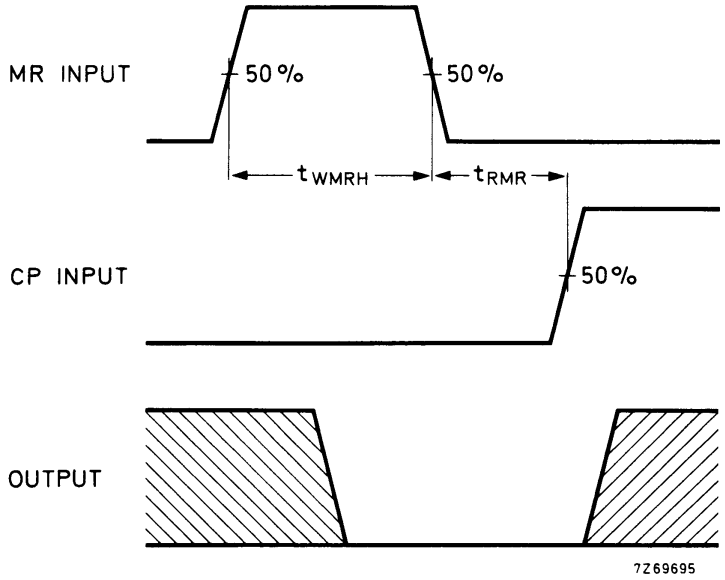


Fig.5 Waveforms showing recovery time for MR and minimum MR pulse width.