

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40174B **MSI** Hex D-type flip-flop

Product specification
File under Integrated Circuits, IC04

January 1995

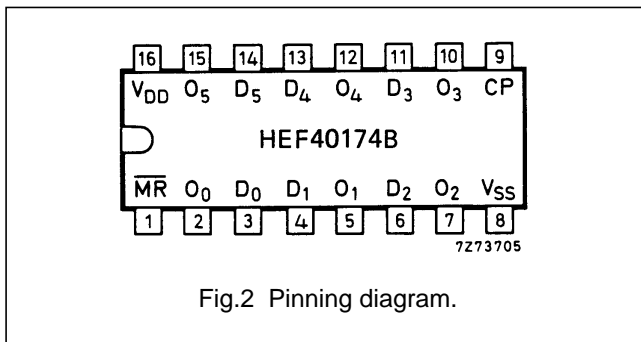
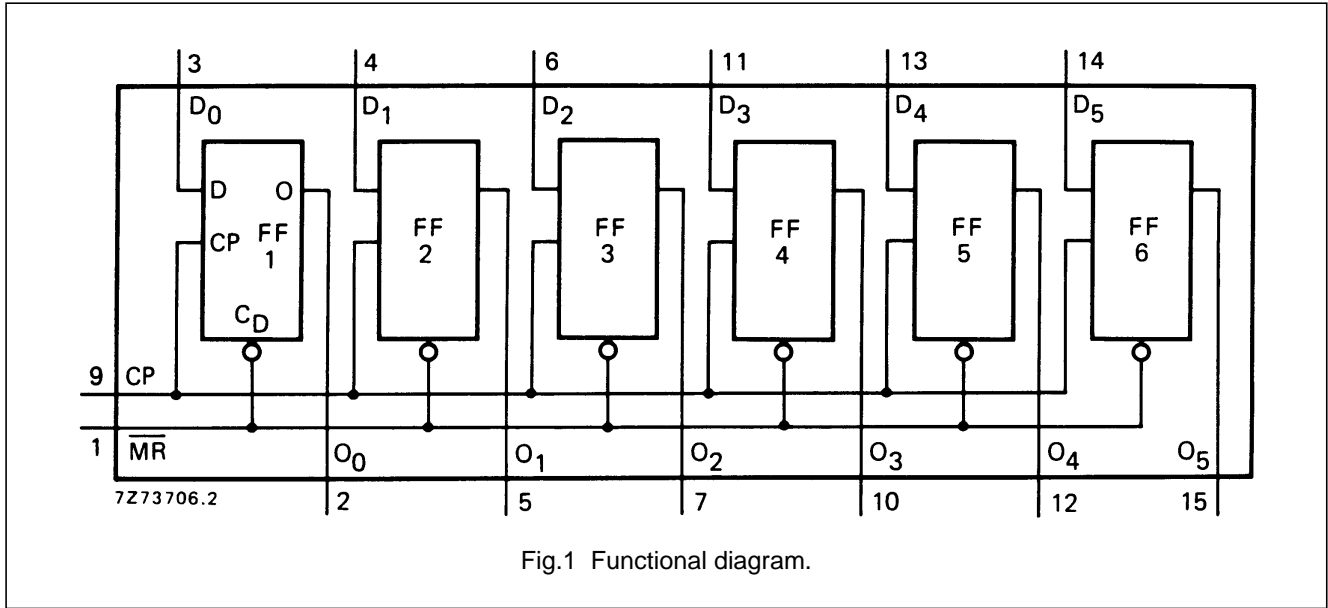
Hex D-type flip-flop

HEF40174B MSI

DESCRIPTION

The HEF40174B is a hex edge-triggered D-type flip-flop with six data inputs (D₀ to D₅), a clock input (CP), an overriding asynchronous master reset input (MR), and six

buffered outputs (O₀ to O₅). Information on D₀ to D₅ is transferred to O₀ to O₅ on the LOW to HIGH transition of CP if MR is HIGH. When LOW, MR resets all flip-flops (O₀ to O₅ = LOW) independent of CP and D₀ to D₅.



PINNING

- D₀ to D₅ data inputs
- CP clock input (LOW to HIGH; edge-triggered)
- MR master reset input (active LOW)
- O₀ to O₅ buffered outputs

FUNCTION TABLE

INPUTS			OUTPUT
CP	D	MR	O
	H	H	H
	L	H	L
	X	H	no change
X	X	L	L

Notes

1. H = HIGH state (the more positive voltage)
 L = LOW state (the less positive voltage)
 X = state is immaterial
- = positive-going transition
- = negative-going transition

- HEF40174BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF40174BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF40174BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays $CP \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		75	155 ns	$48\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10			30	65 ns		$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			20	45 ns		$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{PLH}		75	155 ns	$48\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10			30	65 ns		$19\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			20	45 ns		$12\text{ ns} + (0,16\text{ ns/pF}) C_L$
$\overline{MR} \rightarrow O_n$ HIGH to LOW	5	t_{PHL}		85	175 ns	$58\text{ ns} + (0,55\text{ ns/pF}) C_L$	
	10			35	70 ns		$24\text{ ns} + (0,23\text{ ns/pF}) C_L$
	15			25	50 ns		$17\text{ ns} + (0,16\text{ ns/pF}) C_L$
Output transition times HIGH to LOW	5	t_{THL}		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10			30	60 ns		$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns		$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
LOW to HIGH	5	t_{TLH}		60	120 ns	$10\text{ ns} + (1,0\text{ ns/pF}) C_L$	
	10			30	60 ns		$9\text{ ns} + (0,42\text{ ns/pF}) C_L$
	15			20	40 ns		$6\text{ ns} + (0,28\text{ ns/pF}) C_L$
Set-up time $D_n \rightarrow CP$	5	t_{su}	20	10	ns	see also waveforms Fig.4	
	10		10	5	ns		
	15		10	5	ns		
Hold time $D_n \rightarrow CP$	5	t_{hold}	10	0	ns		
	10		5	0	ns		
	15		5	0	ns		
Minimum clock pulse width; LOW	5	t_{WCPL}	70	35	ns		
	10		30	15	ns		
	15		20	10	ns		
Minimum \overline{MR} pulse width; LOW	5	t_{WMRL}	70	35	ns		
	10		35	15	ns		
	15		25	10	ns		
Recovery time for \overline{MR}	5	t_{RMR}	45	25	ns		
	10		20	10	ns		
	15		15	5	ns		
Maximum clock pulse frequency	5	f_{max}	5	11	MHz		
	10		15	30	MHz		
	15		20	45	MHz		

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	V_{DD} V	TYPICAL FORMULA FOR P(μ W)	
Dynamic power dissipation per package (P)	5 10 15	$3500 f_i + \sum (f_o C_L) \times V_{DD}^2$ $16\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$ $42\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	where f_i = input freq. (MHz) f_o = output freq. (MHz) C_L = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs V_{DD} = supply voltage (V)

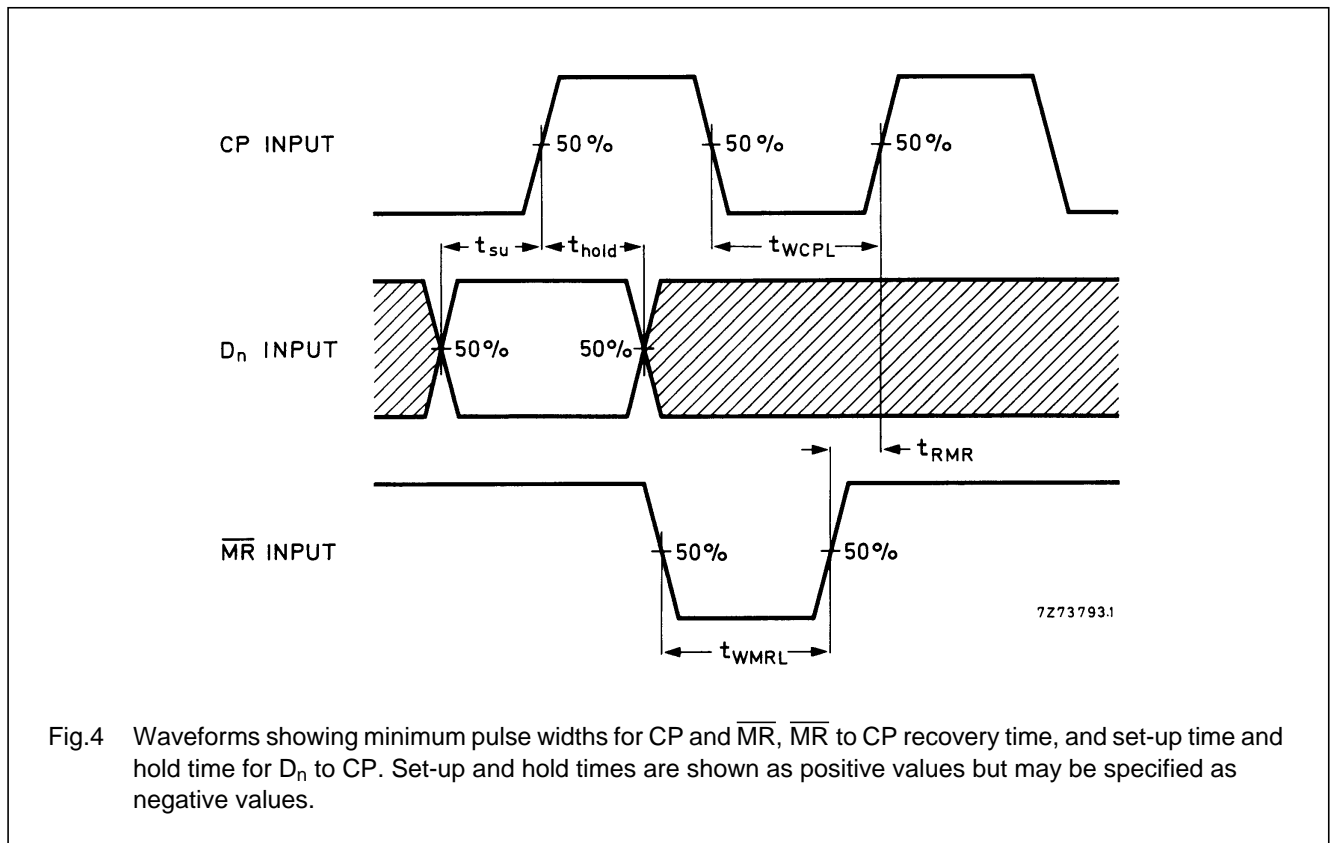


Fig.4 Waveforms showing minimum pulse widths for CP and MR, MR to CP recovery time, and set-up time and hold time for D_n to CP. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40174B are:

- Shift registers
- Buffer/storage register
- Pattern generator